ABSTRACT OF THE DISCLOSURE

This invention provides a clock recovery circuit capable of detecting a timing point of demodulation in a very short time and obtaining a desired demodulation signal, a digital demodulator including such a clock recovery circuit, a bit error rate estimation means capable of minimizing degradation of the communication efficiency and an AFC circuit permitting corrections along the right direction for providing desired values.

The digital demodulator of this invention for demodulating a detection signal obtained by detecting a modulation wave by predetermined detection means based on a timing clock signal includes correlation detection means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of the sampling points; correlation judgement means for comparing the correlations detected by the correlation detection means, judging the pair of sampling points which maximize the correlation and another pair of sampling points providing the next largest correlation, and producing a timing clock signal based on the judgement; and phase shift means for shifting the phase of the signal in the demodulation process so as to equalize the correlations of the two pairs of sampling points.

The bit error rate estimation means samples a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol

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cycle), detects correlations between each adjacent pair of the sampling points, and estimates a bit error rate based on the distribution of the detected correlations.

Further, the AFC circuit includes a bit error rate estimation means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle, detecting correlations between each adjacent pair of the sampling points, and estimating a bit error rate based on the distribution of the detected correlations; and a bit error rate measuring device for measuring a bit error rate based on a series of data inserted in the modulation wave at a predetermined interval for measuring the bit error rate, whereby the frequency drift can be corrected by comparing both the bit error rates.

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