MEMORY CIRCUIT, DATA TRANSMISSION CIRCUIT, AND MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure is proposed based on and claims the priority to Chinese Patent Application 202210174060.X, titled "MEMORY CIRCUIT, DATA TRANSMISSION CIRCUIT, AND MEMORY", filed on February 24, 2022, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to, but is not limited to, a memory circuit, a data transmission circuit, and a memory.

BACKGROUND

[0003] Dynamic random access memory (~~Dynamic Random Access Memory,~~ DRAM) is commonly used as a storage device for mobile devices due to the characteristics such as non-volatility, power reduction, small size, and no mechanical structure.

[0004] With the advancement of technology, consumers have increasingly high requirements for the performance of mobile devices. In this case, the transmission rate becomes a key parameter for evaluating the quality of the storage device.

SUMMARY

[0005] To overcome the problem existing in the related art, the present disclosure provides a memory circuit, a data transmission circuit, and a memory, to improve the

transmission efficiency of read/written data of a memory and ensure the accuracy of data transmission.

[0006] An exemplary embodiment of the present disclosure provides a memory circuit, arranged adjacent to a data transmission region and including: at least one memory structure arranged parallel to the data transmission region, wherein the memory structure includes a first memory array and a second memory array arranged adjacent to each other in a first direction, a distance between the first memory array and the data transmission region is less than a distance between the second memory array and the data transmission region, and the first direction is a direction of approaching the data transmission region; the first memory array includes a read/write module and a forwarding module; the second memory array includes a read/write module; the first memory array performs a data interaction with the data transmission region based on the read/write module in the first memory array; and the second memory array performs a data transmission with the data transmission region based on the read/write module in the second memory array and the forwarding module in the first memory array.

[0007] By setting the forwarding module, during data reading/writing in the second memory array, data is prevented from being forwarded through the read/write module of the first memory array, so that data transmission paths of the first memory array and the second memory array are separated from each other. Subsequently, data reading/writing of the first memory array and the second memory array can be performed alternately, thereby reducing the difference between data reading delays of different memory arrays, preventing read data with a relatively long delay from truncating read data with a relatively short delay, and improving the margin of data transmission. In addition, by separating the data transmission paths of the first memory array and the second memory array, in the process of data writing/reading, a transmission direction of data can be determined by determining whether the data belongs to a writing process or a reading process. This avoids the complex data path determining process when the same data transmission path is used, thereby achieving a higher data transmission rate and higher accuracy of data transmission.

[0008] In an exemplary embodiment, the first memory array and the second memory array each include an even number of memory blocks that are successively arranged in the first direction, two adjacent non-repeated memory blocks share one read/write module, and the read/write module is arranged between two corresponding memory blocks.

[0009] In an exemplary embodiment, the memory block further includes a plurality of memory sub-blocks successively arranged in a second direction perpendicular to the first direction, and the plurality of memory sub-blocks share one read/write module.

[0010] In an exemplary embodiment, the read/write module in the first memory array and the read/write module in the second memory array are arranged in the first direction, and in a second direction perpendicular to the first direction, the forwarding module is arranged at a corresponding side of the read/write module. Through structured arrangement of the read/write module and the forwarding module, a data transmission wire between the read/write module and the forwarding module can be arranged in a structured manner. The resistance of the data transmission wire can be reduced by using minimizing the length of the data transmission wire, thereby improving the rate and accuracy of data transmission.

[0011] In an exemplary embodiment, one forwarding module is arranged at a corresponding side of each read/write module. Through short-distance transmission between a plurality of forwarding modules and multiple forwarding of data, the possibility of errors in the data transmission process is reduced.

[0012] In an exemplary embodiment, data transmission wires between the read/write module and the data transmission region and data transmission wires between the forwarding module and the data transmission region are arranged between adjacent power supply wires; the power supply wire is configured to receive and transmit a power supply signal, to provide the power supply signal to the first memory array and the second memory array. By arranging the data transmission wires between the power supply wires, the layout area occupied by the memory array will not be increased.

[0013] In an exemplary embodiment, the data transmission wires include a low-bit transmission wire and a high-bit transmission wire; the low-bit transmission wire is configured to transmit low-bit data in a memory array, and the high-bit transmission wire is configured to transmit high-bit data in the memory array, to further improve the data transmission efficiency and data transmission efficiency.

[0014] An exemplary embodiment of the present disclosure further provides a data transmission circuit, arranged in a data transmission region and including: at least two data transmission structures, wherein each of the data transmission structures is connected to at least one memory circuit provided by the foregoing embodiment and is configured to read data from the memory circuit and write data into the memory circuit; each of the data transmission structures includes a memory transmission terminal, a bus transmission terminal, and an interactive transmission terminal; the memory transmission terminal is configured to connect the memory circuit, the bus transmission terminal is configured to connect a data bus, and the interactive transmission terminal is configured to connect another one of the data transmission structures; data inputted from the memory transmission terminal is outputted through the bus transmission terminal or the interactive transmission terminal; data inputted from the bus transmission terminal is outputted through the memory transmission terminal or the interactive transmission terminal; data inputted from the interactive transmission terminal is outputted through the bus transmission terminal or the memory transmission terminal; and the data inputted from the interactive transmission terminal is data inputted through the bus transmission terminal or the memory transmission terminal of the another one of the data transmission structures; and a control module, connected to the data transmission structure and receiving an input control signal and an adjustment control signal that are provided by a memory that the control module belongs to; wherein the control module is configured to output the input control signal in a delayed manner based on the adjustment control signal, so as to generate an output control signal corresponding to the input control signal, and the input control signal and the output control signal are used for indicating a data transmission path of the data transmission structure.

[0015] In an exemplary embodiment, the data transmission structure includes: an input unit, configured to receive at least one piece of input data and the input control signal, and output input data corresponding to the input control signal based on the input control signal; an output unit, configured to receive the input data outputted by the input unit and at least one output control signal, and output input data based on a valid port represented by the output control signal; and a latch unit, connected to the output unit and configured to latch the input data outputted by the output unit.

[0016] In an exemplary embodiment, the input unit includes: a plurality of input controllers, wherein each of the input controllers corresponds to the memory transmission terminal, the bus transmission terminal, or the interactive transmission terminal. Each of the input controllers is configured to correspondingly receive the input data from the memory transmission terminal, the bus transmission terminal or the interactive transmission terminal and the input control signal; and the input controller is configured to be turned on based on the input control signal, to output the input data.

[0017] In an exemplary embodiment, the output unit includes: a plurality of output controllers, wherein each of the output controllers corresponds to the memory transmission terminal, the bus transmission terminal or the interactive transmission terminal; each of the output controllers is configured to receive the input data outputted by the input unit corresponding to the memory transmission terminal, the bus transmission terminal or the interactive transmission terminal and the output control signal; and the output controller is configured to be turned on based on the output control signal, to output the input data.

[0018] In an exemplary embodiment, the data transmission structure further includes: an input selection unit, configured to receive at least one input control signal, and generate a strobe corresponding to the input control signal, wherein the strobe corresponds to a valid port represented by the input control signal, and a selection delay exists between the strobe and the input control signal; and a trigger unit, including a clock terminal connected to the input selection unit, an input terminal connected to the input unit, and an output terminal connected to the output unit, and

configured to transmit, based on the strobe, input data received by the input terminal to the output terminal.

[0019] In an exemplary embodiment, the input selection unit includes: a trigger sub-unit, configured to receive the at least one input control signal, and generate an indication signal if the input control signal is received; a delay sub-unit, connected to the trigger sub-unit, and configured to delay the indication signal; and a conversion sub-unit, connected to the delay sub-unit, and configured to convert the indication signal delayed into the strobe.

[0020] In an exemplary embodiment, the data transmission structure further includes: an inverter unit, disposed between the trigger unit and the input unit, and configured to output the input data or invert and output the input data based on an inversion control signal.

[0021] In an exemplary embodiment, the inverter unit includes: a flip control sub-unit, configured to receive the inversion control signal, and generate a first control signal and a second control signal based on the inversion control signal; a first selection sub-unit and a second selection sub-unit connected in parallel, wherein an input terminal of the first selection sub-unit and an input terminal of the second selection sub-unit are configured to receive the input data, and an output terminal of the first selection sub-unit and an output terminal of the second selection sub-unit are connected to the trigger unit. The first selection sub-unit is configured to be turned on based on the first control signal, and invert and output the input data; and the second selection sub-unit is configured to be turned on based on the second control signal, and output the input data.

[0022] In an exemplary embodiment, the memory transmission terminal includes a first transmission terminal, a second transmission terminal, a third transmission terminal, and a fourth transmission terminal; the bus transmission terminal includes a fifth transmission terminal and a sixth transmission terminal; the interactive transmission terminal includes a seventh transmission terminal and an eighth transmission terminal; the first transmission terminal and the second transmission terminal are connected to the first memory array; the third transmission terminal and

the fourth transmission terminal are connected to the second memory array; the first transmission terminal and the third transmission terminal are configured to transmit low-bit data; the second transmission terminal and the fourth transmission terminal are configured to transmit high-bit data; the fifth transmission terminal and the sixth transmission terminal are configured to perform an interactive data transmission between the data bus and the data transmission structure that the fifth transmission terminal and the sixth transmission terminal belong to; and the seventh transmission terminal and the eighth transmission terminal are configured to perform an interactive data transmission between two data transmission structures.

[0023] In an exemplary embodiment, the fifth transmission terminal is configured to perform the interactive data transmission between the data bus and the data transmission structure that the fifth transmission terminal belongs to; and the sixth transmission terminal is configured to perform a one-way data transmission from the data transmission structure, that the sixth transmission terminal belongs to, to the data bus.

[0024] An exemplary embodiment further provides a memory, which adopts the memory circuit provided by the foregoing embodiment to arrange memory arrays, so as to improve transmission efficiency of read/written data of the memory and ensure accuracy of data transmission.

BRIEF DESCRIPTION OF DRAWINGS

[0025] The accompanying drawings which constitute a part of the present disclosure provide further comprehension of the present disclosure. The schematic embodiments of the present disclosure and description thereof are intended to explain the present disclosure and do not constitute an improper limitation to the present disclosure. In the accompanying drawings:

[0026] FIG. 1 is a schematic diagram of a virtual structure of a memory circuit according to an embodiment of the present disclosure;

[0027] FIG. 2 is a specific schematic structural diagram of a memory circuit

according to an embodiment of the present disclosure;

[0028] FIG. 3 is another specific schematic structural diagram of a memory circuit according to an embodiment of the present disclosure;

[0029] FIG. 4 is a schematic structural diagram of a data transmission circuit according to another embodiment of the present disclosure;

[0030] FIG. 5 is a specific schematic structural diagram of a control module according to another embodiment of the present disclosure;

[0031] FIG. 6 is schematic diagram of a specific connection manner of a data transmission structure according to another embodiment of the present disclosure;

[0032] FIG. 7 is a specific schematic structural diagram of a data transmission structure during data reading according to another embodiment of the present disclosure; and

[0033] FIG. 8 is a specific schematic structural diagram of a data transmission structure during data writing according to another embodiment of the present disclosure.

DESCRIPTION OF EMBODIMENTS

[0034] To make the objectives, technical solutions, and advantages of the embodiments of the present disclosure clearer, the following clearly and completely describes the technical solutions in the embodiments of the present disclosure with reference to the accompanying drawings in the embodiments of the present disclosure. Apparently, the described embodiments are some but not all of the embodiments of the present disclosure. All other embodiments obtained by those of ordinary skill in the art based on the embodiments of the present disclosure without creative efforts should fall within the protection scope of the present disclosure. It should be noted that the embodiments in the present disclosure and features in the embodiments may be combined with each other in a non-conflicting manner.

[0035] FIG. 1 is a schematic diagram of a virtual structure of a memory circuit according to this embodiment; FIG. 2 is a specific schematic structural diagram of a

memory circuit according to this embodiment; FIG. 3 is another specific schematic structural diagram of a memory circuit according to this embodiment. The following details the memory circuit according provided by this embodiment with reference to the accompanying drawings.

[0036] Referring to FIG. 1, the memory circuit is arranged adjacent to the data transmission region 100.

[0037] The memory circuit includes at least one memory structure 400 arranged parallel to the data transmission region 100. The memory structure 400 includes: a first memory array 401 and a second memory array 402 that are arranged adjacent to each other in a first direction X. The first direction X is a direction of approaching the data transmission region 100, and a distance between the first memory array 401 and the data transmission region 100 is less than a distance between the second memory array 402 and the data transmission region 100. That is, in the same memory structure 400, the first memory array 401 is arranged close to the data transmission region 100, and the second memory array 402 is arranged away from the data transmission region 100.

[0038] The first memory array 401 includes: a read/write module 410 and a forwarding module 420. The first memory array 401 performs data interaction with the data transmission region based on the read/write module 410 in the first memory array 401. The second memory array 402 includes: a read/write module 410. The second memory array 402 performs data interaction with the data transmission region 100 based on the read/write module 410 in the second memory array 402 and the forwarding module 420 in the first memory array 401.

[0039] That is, in the embodiment of the present disclosure, the read/write module 410 is configured to directly interact with a memory cell in the memory array that the read/write module 410 belongs to. An input written from the data transmission region 100 is transferred through a plurality of read/write modules 410 in the memory array, to implement writing into different memory cells in the memory array. Data is transferred to a memory array away from the data transmission region 100 rapidly and accurately by disposing a forwarding module 420 in a memory array close to the data

transmission region 100.

[0040] Specifically, by setting the forwarding module 420, during data reading/writing in the second memory array 402, data is prevented from being forwarded through the read/write module 410 of the first memory array 401, so that data transmission paths of the first memory array 401 and the second memory array 402 are separated from each other. Subsequently, data reading/writing of the first memory array 401 and the second memory array 402 can be performed alternately, thereby reducing the difference between data reading delays of different memory arrays, preventing read data with a relatively long delay from truncating read data with a relatively short delay, and improving the margin of data transmission. In addition, by separating the data transmission paths of the first memory array 401 and the second memory array 402, in the process of data writing/reading, a transmission direction of data can be determined by determining whether the data belongs to a writing process or a reading process. This avoids the complex data path determining process when the same data transmission path is used, thereby achieving a higher data transmission rate and higher accuracy of data transmission.

[0041] Referring to FIG. 2, in this embodiment, the first memory array 401 and the second memory array 402 each include: an even number of memory blocks 430 that are successively arranged in the first direction X, two adjacent non-repeated memory blocks share one read/write module 410, and the read/write module is arranged between the two corresponding memory blocks 430.

[0042] Specifically, each memory block 430 includes a plurality of memory cells, and the memory block 430 performs data reading/writing through the read/write modules 410 adjacent to each other. More specifically, the memory block 430 includes a plurality of word lines and a plurality of bit lines. Each memory cell corresponds to one word line and one bit line. By conducting a specific word line and bit line, a target memory cell in the memory block 430 is connected to the read/write module 410, so that the read/write module 410 reads data from or writes data into different memory cells in the memory block 430.

[0043] Referring to FIG. 2 and FIG. 3, in some embodiments, the read/write

module 410 in the first memory array 401 and the read/write module in the second memory array 402 are arranged along the first direction X, and in a second direction perpendicular to the first direction X, the forwarding module 420 is arranged at a corresponding side of the read/write module 410. Through structured arrangement of the read/write module 410 and the forwarding module, a data transmission wire between the read/write module 410 and the forwarding module 420 can be arranged in a structured manner. The resistance of the data transmission wire can be reduced by minimizing the length of the data transmission wire, thereby improving the rate and accuracy of data transmission.

[0044] Further, in this embodiment, the forwarding module 420 is arranged at a corresponding side of each read/write module 410. Through short-distance transmission between a plurality of forwarding modules 420 and multiple forwarding of data, the possibility of errors in the data transmission process is reduced.

[0045] It should be noted that, in the accompanying drawings of this embodiment, the forwarding module 420 being arranged at a corresponding side of each read/write module 410 does not limit this embodiment. In other embodiments, the foregoing technical effect can still be achieved while the quantity of forwarding modules is reduced.

[0046] In a specific circuit design, data transmission wires between the read/write module 410 and the data transmission region 100 and data transmission wires between the forwarding module 420 and the data transmission region 100 are arranged between adjacent power supply wires; the power supply wire is configured to receive and transmit a power supply signal, to provide a power supply signal to the first memory array 401 and the second memory array 402.

[0047] Specifically, the data reading/writing process of each memory cell in the first memory array 401 and the second memory array 402 requires a charging/discharging process, and an internal power supply of the memory is needed to charge the memory cell. That is, in the design process of the memory cell layout, a corresponding power supply network needs to be disposed, to be connected to the internal power supply. The power supply network includes power supply wires

extending towards different directions. By arranging the data transmission wires between power supply wires, the power supply wires can be used as shielding wires, to suppress data interference between adjacent data transmission wires. Meanwhile, it is unnecessary to add extra shielding wires or extra layout.

[0048] In addition, in some embodiments, referring to FIG. 2 and FIG. 3, the data transmission wires further include a low-bit transmission wire and a high-bit transmission wire. The low-bit transmission wire is configured to transmit low-bit data in the memory array, and the high-bit transmission wire is configured to transmit high-bit data in the memory array.

[0049] In an example, if the memory array transmits 16 bits of data each time, the low-bit transmission wire is configured to transmit the first bit to the eight bit of data, and the high-bit transmission wire is configured to transmit ninth bit to the 16th bit of data. In addition, in some embodiments, if the memory array transmits 8 bits of data each time, the low-bit transmission wire and the high-bit transmission wire are configured to transmit data stored by different memory arrays. That is, the low-bit transmission wire and the high-bit transmission wire are used as parallel data transmission wires to transmit data, to further improve the data transmission efficiency and the accuracy of data transmission.

[0050] In some embodiments, referring to FIG. 3, the memory block 430 further includes: a plurality of memory sub-blocks 440 successively arranged in a second direction perpendicular to the first direction X. The plurality of memory sub-blocks 440 share one read/write module 410. That is, a plurality of memory sub-blocks 440 of the same memory block 430 that are arranged in a direction parallel to the data transmission region 100 share the neighboring read/write module 410.

[0051] It should be noted that, in this embodiment, one memory structure 400 only including the first memory array 401 and the second memory array 402 is taken as an example for description. In practical applications, the memory structure 400 may further include a third memory array. In this case, corresponding forwarding modules 420 are disposed in the first memory array and the second memory array respectively, thereby implementing data reading/writing of the third memory array.

Correspondingly, a fourth memory array and the like may further be disposed. That is, any specific implementation in which a different data transmission path is disposed for each memory array shall fall within the protection scope of the present disclosure.

[0052] It should be noted that, in this embodiment, one memory structure 400 arranged in a parallel manner is taken as an example for description, which does not limit this embodiment. In other embodiments, a plurality of memory structures may be arranged in the first direction X, and the data transmission manner of each memory structure is the same as that of the memory structure described above.

[0053] In this embodiment, by setting the forwarding module 420, during data reading/writing in the second memory array 402, data is prevented from being forwarded through the read/write module 410 of the first memory array 401, so that data transmission paths of the first memory array 401 and the second memory array 402 are separated from each other. Subsequently, data reading/writing of the first memory array 401 and the second memory array 402 can be performed alternately, thereby reducing the difference between data reading delays of different memory arrays, preventing read data with a relatively long delay from truncating read data with a relatively short delay, and improving the margin of data transmission. In addition, by separating the data transmission paths of the first memory array 401 and the second memory array 402, in the process of data writing/reading, a transmission direction of data can be determined by determining whether the data belongs to a writing process or a reading process. This avoids the complex data path determining process when the same data transmission path is used, thereby achieving a higher data transmission rate and higher accuracy of data transmission.

[0054] Each unit involved in this embodiment is a logical unit. During actual application, a logical unit may be a physical unit, or may be a part of a physical unit, or may be implemented as a combination of a plurality of physical units. In addition, in order to highlight the innovative part of the present disclosure, units that are not closely related to resolving the technical problem proposed by the present disclosure are not introduced in this embodiment, but this does not indicate that there are no other units in this embodiment.

[0055] It is to be noted that features disclosed in the memory circuit in the above embodiment may be combined freely without conflicts to obtain a new memory circuit.

[0056] Another embodiment of the present disclosure provides a data transmission circuit, to improve the transmission efficiency of read/written data of the memory.

[0057] FIG. 4 is a schematic structural diagram of a data transmission circuit according to this embodiment; FIG. 5 is specific schematic structural diagram of a control module according to this embodiment; FIG. 6 is schematic diagram of a specific connection manner of a data transmission structure according to this embodiment; FIG. 7 is a specific schematic structural diagram of a data transmission structure during data reading according to this embodiment; FIG. 8 is a specific schematic structural diagram of a data transmission structure during data writing according to this embodiment. The following describes the data transmission circuit provided by this embodiment in further detail with reference to the accompanying drawings.

[0058] Referring to FIG. 4, the data transmission circuit is arranged in the data transmission region 100.

[0059] The data transmission circuit includes: at least two data transmission structures 101 and a control module 104. Each data transmission structure is connected to at least one memory circuit provided by the foregoing embodiment, and is configured to read data from the memory circuit and write data into the memory circuit.

[0060] Each data transmission structure includes a memory transmission terminal 111, a bus transmission terminal 112, and an interactive transmission terminal 113. The memory transmission terminal 111 is configured to connect the memory region 102; the bus transmission terminal 112 is configured to connect the data bus 103; the interactive transmission terminal 113 is configured to connect the interactive transmission terminal 113 of another data transmission structure.

[0061] Data inputted from the memory transmission terminal 111 is outputted through the bus transmission terminal 112 or the interactive transmission terminal 113.

Data inputted from the bus transmission terminal 112 is outputted through the memory transmission terminal 111 or the interactive transmission terminal 113. Data inputted from the interactive transmission terminal 113 is outputted through the bus transmission terminal 112 or the memory transmission terminal 111. Data inputted from the interactive transmission terminal 113 is data inputted through the bus transmission terminal 112 or the memory transmission terminal 111 of another data transmission structure 101.

[0062] The control module 104 is connected to the data transmission structure 101 and receives an input control signal and an adjustment control signal provided by the memory that the control module 104 belongs to.

[0063] Referring to FIG. 4 in combination with FIG. 5, the control module 104 is configured to output the input control signal in a delayed manner based on the adjustment control signal, to generate an output control signal corresponding to the input control signal. The input control signal and the output control signal are used for indicating a data transmission path of the data transmission structure 101.

[0064] The adjustment control signal is generated based on the memory that the data transmission circuit belongs to, and is used for controlling a delay between the corresponding input control signal and output control signal.

[0065] The control module 104 controls data transmission paths of two data transmission structures 101, so that different data transmission structures transmit data alternately. Data transmission of different memory regions 102 can be implemented corresponding to the same data transmission structure 101. Through alternate transmission of multiple paths of data, data transmission is more compact, thereby improving the data transmission efficiency of the memory.

[0066] It should be noted that, in other embodiments, the quantity of data transmission structures may be any even number greater than 2. Every two data transmission structures form the foregoing data transmission circuit, thereby further improving the data transmission efficiency of the memory.

[0067] Specifically, a signal delay between the input control signal and the output control signal is controlled by the adjustment control signal, which avoids an output

terminal from turning on earlier than or later than preset timing, ensuring that the data transmission structure outputs the corresponding input data accurately. In some embodiments, referring to FIG. 4 and FIG. 6, the memory transmission terminal 111 includes: a first transmission terminal A, a second transmission terminal B, a third transmission terminal C, and a fourth transmission terminal D; the bus transmission terminal 112 includes: a fifth transmission terminal E and a sixth transmission terminal F; the interactive transmission terminal 113 includes: a seventh transmission terminal G and an eighth transmission terminal H.

[0068] The first transmission terminal A and the second transmission terminal B are connected to a memory region 102 of the memory different from a memory region 102 that the third transmission terminal C and the fourth transmission terminal D are connected to. The first transmission terminal A and the third transmission terminal C are configured to transmit low-bit data; the second transmission terminal B and the fourth transmission terminal D are configured to transmit high-bit data; the fifth transmission terminal E and the sixth transmission terminal F are configured to perform interactive data transmission between the data bus 103 and the data transmission structure 101 that the fifth transmission terminal E and the sixth transmission terminal F belong to; the seventh transmission terminal G and the eighth transmission terminal H are configured to perform interactive data transmission between two data transmission structures 101.

[0069] It should be noted that, the first transmission terminal A and the second transmission terminal B may be configured to transmit high-bit data and low-bit data of the same piece of data. For example, for transmission of 16-bit data, the first transmission terminal A is configured to transmit data of lower 8 bits, and the second transmission terminal B is configured to transmit data of higher 8 bits. The first transmission terminal A and the second transmission terminal B may alternatively be configured to transmit different data. For transmission of 8-bit data, the first transmission terminal A and the second transmission terminal B may be configured to transmit different data.

[0070] Further, in some embodiments, the fifth transmission terminal E is

configured to perform interactive data transmission between the data bus 103 and the data transmission structure 101 that the fifth transmission terminal E belongs to; the sixth transmission terminal F is configured to perform one-way data transmission from the data transmission structure 101, that the sixth transmission terminal F belongs to, to the data bus 103. Through special configuration for the fifth transmission terminal E and the sixth transmission terminal F, during transmission from the data bus 103 to the data transmission structure 101, data can only be inputted through the fifth transmission terminal E. On-die error correction code (ECC) detection for data can be implemented by setting an ECC module on the fifth transmission terminal E, without adding extra circuit layout settings for ECC detection during data transmission using the data transmission circuit.

[0071] In some embodiments, referring to FIG. 5 in combination with FIG. 6, the input control signal includes: Sel A, Sel B, Sel C, Sel D, Sel E, Sel F, Sel G, and Sel H; the output control signal includes: Drv A, Drv B, Drv C, Drv D, Drv E, Drv F, Drv G, and Drv H.

[0072] The first transmission terminal A corresponds to the input control signal Sel A and the output control signal Drv A; the second transmission terminal B corresponds to the input control signal Sel B and the output control signal Drv B; the third transmission terminal C corresponds to the input control signal Sel C and the output control signal Drv C; the fourth transmission terminal D corresponds to the input control signal Sel D and the output control signal Drv D; the fifth transmission terminal E corresponds to the input control signal Sel E and the output control signal Drv E; the sixth transmission terminal F corresponds to the input control signal Sel F and the output control signal Drv F; the seventh transmission terminal G corresponds to the input control signal Sel G and the output control signal Drv G; the eighth transmission terminal H corresponds to the input control signal Sel H and the output control signal Drv H.

[0073] Referring to FIG. 4 and FIG. 6, data inputted from the memory transmission terminal 111 is outputted through the bus transmission terminal 112 or the interactive transmission terminal 113. That is, data read from the first transmission

terminal A, the second transmission terminal B, the third transmission terminal C and the fourth transmission terminal D may be read through the fifth transmission terminal E and the sixth transmission terminal F or read through the seventh transmission terminal G and the eighth transmission terminal H.

[0074] Data inputted from the bus transmission terminal 112 is outputted through the memory transmission terminal 111 or the interactive transmission terminal 113. That is, data written from the fifth transmission terminal E can be written through the first transmission terminal A, the second transmission terminal B, the third transmission terminal C, and the fourth transmission terminal D or through the seventh transmission terminal G and the eighth transmission terminal H.

[0075] Data inputted from the interactive transmission terminal 113 can be outputted through the bus transmission terminal 112 or the memory transmission terminal 111. That is, data inputted from the seventh transmission terminal G and the eighth transmission terminal H can be written through the first transmission terminal A, the second transmission terminal B, the third transmission terminal C, and the fourth transmission terminal D or read through the fifth transmission terminal E and the sixth transmission terminal F.

[0076] Referring to FIG. 7 and FIG. 8, the data transmission structure 101 includes: an input unit 201, an output unit 203, and a latch unit 204. The input unit 201 is configured to receive at least one piece of input data and the input control signal, and output the input data corresponding to the input control signal based on the input control signal.

[0077] The output unit 203 is configured to receive the input data outputted by the input unit 201 and at least one output control signal and output the input data based on a valid port represented by the output control signal.

[0078] The latch unit 204 is connected to the output unit 203 and configured to latch the input data outputted by the output unit 203.

[0079] The input unit 201 includes a plurality of input controllers 211. Each input controller 211 corresponds to the memory transmission terminal 111, the bus transmission terminal 112 or the interactive transmission terminal 113. Each input

controller 211 is configured to correspondingly receive the input data from the memory transmission terminal 111, the bus transmission terminal 112, or the interactive transmission terminal 113 and the input control signal. The input controller 211 is configured to be turned on a corresponding port based on the input control signal, to output the input data of the corresponding port.

[0080] For example, in the case of data reading, referring to FIG. 7, data of the memory region connected to the data transmission structure 101 is read out through the first transmission terminal A, the second transmission terminal B, the third transmission terminal C or the fourth transmission terminal D; alternatively, data of the memory region connected to another data transmission structure 101 may be read out through the seventh transmission terminal G and the eighth transmission terminal H.

[0081] Input data Data A of the first transmission terminal A is connected to an input controller 211, where the input controller is controlled through the input control signal Sel A, and upon reception of the input control signal Sel A, the input data Data A of the first transmission terminal A is outputted. Input data Data B of the second transmission terminal B is connected to an input controller 211, where the input controller is controlled through the input control signal Sel B, and upon reception of the input control signal Sel B, the input data Data B of the second transmission terminal B is outputted. Input data Data C of the third transmission terminal C is connected to an input controller 211, where the input controller is controlled through the input control signal Sel C, and upon reception of the input control signal Sel C, the input data Data C of the third transmission terminal C is outputted. Input data Data D of the fourth transmission terminal D is connected to an input controller 211, where the input controller is controlled through the input control signal Sel D, and upon reception of the input control signal Sel D, the input data Data D of the fourth transmission terminal D is outputted. Input data Data G of the seventh transmission terminal G is connected to an input controller 211, where the input controller is controlled through the input control signal Sel G, and upon reception of the input control signal Sel G, the input data Data G of the seventh transmission terminal G is

outputted. Input data Data H of the eighth transmission terminal H is connected to an input controller 211, where the input controller is controlled through the input control signal Sel H, and upon reception of the input control signal Sel H, the input data Data H of the eighth transmission terminal H is outputted.

[0082] Specifically, in the case of data writing, referring to FIG. 8, data is written into the data transmission structure 101 through the fifth transmission terminal E, or written data received by another data transmission structure 101 is written through the seventh transmission terminal G and the eighth transmission terminal H.

[0083] Input data Data E of the fifth transmission terminal E is connected to an input controller 211, where the input controller is controlled through the input control signal Sel E, and upon reception of the input control signal Sel E, the input data Data E of the fifth transmission terminal E is outputted. Input data Data G of the seventh transmission terminal G is connected to an input controller 211, where the input controller is controlled through the input control signal Sel G, and upon reception of the input control signal Sel G, the input data Data G of the seventh transmission terminal G is outputted. Input data Data H of the eighth transmission terminal H is connected to an input controller 211, where the input controller is controlled through the input control signal Sel H, and upon reception of the input control signal Sel H, the input data Data H of the eighth transmission terminal H is outputted.

[0084] In some embodiments, the data transmission structure further includes a mask unit 202 configured to generate data mask ~~data~~ DM according to the input data Data E of the fifth transmission terminal E. The data mask ~~data~~ DM is inputted through the input controller 211 corresponding to the fifth transmission terminal E, to implement selective input for data on the data bus 103.

[0085] Specifically, the memory includes a data mask function and a data bus inversion function. When the data mask is effective, corresponding 8-bit data is not written; when more than half of bits in the written 8-bit data are 1, the written 8-bit data is inverted if the transmission path 0 consumes less power. When both the data mask (~~Data Mask,~~ DM) function and the ~~data inversion~~data bus inversion (~~databus inversion,~~ DBI) function are enabled, because the data mask signal and the ~~data~~

~~inversion~~data bus inversion signal need to use the same data port, only one of the signals can be inputted. In the present disclosure, the ~~data inversion~~data bus inversion signal is inputted. In other words, during data writing, the input data and the ~~data inversion~~data bus inversion signal are transmitted to the data transmission structure together. When the ~~data inversion~~data bus inversion signal is valid, it indicates that the synchronously inputted input data Data E needs to be inverted. Inversion is unnecessary if the input data Data E does not need to be written. Therefore, the ~~data inversion~~data bus inversion signal being valid also indicates that the input data Data E needs to be written. When the ~~data inversion~~data bus inversion signal is invalid, if the input data is inputted normally more than half of bits of the input data should be 0. In other words, when the ~~data inversion~~data bus inversion signal is invalid, it is necessary to detect whether half of bits or more of the input data are 0; if yes, the data is inputted normally without ~~data inversion~~data bus inversion; if less than half of bits of the input data are 0 and more than half of bits are 1, the input data in this case represents that the data mask signal is valid, and the corresponding 8-bit input data is shielded and not stored into the memory array.

[0086] In other words, when the ~~data inversion~~data bus inversion signal is valid, the fifth transmission terminal E receives the 8-bit original data to be written, and the inverter unit 207 receives the inversion control signal DBI. The inversion control signal DBI in this case represents that a data flipping signal is valid. For example, the inversion control signal DBI is 1, and data inputted from the input unit 201 is flipped to be outputted to the output unit 203. When the ~~data inversion~~data bus inversion signal is invalid, whether the fifth transmission terminal E receives the 8-bit original data to be written or the data mask ~~data~~ DM is determined according to the content of Data E. Specifically, when the ~~data inversion~~data bus inversion signal is invalid, inputted/outputted Data E is encoded/decoded through the mask unit 202, to determine whether the data mask signal is valid (the signal is valid if it is 1, and invalid if it is 0). If the data mask signal~~DM~~ is indicates that the data mask signal is valid, the 8-bit original data does not need to be written. In this case, the fifth transmission terminal E receives the data mask ~~data~~ DM; if the data mask signal~~DM~~

indicates that the data mask signal is invalid, the 8-bit original data needs to be written. In this case, the fifth transmission terminal E receives the input data Data E.

[0087] It should be noted that, any one of the data transmission structures only inverts data inputted through the corresponding fifth transmission terminal E. That is, during data writing, the inversion control signal DBI received by the flip control sub-unit 221 can only be the inversion control signal corresponding to the input data Data E, rather than the inversion control signal corresponding to the input data Data G and Data H. Because Data G and Data H are data inputted through the seventh input terminal Sel G and the eighth input terminal Sel H, that is, data inputted from the data bus 103 through another data transmission structure. In this case, the ~~data inversion~~data bus inversion process of the input data has been finished in the inverter unit 207 of another data transmission structure.

[0088] The output unit 203 includes: a plurality of output controllers 212. Each output controller 212 corresponds to the memory transmission terminal 111, the bus transmission terminal 112 or the interactive transmission terminal 113. Each output controller 212 is configured to corresponding receive the input data from the memory transmission terminal 111, the bus transmission terminal 112 or the interactive transmission terminal 113 and the output control signal. The output controller 212 is configured to be turned on based on the output control signal, to output the input data.

[0089] Specifically, in the case of data reading, referring to FIG. 7, data is read to the data bus 103 through the fifth transmission terminal E or the sixth transmission terminal F; alternatively, data may be read to another data transmission structure 101 through the seventh transmission terminal G and the eighth transmission terminal H, and finally read to another data bus 103 through the fifth transmission terminal E or sixth transmission terminal F corresponding to the other data transmission structure 101.

[0090] The output controller 212 connected to the fifth transmission terminal E is controlled through the output control signal Drv E, and upon reception of the output control signal Drv E, data is outputted through the fifth transmission terminal E. The output controller 212 connected to the seventh transmission terminal G is controlled

through the output control signal Drv G, and upon reception of the output control signal Drv G, data is outputted through the seventh transmission terminal G; the output controller 212 connected to the eighth transmission terminal H is controlled through the output control signal Drv H, and upon reception of the output control signal Drv H, data is outputted through the eighth transmission terminal H.

[0091] Specifically, in the case of data writing, referring to FIG. 8, data is written, through the first transmission terminal A, the second transmission terminal B, the third transmission terminal C or the fourth transmission terminal D, into the memory region connected to the data transmission structure 101, or written, through the seventh transmission terminal G and the eighth transmission terminal H, into the memory region connected to another data transmission structure 101.

[0092] The output controller 212 connected to the first transmission terminal A is controlled through the output control signal Drv A, and upon reception of the output control signal Drv A, data is outputted through the first transmission terminal A. The output controller 212 connected to the second transmission terminal B is controlled through the output control signal Drv B, and upon reception of the output control signal Drv B, data is outputted through the second transmission terminal B. The output controller 212 connected to the third transmission terminal C is controlled through the output control signal Drv C, and upon reception of the output control signal Drv C, the third transmission terminal C is outputted. The output controller 212 connected to the fourth transmission terminal D is controlled through the output control signal Drv D, and upon reception of the output control signal Drv D, data is outputted through the fourth transmission terminal D. The output controller 212 connected to the seventh transmission terminal G is controlled through the output control signal Drv G, and upon reception of the output control signal Drv G, data is outputted through the seventh transmission terminal G. The output controller 212 connected to the eighth transmission terminal H is controlled through the output control signal Drv H, and upon reception of the output control signal Drv H, data is outputted through the eighth transmission terminal H.

[0093] In this embodiment, the latch unit 204 includes a first inverter 214 and a

second inverter 213 connected end to end. An input terminal of the first inverter 214 and an output terminal of the second inverter 213 are connected in parallel with an output terminal of the output unit 203. Through parallel connection between the latch unit 204 and the output terminal of the output unit 203, data outputted by the output unit 203 is stored. It should be noted that, in other embodiments, the latch unit includes a first inverter and a second inverter connected end to end. An input terminal of the first inverter and an output terminal of the second inverter are connected series with an output port of the input unit. Through serial connection between the latch unit and the output terminal of the output unit, so that data outputted by the output unit is latched in an inverted manner, and the data outputted by the output unit is stored subsequently through an inverter connected in series.

[0094] In some embodiments, data input is further delayed, to further ensure the accuracy of data in the multi-path transmission process.

[0095] Specifically, referring to FIG. 7 and FIG. 8, the data transmission structure further includes: an input selection unit 205 and a trigger unit 206.

[0096] The input selection unit 205 is configured to receive at least one input control signal, and generate a strobe corresponding to the input control signal, where the strobe corresponds to a valid port represented by the input control signal, and a selection delay exists between the strobe and the input control signal; and a trigger unit 206 including a clock terminal connected to the input selection unit 205, an input terminal connected to the input unit 201, and an output terminal connected to the output unit 203, and configured to transmit, based on the strobe, the input data received by the input terminal to the output terminal.

[0097] The input selection unit 205 includes: a trigger sub-unit 215 configured to receive at least one input control signal, and generate an indication signal if the input control signal is received; and a delay sub-unit 216, connected to the trigger sub-unit 215 and configured to delay the indication signal; and a conversion sub-unit 217, connected to the delay sub-unit 216 and configured to convert the delayed indication signal into the strobe.

[0098] The delay sub-unit 216 delays the indication signal, to ensure that the data

transmission structure outputs the input data correspondingly. Specific delay parameters of the delay sub-unit 216 are set based on the memory that the delay sub-unit 216 belongs to. In some embodiments, the specific delay parameters of the delay sub-unit 216 can be configured by operators.

[0099] The trigger sub-unit 215 in this embodiment is implemented by an OR gate. During data reading, referring to FIG. 7, the input control signal Sel A, Sel B, Sel C, Sel D, Sel G or Sel H is inputted to the trigger sub-unit 215. The trigger sub-unit 215 generates an indication signal based on an active level of the input control signal Sel A, Sel B, Sel C, Sel D, Sel G or Sel H. After being delayed by the delay sub-unit 216, the indication signal is converted into the strobe by the conversion sub-unit 217, to drive the trigger unit 206. During data writing, referring to FIG. 5, the input control signal Sel E, Sel G or Sel H is inputted to the trigger sub-unit 215. The trigger sub-unit 215 generates an indication signal based on an active level of the input control signal Sel E, Sel G or Sel H. After being delayed by the delay sub-unit 216, the indication signal is converted into the strobe by the conversion sub-unit 217, to drive the trigger unit 206.

[0100] In some embodiments, the trigger unit consists of a D flip-flop.

[0101] In some embodiments, the data transmission structure 101 further includes: an inverter unit 207, disposed between the trigger unit 206 and the input unit 201 and configured to output the input data or invert and output the input data based on an inversion control signal.

[0102] An inversion control signal after data is quantized. The inverter unit directly outputs the data or inverts and outputs the data, to reduce the data energy consumption of the data transmission structure 101. Specifically, since low-level data transmission consumes less energy, low-level data transmission can save energy. If high-level data is more than low-level data after data quantization, the inversion control signal controls the data to be inverted before being transmitted; if high-level data is less than low-level data in the data, the inversion control signal controls the data to be transmitted directly.

[0103] Referring to FIG. 7 and FIG. 8, the inverter unit 207 includes: a flip

control sub-unit 221 configured to receive the inversion control signal, and generate a first control signal and a second control signal based on the inversion control signal; a first selection sub-unit 222 and a second selection sub-unit 223 connected in parallel, wherein an input terminal of the first selection sub-unit 222 and an input terminal of the second selection sub-unit 223 are configured to receive the input data, and an output terminal of the first selection sub-unit 222 and an output terminal of the second selection sub-unit 223 are connected to the trigger unit 206. The first selection sub-unit 222 is configured to be turned on based on the first control signal, and invert and output the input data; the second selection sub-unit 223 is configured to be turned on based on the second control signal, and output the input data directly.

[0104] It should be noted that, the first control signal and the second control signal may be used as two signals to drive the first selection sub-unit 222 and the second selection sub-unit 223, or may be used as a high level and a low level of the same signal to drive the first selection sub-unit 222 and the second selection sub-unit 223.

[0105] Referring to FIG. 7, in some embodiments, the inverter unit 207 further includes: a judging sub-unit 224 configured to receive input data and generate the inversion control signal based on the input data.

[0106] In this embodiment, the control module 104 controls data transmission paths of two data transmission structures 101, so that different data transmission structures transmit data alternately. Data transmission of different memory regions 102 can be implemented corresponding to the same data transmission structure 101. Through alternate transmission of multiple paths of data, data transmission is more compact, thereby improving the data transmission efficiency of the memory.

[0107] It should be noted that, determining whether the signal exists or not is an example of the signal driving method mentioned in this embodiment. In an actual application, driving may be performed depending on whether the signal exists or not or depending on a high level or low level of the signal, that is, in the presence of the signal, driving is performed depending on whether the level of the signal is an active level.

[0108] Each unit involved in this embodiment is a logical unit. During actual application, a logical unit may be a physical unit, or may be a part of a physical unit, or may be implemented as a combination of a plurality of physical units. In addition, in order to highlight the innovative part of the present disclosure, units that are not closely related to resolving the technical problem proposed by the present disclosure are not introduced in this embodiment, but this does not indicate that there are no other units in this embodiment.

[0109] It is to be noted that features disclosed in the data transmission circuit in the above embodiment may be combined freely without conflicts to obtain a new embodiment of the data transmission circuit.

[0110] Another embodiment of the present disclosure provides a memory, which adopts the memory circuit provided by the foregoing embodiment to arrange memory arrays, so as to improve transmission efficiency of read/written data of the memory and ensure accuracy of data transmission.

[0111] In some embodiments, the memory is a DRAM chip provided with memory meeting a DDR2 memory specification.

[0112] In some embodiments, the memory is a DRAM chip provided with memory meeting a DDR3 memory specification.

[0113] In some embodiments, the memory is a DRAM chip provided with memory meeting a DDR4 memory specification.

[0114] In some embodiments, the memory is a DRAM chip provided with memory meeting a DDR5 memory specification.

[0115] Persons skilled in the art should understand that the embodiments of the present disclosure may be provided as a method, an apparatus (device), or a computer program product. Therefore, the present disclosure may use a form of hardware only embodiments, software only embodiments, or embodiments with a combination of software and hardware. Moreover, the present disclosure may be in a form of a computer program product that is implemented on one or more computer-usable storage media that include computer-usable program code. The computer storage media include volatile, non-volatile, removable, and non-removable media

implemented in any method or technology for storing information (such as computer-readable instructions, data structures, program modules, or other data), including but not limited to, a random access memory (RAM), a read-only memory (ROM), an electrically erasable programmable read-only memory (EEPROM), a flash memory or other storage technologies, a compact disc read-only memory (CD-ROM), a digital versatile disk (DVD) or other optical disc storage, a magnetic cassette, a magnetic tape, magnetic disk storage or other magnetic storage apparatuses, or any other medium that can be used to store desired information and can be accessed by a computer. In addition, as is well known to persons of ordinary skill in the art, the communication media usually contain computer-readable instructions, data structures, program modules, or other data in modulated data signals such as carrier waves or other transmission mechanisms, and may include any information transfer medium.

[0116] The present disclosure is described with reference to the flowcharts and/or block diagrams of the method, the apparatus (device), and the computer program product according to the embodiments of the present disclosure. It should be understood that computer program instructions may be used to implement each process and/or each block in the flowcharts and/or the block diagrams and a combination of a process and/or a block in the flowcharts and/or the block diagrams. These computer program instructions may be provided for a general-purpose computer, a dedicated computer, an embedded processor, or a processor of any other programmable data processing device to generate a machine, such that the instructions executed by a computer or a processor of any other programmable data processing device generate an apparatus for implementing a specific function in one or more processes in the flowcharts and/or in one or more blocks in the block diagrams.

[0117] These computer program instructions may be stored in a computer readable memory that can instruct the computer or any other programmable data processing device to work in a specific manner, such that the instructions stored in the computer readable memory generate an artifact that includes an instruction apparatus. The instruction apparatus implements a specific function in one or more processes in the flowcharts and/or in one or more blocks in the block diagrams.

[0118] These computer program instructions may also be loaded onto a computer or another programmable data processing device, such that a series of operations and steps are performed on the computer or the another programmable device, thereby generating computer-implemented processing. Therefore, the instructions executed on the computer or the another programmable device provide steps for implementing a specific function in one or more processes in the flowcharts and/or in one or more blocks in the block diagrams.

[0119] In the specification, the terms "include", "comprise", or any other variations thereof are intended to cover a non-exclusive inclusion, such that an article or a device including a series of elements not only includes those elements, but also includes other elements that are not explicitly listed, or also includes inherent elements of the article or the device. Without more restrictions, the elements defined by the statement "including a ..." do not exclude the existence of other identical elements in the article or device including the elements.

[0120] The preferred embodiments of the present disclosure are described above. However, those skilled in the art can make changes and modifications to these embodiments once they learn the basic inventive concept of the present disclosure. Therefore, the appended claims are intended to be interpreted as including the preferred embodiments and all changes and modifications falling within the scope of the present disclosure.

[0121] Apparently, those skilled in the art can make various modifications and variations to the present disclosure without departing from the spirit and scope of the present disclosure. In this way, if these changes and modifications to the present disclosure fall within the scope of the claims of the present disclosure and equivalent technologies thereof, the present disclosure is further intended to include these changes and modifications.

INDUSTRIAL APPLICABILITY

[0122] The memory circuit provided in the present disclosure can improve the

transmission efficiency of read/written data of the memory and ensure accuracy of data transmission.