

SILICON PHOTONIC INTEGRATED CHIP DEVICE AND FABRICATING METHOD THEREFOR

FIELD OF THE INVENTION

- 5 The disclosures made herein relate generally to the silicon photonics and more particularly to a silicon photonic integrated chip (PIC) device and a fabricating method therefor.

BACKGROUND OF THE INVENTION

- 10 Monolithically integrated photonic circuits are mainly used as optical data links in applications including high performance computing (HPC), inter-device interconnects and optical memory extension (OME). They are also very much useful as input/output means in mobile devices to enable data exchange between the mobile devices and a host device and/or cloud servers at a rapid rate which is
15 not possible with wireless technology or electrical cables.

Due to the compatibility with most of the existing semiconductor fabrication techniques, silicon photonic integrated circuit (PIC) devices are more advantageous in terms of cost of manufacturing and maturity of technology.

- 20 However, silicon PIC devices are prone to damage due to external environmental conditions such as moisture, contamination, scratches, etc. Conventionally, thick bi-layer stacks of silicon dioxide (SiO_2) and silicon nitride (SiN) were used as passivation layers for protecting silicon PIC devices against such environmental conditions.

United States Patent No.: US 10,416,380 B1 discloses a method for forming an integrated photonic device with one or more suspended structures such as optical mode spot size converter and photonic phase shifter. The suspended structure is formed by removing a part of a substrate such that a cavity is formed under the
5 suspended structure. Furthermore, the cavity is sealed by filling the cavity with a dielectric material such as silicon oxide (SiO₂) and silicon oxynitride, so as to prevent or reduce moisture from entering the cavity.

However, sealing the cavity imposes other disadvantages including:

- 10 - higher consumption of dielectric material;
- longer process recipe or too many shorter process recipes;
- additional stress on semiconductor wafer which leads to wafer bowing and breaking, and therefore inappropriate seating of the wafer in a semiconductor equipment;
- 15 - higher optical signal absorption loss; and
- limitations in size of the cavity.

Hence, there is a need for a silicon photonic integrated chip (PIC) device and a fabricating method therefor, wherein the device is capable of resisting moisture
20 without compromising light coupling performance while obviating all the abovementioned drawbacks of the prior art.

SUMMARY OF THE INVENTION

The present invention relates to a silicon photonic integrated chip (PIC) device, comprising a silicon-on-insulator (SOI) substrate, an optical waveguide, suspended edge coupler and a protective film. The substrate serves as a platform
5 on which one or more device components are fabricated. The optical waveguide is disposed on the SOI substrate for guiding light waves. The suspended edge coupler couples the light waves between the waveguide and an optical fiber. The protective film covers an exposed surface of the device.

10 In one aspect of the present invention the suspended edge coupler includes one or more edge facets, lateral cavities and/or trenches, wherein a cross section of an upper surface of the protective film conforms to that of the exposed surface of the device. The protective film is disposed on the device by a plasma enhanced chemical vapor deposition (PECVD) process, wherein a thickness of said
15 protective film is within a range of 10 – 100 nanometers.

The protective film is formed of an electrically insulative composition comprising a silicon nitride and/or silicon oxynitride. One or more electrical contacts are on the exposed surface, wherein the protective film includes an opening for exposing
20 each electrical contact.

A method for fabricating a silicon photonic integrated chip (PIC) device is also disclosed. The method comprises the steps of: disposing an optical waveguide on a silicon-on-insulator (SOI) substrate for guiding light waves, forming one or

more device components on the SOI substrate or the waveguide, forming a suspended edge coupler for coupling the light waves between the waveguide and an optical fiber, and disposing a protective film on an exposed surface of the silicon PIC device.

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The suspended edge coupler is formed with an edge facet, lateral cavity and/or trench, and the protective film is disposed on the exposed surface of the silicon PIC device, such that a cross section of an upper surface of the protective film conforms to that of the exposed surface.

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The protective film is disposed on the silicon PIC device by a plasma enhanced chemical vapor deposition (PECVD) process, wherein a thickness of the protective film is within a range of 10 – 100 nanometers. The protective film is formed of an electrically insulative composition.

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BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

20 In the appended drawings:

Figure 1 shows a cross sectional view of the device, in accordance with an exemplary embodiment of the present invention.

Figure 2 shows a perspective cross sectional view of the device, in accordance with an exemplary embodiment of the present invention.

Figure 3 shows a cross sectional view of the device with electrical contacts, in accordance with an exemplary embodiment of the present invention.

Figure 4 shows a flow diagram of the method for fabricating the device, in accordance with the first embodiment of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

Detailed description of preferred embodiments of the present invention is disclosed herein. It should be understood, however, that the embodiments are merely exemplary of the present invention, which may be embodied in various
10 forms. Therefore, the details disclosed herein are not to be interpreted as limiting, but merely as the basis for the claims and for teaching one skilled in the art of the invention. The numerical data or ranges used in the specification are not to be construed as limiting. The following detailed description of the preferred embodiments will now be described in accordance with the attached drawings,
15 either individually or in combination.

The present invention relates to silicon photonic integrated chip (PIC) device and a fabricating method therefor. The device comprising a protective film covering exposed surfaces of the edge facets, trenches and lateral cavities, such that a cross
20 section of an upper surface of the protective film conforms to that of the exposed surfaces. By this way, the protective film protects the device from moisture without compromising the light coupling performance of the device, while minimizing time and material consumption for fabricating the device. Since the protective film is thinner, a stress experienced by a semiconductor wafer during

fabrication is reduced, and therefore minimizing the chances of wafer bowing. Furthermore, a thinner protective film minimizes absorption loss of an optical signal and allows wider trenches which in turn avoids any lithographic, etching, deposition or wafer cleaning constraints due to narrower trenches.

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Referring to the accompanying drawings, **Figure 1** shows a cross sectional view of the silicon photonic integrated chip (PIC) device, in accordance with an exemplary embodiment of the present invention. The device (10) comprises a silicon-on-insulator (SOI) substrate (11), an optical waveguide (not shown),
 10 suspended edge coupler (12) and a protective film (13). The SOI substrate (11) serves as a platform on which the device (10) is fabricated, wherein one or more device components are fabricated on the SOI substrate (11). Preferably, the device components include any conventional PIC device components. The waveguide is disposed on the SOI substrate (11) for guiding light waves, wherein the suspended
 15 edge coupler (12) couples the light waves between the waveguide and an optical fiber (not shown). Alternatively, the device components are fabricated over the waveguide. The protective film (13) protects the device (10) from any external environmental conditions including moisture, contamination and scratches.

20 The suspended edge coupler (12) includes at least one edge facet (12a), trench (12b) and/or lateral cavity (12c). The protective film (13) covers an exposed surface (14, as in Figure 2) of the edge facet (12a), trench (12b) and/or lateral cavity (12c), such that a cross section of an upper surface (13a) of the protective film (13) conforms to that of the exposed surface (14) of the edge facet (12a),

trench (12b) and/or lateral cavity (12c). The protective film (13) is disposed on the exposed surface (14) by a plasma enhanced chemical vapor deposition (PECVD) process. Preferably, the protective film (13) is formed of an electrically insulative composition comprising silicon nitride and/or silicon oxynitride.

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A plurality of electrical contacts (15, as in Figure 3) is on the exposed surface (14), wherein the protective film (13) includes an opening (13b, as in Figure 3) for exposing each electrical contact (15). In a preferred embodiment, the electrical contacts (15) include bondpads.

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The protective film (13) is etched to form the openings (13b), wherein the protective film (13) is masked to define one or more portions to be etched to form the openings (13b). Preferably, the protective film (13) is etched using any conventional etch recipe including an anisotropic composition. Alternatively, the protective film (13) may also be blanket etched to form the openings (13b) without masking the protective film (13).

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In a preferred embodiment, a thickness of the protective film (13) is within a range of 10 – 100 nanometers. The edge facet (12a), the lateral cavity (12c) or the trench (12b) are formed by etching the edge coupler (12) and/or the SOI substrate (11), such that an angle of a sidewall of the edge facet (12a), and/or the trench (12b) with respect to the SOI substrate (11) is within 87 - 90°. Preferably, the angle of the sidewall is 90°.

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The protective film (13) protects the device (10) from any external environmental conditions without compromising a light coupling performance of the device (10), while minimizing time and material consumption during fabrication of the device (10). Since the protective film (13) is thinner, a stress experienced by the SOI substrate (11) during fabrication of the device (10) is reduced, and therefore minimizing the chances of wafer bowing or breaking. Furthermore, a thinner protective film minimizes absorption loss of an optical signal and allows wider trenches which in turn avoids any lithographic, etching, deposition or wafer cleaning constraints due to narrower trenches.

Figure 4 shows a flow diagram of the method for fabricating the silicon PIC device, in accordance with the first embodiment of the present invention. The method (20) comprises the steps of: disposing an optical waveguide on a silicon-on-insulator (SOI) substrate for guiding light waves (21), forming one or more device components on the SOI substrate or on the waveguide (22), forming a suspended edge coupler for coupling the light waves between the waveguide and an optical fiber (23), and disposing a protective film for protecting the device from any external environmental conditions (24).

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Preferably, the suspended edge coupler is formed with one or more edge facets, lateral cavities and/or trenches, wherein an angle of a sidewall of the edge facet and/or the trench with respect to said substrate is within 87 - 90°. Furthermore, the protective film is disposed on an exposed surface of the edge facets, lateral

cavities and/or trenches, such that a cross section of an upper surface of the protective film conforms to that of the exposed surface. A thickness of the protective film is within a range of 10 – 100 nanometers.

- 5 More preferably, the protective film is disposed on the device by a plasma enhanced chemical vapor deposition (PECVD) process, wherein the protective film is formed of an electrically insulative composition comprising silicon nitride and/or silicon oxynitride.
- 10 Furthermore, one or more electrical contacts such as bondpads, are disposed on the exposed surface and an opening is etched through the protective film for exposing each electrical contact.

- Preferably, the protective film is masked with a photoresist defining one or more
- 15 portions to be etched to form the openings, before the etching step, wherein the protective film is etched using any conventional etch recipe including an anisotropic composition. Alternatively, the protective film is blanket etched without masking the protective film.

- 20 The present invention exhibits better moisture resistance without compromising a light coupling performance, while minimizing time and material consumption during fabrication of the device. Since the protective film is thinner, a stress experienced by the silicon substrate during fabrication of the device, particularly during disposing the protective film, is reduced, and therefore minimizing the

chances of wafer bowing or breaking. Furthermore, a thinner protective film minimizes absorption loss of an optical signal and allows wider trenches which in turn avoids any lithographic, etching, deposition or wafer cleaning constraints due to narrower trenches.

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The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a", "an" and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises",
10 "comprising", "including" and "having" are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

15 The method steps, processes and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed. The use of the expression "at least" or "at least one" suggests the use of one or
20 more elements, as the use may be in one of the embodiments to achieve one or more of the desired objects or results.

CLAIMS.

1. A silicon photonic integrated chip (PIC) device (10), comprising:
 - (a) a silicon-on-insulator, SOI, substrate (11) serving as a platform for fabricating said device (10);
 - (b) at least one optical waveguide disposed on said SOI substrate for guiding light waves, wherein one or more device components are fabricated on said SOI substrate (11) or said optical waveguide;
 - (c) a suspended edge coupler (12) for coupling said light waves between said waveguide and an optical fiber; and
 - (d) at least one protective film (13) protecting the device (10) from one or more external environmental conditions,
 characterized in that:
 - said suspended edge coupler (12) includes at least one edge facet (12a), trench (12b) and/or lateral cavity (12c),
 - said protective film (13) covers an exposed surface of said edge facet (12a), trench (12b) and/or lateral cavity (12c), such that a cross section of said protective film (13) conforms to that of said exposed surface (14) of said edge facet (12a), trench (12b) and/or lateral cavity (12c)
 - said protective film (13) is formed of an electrically insulative composition comprising at least one of silicon nitride and silicon oxynitride, and
 - a thickness of said protective film (13) is within a range of 10 – 100 nanometers.
2. The device (10) as claimed in claim 1, wherein said protective film (13) is disposed on said device (10) by a plasma enhanced chemical vapor deposition (PECVD) process.

3. The device (10) as claimed in claim 1, comprises one or more electrical contacts on said exposed surface (14), wherein said protective film (13) includes an opening for exposing each electrical contact.
- 5 4. The device (10) as claimed in claim 3, wherein said electrical contacts include bondpads.
5. The device (10) as claimed in claim 3, wherein said protective film (13) is etchable to form said opening.
- 10 6. The device (10) as claimed in claim 5, wherein a mask is provided to define one or more portions to be etched to form said opening.
7. The device (10) as claimed in claim 5, wherein an anisotropic composition is provided to facilitate etching of said protective film (13).
- 15 8. The device (10) as claimed in claim 1, wherein said etching is blanket etching.
- 20 9. The device (10) as claimed in claim 1, wherein an angle of a sidewall of said edge facet (12a) and/or said trench (12b) with respect to said SOI substrate (11) is within 87 - 90°.
- 25 10. A method (20) for fabricating a silicon photonic integrated chip (PIC) device, comprising the steps of:
 - (a) disposing at least one optical waveguide on a silicon-on-insulator, SOI, substrate for guiding light waves (21);
 - (b) forming one or more device components on said SOI substrate or said waveguide (22);
 - 30 (c) forming a suspended edge coupler for coupling said light waves between said waveguide and an optical fiber (23); and

(d) disposing at least one protective film for protecting said device from one or more external environmental conditions (24),

characterized in that:

- 5 – said suspended edge coupler is formed with at least one edge facet, lateral cavity and/or trench,
- said protective film is disposed on an exposed surface of said silicon PIC device, such that a cross section of an upper surface of said protective film conforms to that of said exposed surface,
- 10 – said protective film is formed of an electrically insulative composition comprising at least one of silicon nitride and silicon oxynitride, and
- a thickness of said protective film is within a range of 10 – 100 nanometers.

11. The method (20) as claimed in claim 10, wherein said protective film is disposed on said device by a plasma enhanced chemical vapor deposition (PECVD) process.

12. The method (20) as claimed in claim 10, further comprising the steps of: disposing one or more electrical contacts on said exposed surface and etching an opening through said protective film for exposing each electrical contact.

13. The method (20) as claimed in claim 12, further comprising the step of masking said protective film to define one or more portions to be etched to form said opening, before said etching step.

14. The method (20) as claimed in claim 12, wherein said etching step is blanket etching.

15. The method (20) as claimed in claim 10, wherein an angle of a sidewall of said edge facet and/or said trench with respect to said SOI substrate is within 87 - 90°.