determined independently for each of the first device 1108 and the second device 1110 based upon, *inter alia*, the stress transference effect of the third spacer 1500 and/or the offset of a subsequently deposited low resistance electrical contact over the first device source/drain 1124 and the second device source/drain 1126.

[0126] As an exemplary illustration, the third spacer 1500 may include a thickness ranging from about 50 angstroms to about 500 angstroms at its interface with the substrate 1106. However, it is to be understood that the thickness of the third spacer 1500 may include any thickness that is optimized to strategically alter the first stress level of the first device 1108 and the second stress level of the second device 1110.

[0127] Subsequent to forming the third spacer 1500, the remaining portions of the mask layer 1300, of FIG. 14, are removed from over the resistance device 1128. The process techniques used to remove the mask layer 1300 are well known within the art and not repeated herein.

[0128] Notably, the stress inducing layer 1200 remains over the resistance device 1128, thereby preventing/blocking the deposition of a subsequently formed low resistance electrical contact. In at least one embodiment, the portion of the stress inducing layer 1200 remaining over the second region 1104, e.g., formed over the resistance device 1128 and the isolation structure 1130, can include the stress altered form of the interface 1304, of FIG. 13, formed between the second device 1110 and the resistance device 1128 as a stress altered section or boundary 1502.

[0129] Referring now to FIG. 16, therein is shown the structure of FIG. 15 after forming an electrical contact 1600. Subsequent to forming the third spacer 1500, the electrical contact 1600, such as a low resistance silicide or salicide electrical contact, can be formed over the gate 1112 and adjacent the third spacer 1500 (e.g., over a portion of the first device source/drain 1124 and the second device source/drain 1126) of the first device 1108 and the second device 1110. Notably, the stress inducing layer 1200 formed over the resistance device 1128 blocks the deposition of the electrical contact 1600 form being formed over the resistance device 1128.

[0130] In some embodiments, the electrical contact 1600 may include any conducting compound that forms an electrical interface between itself and another material that is thermally stable and provides uniform electrical properties with low resistance. In other embodiments, the electrical contact 1600 may include refractory metal materials such as, tantalum (Ta), cobalt (Co), titanium (Ti), tungsten (W), platinum (Pt), or molybdenum (Mo). In yet other embodiments, the electrical contact 1600 formed over a portion of the first device

source/drain 1124 and the second device source/drain 1126 can be aligned to the third spacer 1500 via a salicide process.

[0131] It will be appreciated by those skilled in the art that the electrical contact 1600 can affect the mobility of carriers (e.g., due to stresses imparted by the electrical contact 1600)

~~What is claimed is:~~

1. An integrated circuit system comprising:

providing a substrate including a first region with a first device and a second device and a second region with a resistance device;

configuring the first device, the second device, and the resistance device to include a first spacer and a second spacer;

forming a stress inducing layer over the first region and the second region;

processing at least a portion of the stress inducing layer formed over the first region to alter the stress within the stress inducing layer; and

forming a third spacer adjacent the second spacer of the first device and the second device from the stress inducing layer.

2. The system as claimed in claim 1 wherein:

providing the first device includes providing an NFET device and providing the second device includes providing a PFET device.

3. The system as claimed in claim 1 wherein:

forming the stress inducing layer includes forming a tensile stressed layer.

4. The system as claimed in claim 1 wherein:

processing at least a portion of the stress inducing layer inlcudes implanting germanium or xenon.

5. The system as claimed in claim 1 wherein:

forming the third spacer creates a first stress level in the first device and a second stress level in the second device, the first stress level differing from the second stress level.

6. An integrated circuit system comprising:

providing a substrate including a first region with a first device and a second device and a second region with a resistance device;

configuring the first device, the second device, and the resistance device to include a first spacer and a second spacer;

forming a stress inducing layer over the first region and the second region;

processing at least a portion of the stress inducing layer formed over the second device to alter the stress within the stress inducing layer; and

forming a third spacer from the stress inducing layer to create a first stress level in the first device and a second stress level in the second device, the first stress level differing from the second stress level.

7. The system as claimed in claim 6 further comprising:

adjusting the thickness of the third spacer adjacent the first device to alter the first stress level within the first device.

8. The system as claimed in claim 6 further comprising:

adjusting the thickness of the third spacer adjacent the second device to alter the second stress level within the second device.

9. The system as claimed in claim 6 further comprising:

configuring the second device to include a punch-through suppresion layer within a second device source/drain.

10. The system as claimed in claim 6 further comprising:

forming an electrical contact adjacent the third spacer of the first device and the second device.

11. An integrated circuit system comprising:

a substrate including a first region with a first device and a second device and a second region with a resistance device;

the first device, the second device, and the resistance device each including a first spacer and a second spacer; and

the first device and the second device further including a third spacer that creates a first stress level in the first device and a second stress level in the second device, the first stress level differing from the second stress level.

12. The system as claimed in claim 11 wherein:

the first device includes an NFET device and the second device includes a PFET device.

13. The system as claimed in claim 11 wherein:

the third spacer of the first device includes a tensile stressed material.

14. The system as claimed in claim 11 wherein:

the third spacer of the second device includes a tensile stressed material relaxed by germanium or xenon.

15. The system as claimed in claim 11 wherein:

the first stress level within the first device can be controlled by the thickness of the third spacer adjacent the first device.

16. The system as claimed in claim 11 wherein:

the second stress level within the second device can be controlled by the thickness of the third spacer adjacent the second device.

17. The system as claimed in claim 11 wherein:

the second device includes a punch-through suppresion layer within a second device source/drain.

18. The system as claimed in claim 17 wherein:

the punch-through suppression layer includes a silicon germanium layer.

19. The system as claimed in claim 11 wherein:

the first stress level includes a tensile stress that is greater than the second stress level.

20. The system as claimed in claim 11 further comprising:

an electrical contact adjacent the third spacer of the first device and the second device.

What is claimed is:

1. A method for manufacturing an integrated circuit system comprising:

providing a substrate including a first region with a first device and a second device and a second region with a resistor device;

configuring each of the first device, the second device, and the resistor device to include a gate, a gate dielectric, a first spacer and a second spacer;

forming a stress inducing layer over the first region and the second region;

processing at least a portion of the stress inducing layer formed over the first region to alter the stress within the stress inducing layer; and

forming a third spacer adjacent the second spacer of the first device and the second device from the stress inducing layer, the stress inducing layer including a portion remaining over the second region with a stress altered boundary between the second device and the resistor device.

2. The method as claimed in claim 1 wherein:

providing the first device includes providing an NFET device and providing the second device includes providing a PFET device.

3. The method as claimed in claim 1 wherein:

forming the stress inducing layer includes forming a tensile stressed layer.

4. The method as claimed in claim 1 wherein:

processing at least a portion of the stress inducing layer includes implanting germanium or xenon.

5. The method as claimed in claim 1 wherein:

forming the third spacer creates a first stress level in the first device and a second stress level in the second device, the first stress level differing from the second stress level.

6. A method for manufacturing an integrated circuit system comprising:

providing a substrate including a first region with a first device and a second device and a second region with a resistor device;

configuring each of the first device, the second device, and the resistor device to include a gate, a gate dielectric, a first spacer and a second spacer;

forming a stress inducing layer over the first region and the second region;

processing at least a portion of the stress inducing layer formed over the second device to alter the stress within the stress inducing layer; and

forming a third spacer from the stress inducing layer to create a first stress level in the first device and a second stress level in the second device, the first stress level differing from the second stress level and a portion of the stress inducing layer remaining over the second region with a stress altered boundary between the second device and the resistor device.

7. The method as claimed in claim 6 wherein:

forming the third spacer to create the first stress level within the first device includes adjusting the thickness of the third spacer adjacent the first device.

8. The method as claimed in claim 6 wherein:

forming the third spacer to create the second stress level within the second device includes adjusting the thickness of the third spacer adjacent the second device.

9. The method as claimed in claim 6 further comprising:

configuring the second device to include a punch-through suppression layer within a second device source/drain.

10. The method as claimed in claim 6 further comprising:

forming an electrical contact adjacent the third spacer of the first device and the second device.