OFFSET CANCELLATION FOR LATCHING IN A MEMORY DEVICE

CROSS REFERENCES

[0001] The present Application for Patent claims priority to PCT Application No. PCT/US2018/042584, by Vimercati, entitled "OFFSET CANCELLATION FOR LATCHING IN A MEMORY DEVICE," filed July 18, 2018, which claims priority to U.S. Patent Application No. 15/655,644 by Vimercati, entitled "Offset Cancellation for Latching in a Memory Device," filed July 20, 2017, each of which is assigned to the assignee hereof, and each of which is expressly incorporated by reference in its entirety herein.

BACKGROUND

[0002] The following relates generally to operating a memory array and more specifically to offset cancellation for latching in memory device.

[0003] Memory devices are widely used to store information in various electronic devices such as computers, wireless communication devices, cameras, digital displays, and the like. Information is stored by programing different states of a memory device. For example, binary devices have two states, often denoted by a logic "1" or a logic "0." In other systems, more than two states may be stored. To access the stored information, a component of the electronic device may read, or sense, the stored state in the memory device. To store information, a component of the electronic device may write, or program, the state in the memory device.

[0004] Various types of memory devices exist, including magnetic hard disks, random access memory (RAM), read only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, phase change memory (PCM), and others. Memory devices may be volatile or non-volatile. Non-volatile memory, e.g., FeRAM, may maintain their stored logic state for extended periods of time even in the absence of an external power source. Volatile memory devices, e.g., DRAM, may lose their stored state over time unless they are periodically refreshed by an external power source. FeRAM may use similar device architectures as volatile memory but may have non-volatile properties due to the use of a ferroelectric capacitor as a storage device. FeRAM devices may thus have improved performance compared to other non-volatile and volatile memory devices.

[0005] Improving memory devices, generally, may include increasing memory cell density, increasing read/write speeds, increasing reliability, increasing data retention,

length that results in a non-negligible capacitance (e.g., on the order of picofarads (pF)). The resulting voltage of digit line 115-a may then be compared to a reference (e.g., a voltage of reference line 225) by sense component 125-a in order to determine the stored logic state in memory cell 105-a. Other sensing processes may be used.

[0035] Sense component 125-a may include various transistors or amplifiers to detect and amplify a difference in signals, which may be referred to as latching. Sense component 125-a may include a sense amplifier that receives and compares the voltage of digit line 115-a and reference line 225, which may be a reference voltage. The sense amplifier output may be driven to the higher (e.g., a positive) or lower (e.g., negative or ground) supply voltage based on the comparison. For instance, if digit line 115-a has a higher voltage than reference line 225, then the sense amplifier output may be driven to a positive supply voltage. In some cases, the sense amplifier may additionally drive digit line 115-a to the supply voltage. Sense component 125-a may then latch the output of the sense amplifier and/or the voltage of digit line 115-a, which may be used to determine the stored state in memory cell 105-a, e.g., logic 1. Alternatively, if digit line 115-a has a lower voltage than reference line 225, the sense amplifier output may be driven to a negative or ground voltage. Sense component 125-a may similarly latch the sense amplifier output to determine the stored state in memory cell 105-a, e.g., logic 0. The latched logic state of memory cell 105-a may then be output, for example, through column decoder 130 as output 135 with reference to FIG. 1.

[0036] To write memory cell 105-a, a voltage may be applied across capacitor 205. Various methods may be used. In one example, selection component 220 may be activated through word line 110-a in order to electrically connect capacitor 205 to digit line 115-a. A voltage may be applied across capacitor 205 by controlling the voltage of cell plate 230 (through plate line 210) and cell bottom 215 (through digit line 115-a). To write a logic 0, cell plate 230 may be taken high, that is, a positive voltage may be applied to plate line 210, and cell bottom 215 may be taken low, e.g., virtually grounding or applying a negative voltage to digit line 115-a. The opposite process is performed to write a logic 1, where cell plate 230 is taken low and cell bottom 215 is taken high.

[0037] Circuit 200 may also include capacitors 235-a, capacitor 235-b and switching component 240. In some cases, sense component 125-a may be coupled to capacitor 235-a and capacitor 235-b. Capacitor 235-a and capacitor 235-b may be coupled to switching component 240. In some cases, the switching component 240 may be or include an nMOS

by controlling the voltage applied at the gate of the switching component. For example, a switching component 415-a (e.g., first switching component) may be activated by applying a signal to the gate of the switching component 415-a and then passing a voltage (which may in some cases be a positive voltage) supplied by voltage source 425-b (e.g., a second voltage source) through the switching component 415-a and a switching component 415-b (e.g., a second switching component) may be activated by applying a signal to the gate of the switching component 415-b and then passing a voltage (which may in some cases be a reference voltage) supplied by the reference voltage component 420-a (e.g., a first reference voltage component) through the switching component 415-b. The voltage supplied by the voltages sources may satisfy the threshold voltage requirements to turn on the respective switching component. In some cases, a controller may coordinate the application of voltages to the switching components in circuit 400.

[0051] Switching component 415 may represent switching component 415-a coupled between voltage source 425-b and capacitor 410-a (e.g., a first capacitor) and capacitor 410-b (e.g., a second capacitor) via node 430-g (e.g., a third node). In some cases, switching component 415-a may be or may include an nmos transistor. In some cases, switching component 415-c (e.g., a third switching component) may be coupled to a reference voltage component 420-b (e.g., a second reference voltage component). In some cases, switching component 415-c may be or include an isolation reference device component. Switching component 415-d (e.g., a fourth switching component) may be coupled to capacitor 410-a via node 430-h (e.g., a first node). In some cases, switching component 415-d may be or include an nmos transistor. Switching component 415-e (e.g., a fifth switching component) may be coupled to the capacitor 410-b via node 430-i (e.g., a second node). In some cases, switching component 415-e may be or include an nmos transistor. Switching component 415-f (e.g., a sixth switching component) may be coupled to transistor 435-a and transistor 435-b. In some cases, switching component 415-f may be or include a pMOS transistor.

[0052] In some cases, one or more voltage sources may be used to control the voltage applied at the gates of the switching components (e.g., the gate of each switching component may be connected, for instance via a wired connection, to a voltage supply). When activated, a switching component may enable the flow of current between two components; when deactivated, the switching component may prevent the flow of current between the two components. Voltage source 425-a may supply a voltage of positive voltage (e.g., 1.6 V) to switching component 415-f. In some examples, voltage source 425-b may supply a positive

[0104] Some examples of the memory array described above may also include a fourth switching component coupled to the first capacitor via the first node, wherein the fourth switching component comprises an nmos transistor. Some examples of the memory array described above may also include a fifth switching component coupled to the second capacitor via the second node, wherein the fifth switching component comprises an nmos transistor.

[0105] Some examples of the memory array described above may also include a sixth switching component coupled to the first transistor and the second transistor, wherein the sixth switching component comprises a pMOS transistor.

[0106] A method of for operating a memory array is described. The method may include activating a first switching component coupled between a second voltage source and a first capacitor and a second capacitor, applying a reference voltage to a sense component after the first switching component is activated, wherein the sense component is coupled to the first capacitor and the second capacitor, deactivating the first switching component after the reference voltage is applied to the sense component, and measuring a voltage offset across both the first capacitor and the second capacitor.

[0107] An apparatus for operating a memory array is described. The apparatus may include means for activating a first switching component coupled between a second voltage source and a first capacitor and a second capacitor, means for applying a reference voltage to a sense component after the first switching component is activated, wherein the sense component is coupled to the first capacitor and the second capacitor, means for deactivating the first switching component after the reference voltage is applied to the sense component, and means for measuring a voltage offset across both the first capacitor and the second capacitor.

[0108] Another apparatus for operating a memory array is described. The apparatus may include a memory cell and a memory controller in electronic communication with the memory cell, wherein the memory cell is operable to activate a first switching component coupled between a second voltage source and a first capacitor and a second capacitor, apply a reference voltage to a sense component after the first switching component is activated, wherein the sense component is coupled to the first capacitor and the second capacitor, deactivate the first switching component after the reference voltage is applied to the sense

CLAIMS

What is claimed is:

1. A device for operating a memory array, comprising: a sense component in electronic communication with the memory array, and a first voltage source, wherein the sense component comprises a first transistor and a second transistor; a first capacitor coupled to the first transistor via a first node; a second capacitor coupled to the second transistor via a second node; a first switching component coupled between a second voltage source and the first capacitor and the second capacitor via a third node; and a sixth switching component coupled to the first transistor and the second transistor, wherein the sixth switching component comprises a pMOS transistor.

2. The device of claim 1, wherein: the first capacitor is positioned between the first node and the third node and the second capacitor is positioned between the second node and the third node.

3. The device of claim 1, further comprising: a first reference voltage component coupled to the first transistor of the sense component, wherein the first reference voltage component comprises a second switching component; and a second reference voltage component coupled to the second transistor of the sense component, wherein the second reference voltage component comprises a third switching component.

4. The device of claim 1, further comprising: a fourth switching component coupled to the first capacitor via the first node, wherein the fourth switching component comprises a nMOS transistor; and a fifth switching component coupled to the second capacitor via the second node, wherein the fifth switching component comprises a nMOS transistor.

5. A system, comprising: a memory array; a controller configured to transfer data to the memory array; and a processor configured to process signals from the controller, wherein the memory array further comprises: a sense component in electronic communication with the memory array, and a first voltage source, wherein the sense component comprises a first transistor and a second transistor; a first capacitor coupled to the first transistor via a first node; a second capacitor coupled to the second transistor via a second node; a first switching component coupled between a second voltage source and the first capacitor and the second capacitor via a third node; and an additional switching component coupled to the first transistor and the second transistor, wherein the additional switching component comprises a pMOS transistor.

6. The system of claim 5, wherein: the first capacitor is positioned between the first node and the third node and the second capacitor is positioned between the second node and the third node.

7. The system of claim 5, further comprising: a first reference voltage component coupled to the first transistor of the sense component, wherein the first reference voltage

component comprises a second switching component; and a second reference voltage component coupled to the second transistor of the sense component, wherein the second reference voltage component comprises a third switching component.

8. A method for operating a memory array, comprising: activating a first switching component coupled between a second voltage source and a first capacitor and a second capacitor; applying a reference voltage to a sense component after the first switching component is activated, wherein the sense component is coupled to the first capacitor and the second capacitor; deactivating the first switching component after the reference voltage is applied to the sense component; and measuring a voltage offset across both the first capacitor and the second capacitor.

9. The method of claim 8, further comprising: reading a logic state from a memory cell in electronic communication with the first capacitor and the second capacitor based at least in part on measuring the voltage offset.

10. The method of claim 8, further comprising: initiating a sensing operation after the first switching component is activated.

11. The method of claim 8, further comprising: activating a second switching component in electronic communication with the memory array; and generating a first signal across a first transistor in response to activating the second switching component.

12. The method of claim 11, further comprising: deactivating the second switching component in electronic communication with the memory array and the sense component after the first signal is generated across the first transistor.

13. The method of claim 8, further comprising: activating a third switching component in electronic communication with a first reference voltage component and the sense component; and generating a second signal across a second transistor in response to activating the third switching component.

14. The method of claim 13, further comprising: deactivating the third switching component in electronic communication with the first reference voltage component and the sense component after the second signal is generated across the second transistor.

15. The method of claim 8, further comprising: activating a fourth switching component and a fifth switching component after activating the first switching component, wherein the fourth switching component is coupled to the first capacitor via a first node and the fifth switching component is coupled to the second capacitor via a second node.

16. The method of claim 15, further comprising: activating a sixth switching component after activating the fourth switching component and the fifth switching component, wherein the sixth switching component is coupled to a first transistor and a second transistor in the

sense component.

17. The method of claim 8, further comprising: measuring a first voltage at a first node that is dependent on a first threshold voltage of a first transistor in the sense component, wherein the first node connects the first capacitor to the first transistor in the sense component, and wherein measuring the voltage offset across both the first capacitor and the second capacitor is based at least in part on measuring the first voltage.

18. The method of claim 8, further comprising: measuring a second voltage at a second node that is dependent on a second threshold voltage of a second transistor, wherein the second node connects the second capacitor to the second transistor in the sense component, and wherein measuring the voltage offset across both the first capacitor and the second capacitor is based at least in part on measuring the second voltage.

19. The method of claim 8, further comprising: reducing a voltage disparity between a first transistor and a second transistor of the sense component by coupling the first capacitor and the second capacitor to the sense component.

20. An apparatus comprising: a ferroelectric memory cell in a memory array; a transistor coupled to the ferroelectric memory cell; and a memory controller in electronic communication with the ferroelectric memory cell, wherein the memory controller is operable to: initiate activation of a first switching component coupled between a second voltage source and a first capacitor and a second capacitor; initiate application of a reference voltage to a sense component after the first switching component is activated, wherein the sense component is coupled to the first capacitor and the second capacitor; initiate deactivation of the first switching component after the reference voltage is applied to the sense component; and initiate measurement of a voltage offset across both the first capacitor and the second capacitor.

21. The apparatus of claim 20, wherein the memory controller is operable to: read a logic state from the ferroelectric memory cell in electronic communication with the first capacitor and the second capacitor based at least in part on measuring the voltage offset.

22. The apparatus of claim 20, wherein the memory controller is operable to: initiate a sensing operation after the first switching component is activated.

23. The apparatus of claim 20, wherein the memory controller is operable to: initiate activation of a second switching component in electronic communication with the memory array; initiate generation of a first signal across a first transistor in response to activating the second switching component; initiate activation of a third switching component in electronic communication with a first reference voltage component and the sense component after a sensing operation is initiated; and initiate generation of a second signal across a second transistor in response to activating the third switching component.

24. The apparatus of claim 23, wherein the memory controller is operable to: initiate deactivation of the second switching component in electronic communication with the memory array and the sense component after generation of the first signal across the first transistor; and initiate deactivation of the third switching component in electronic communication with the first reference voltage component and the sense component after generation of the second signal across the second transistor.