

CLAIMS

1. A method, comprising:

performing a series of process steps on a first plurality of test wafers, each of the first plurality of test wafers forming a plurality of features, wherein a first process step in the series of process steps is performed under a first process condition, wherein the series of process steps includes at least one process step;

performing the series of process steps on a second plurality of test wafers, each of the second plurality of test wafers forming the plurality of features, wherein the first process step is performed under a second process condition;

measuring a first dimension of the plurality of features located on the first plurality of test wafers;

measuring a second dimension of the plurality of features located on the second plurality of test wafers; and

determining a sensitivity factor for the plurality of features relating change in dimension and change in process condition.

2. The method of claim 1, wherein the determining includes:

determining the sensitivity factor based on a difference between the first process condition and the second process condition, and based on a difference between the first dimension and the second dimension.

3. The method of claim 1,

wherein the first process condition is a first temperature of a pedestal configured to support a test wafer, the first process step being an etch process step,

wherein the second process condition is a second temperature of the pedestal.

4. The method of claim 3, wherein the sensitivity factor is a trim sensitivity factor relating a change in dimension of the plurality of features and change in temperature of a pedestal configured to support a test wafer when performing an etch process step as the first process step.

5. The method of claim 1,

wherein the first process condition is a first time period for performing an etch process step as the first process step,

wherein the second process condition is a second time period for performing the trim process step.

6. The method of claim 5, wherein the sensitivity factor is a trim sensitivity factor relating a change in a dimension of the plurality of features and change in time when performing an etch process step as the first process step.
7. The method of claim 1,
wherein the first process condition is a first temperature of a pedestal configured for wafer support, the first process step being a deposition step,
wherein the second process condition is a second temperature of the pedestal.
8. The method of claim 7, wherein the sensitivity factor is a deposition sensitivity factor relating a change in dimension of the plurality of features and change in temperature of a pedestal configured to support a test wafer when performing a deposition process step as the first process step.
9. The method of claim 1,
wherein the first process condition is a first number of cycles of a deposition step that is the first process step,
wherein the second process condition is a second number of cycles of the deposition step.
10. The method of claim 9, wherein the sensitivity factor is a deposition sensitivity factor relating a change in dimension of the plurality of features and change in a number of atomic layer deposition cycles when performing a deposition process step as the first process step.
11. The method of claim 1, wherein the measuring the first dimension includes:
measuring each of the plurality of features on the first plurality of test wafers to determine a plurality of dimensions; and
determining an average of the plurality of dimensions that is the first dimension.
12. The method of claim 11,
wherein each of the plurality of features is measured at an end of the series of process steps,
wherein the series of process steps is a self-aligned double patterning (SADP) process,
wherein the first process step is included in a first patterning of the SADP process.
13. The method of claim 11,
wherein each of the plurality of features is measured at an end of the first process step.
14. The method of claim 1, wherein the measuring the second dimension includes:
measuring each of the plurality of features on the second plurality of test wafers to determine a plurality of dimensions; and

determining an average of the plurality of dimensions that is the second dimension.

15. The method of claim 14,
wherein each of the plurality of features is measured at an end of the series of process steps,

wherein the series of process steps is a self-aligned double patterning (SADP) process,
wherein the first process step is included in a first patterning of the SADP process.

16. The method of claim 14,
wherein each of the plurality of features is measured at an end of the first process step.

17. The method of claim 1, wherein each of the first plurality of test wafers and each of the second plurality of test wafers is a blanket wafer.

18. The method of claim 1, wherein each of the first plurality of test wafers and each of the second plurality of test wafers is a topographic wafer.

19. A method comprising:

performing a series of process steps on a wafer to obtain a plurality of features,
wherein a process step is performed under a process condition;

measuring a dimension of the plurality of features after performing the series of process steps;

determining a difference between the dimension that is measured and a target dimension for the plurality of features;

modifying the process condition for the process step based on the difference and a sensitivity factor for the plurality of features relating change in dimension and change in process condition.

20. The method of claim 19, further comprising:

performing the series of process steps using the process condition that is modified for the process step on another wafer.

21. The method of claim 19, wherein the modifying the process condition includes:

modifying a temperature of a pedestal configured for wafer support, the temperature used when performing the process step that is an etch process step,

wherein the sensitivity factor is a trim sensitivity factor relating a change in dimension of the plurality of features and change in temperature of the pedestal when performing the etch process step.

22. The method of claim 19, wherein the modifying the process condition includes:

modifying a time for performing the process step that is an etch process step,

wherein the sensitivity factor is a trim sensitivity factor relating a change in dimension of the plurality of features and change in time when performing the etch process step.

23. The method of claim 19, wherein the modifying the process condition includes: modifying a temperature of a pedestal configured for wafer support, the temperature used when performing the process step that is a deposition step,

wherein the sensitivity factor is a deposition sensitivity factor relating a change in dimension of the plurality of features and change in temperature of the pedestal when performing the deposition process step.

24. The method of claim 19, wherein the modifying the process condition includes: modifying a number of cycles of a deposition step that is the process step,

wherein the sensitivity factor is a deposition sensitivity factor relating a change in dimension of the plurality of features and change in a number of atomic layer deposition cycles when performing the deposition step.

25. The method of claim 19, wherein the measuring the dimension includes: measuring each of the plurality of features to determine a plurality of dimensions; and determining an average of the plurality of dimensions, the average being the dimension.

26. The method of claim 25, wherein each of the plurality of features is measured at an end of the series of process steps,

wherein the series of process steps is a self-aligned double patterning (SADP) process, wherein the process step is included in a first patterning of the SADP process.

27. A method, comprising: measuring an incoming ADI dimension of a mandrel on a wafer; determining a difference between an incoming ADI dimension and a desired ADI dimension of the mandrel;

modifying a time for performing an etch process step based on the difference and an etch rate of the etch process step to achieve a desired ADT dimension of a core feature based on the incoming ADI dimension, the core feature being formed when performing a first patterning process of a self-aligned double patterning (SADP) process;

receiving a change in a second patterning process of the SADP process; and determining a modified ASD dimension for an oxide layer over the core feature based on the change in the second patterning process; and

determining a number of deposition cycles when performing an atomic layer deposition (ALD) process to achieve the modified ASD dimension based on a deposition rate of the ALD process and the desired ADT dimension of the core feature.

28. The method of claim 27, further comprising:

performing the number of deposition cycles in the ALD process that is performed within the first patterning process.

29. The method of claim 27, wherein the change in the second patterning process is a change in a dry etch process.

30. The method of claim 27, wherein the determining the difference includes:

determining that the incoming ADI dimension is larger than the desired ADI dimension.

31. The method of claim 27, wherein the determining the difference includes:

determining that the incoming ADI dimension is smaller than the desired ADI dimension.

32. The method of claim 27, further comprising:

determining the etch rate based on a sensitivity factor relating a change in ADI dimension and change in time to determine the etch rate.

33. The method of claim 27, further comprising:

determining the deposition rate of the ALD process based on a sensitivity factor relating a change in ASD dimension per deposition cycle.