

DIODE AND ROM OR EEPROM DEVICE
UTILISING SAME

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The present invention relates to a diode and a ROM or EEPROM device utilizing same. More specifically, the present invention relates to a diode which utilizes an amorphous alloy including silicon and fluorine. In this respect, reference is made to U.S. Patent No. 4,217,374 Stanford R. Ovshinsky and Masatsugu Izu entitled: AMORPHOUS SEMICONDUCTORS EQUIVALENT TO CRYSTALLINE SEMICONDUCTORS and U.S. Patent No. 4,226,898 Stanford R. Ovshinsky and Arun Madan, of the same title.

Silicon is the basis of the huge crystalline semiconductor industry and is the material which is utilized in substantially all the commercial integrated circuits now produced. When crystalline semiconductor technology reached a commercial state it became the foundation of the present huge semiconductor device manufacturing industry. This was due to the ability of the scientist to grow substantially defect-free germanium and particularly silicon crystals, and then turn them into extrinsic materials with p-type and n-type conductivity regions therein. This was accomplished by diffusing into such crystalline material parts per million of donor (n) or acceptor (p) dopant materials intro-

duced as substitutional impurities into the substantially pure crystalline materials, to increase their electrical conductivity and to control their being either of a p or n conduction type.

5 The semiconductor fabrication processes for making p-n junction crystals involve extremely complex, time consuming, and expensive procedures as well as high processing temperatures. Thus, these crystalline materials used in rectifying and
10 other current control devices are produced under very carefully controlled conditions by growing individual single silicon or germanium crystals, and where p-n junctions are required, by doping such single crystals with extremely small and critical
15 amounts of dopants. These crystal growing processes produce relatively small crystal wafers upon which the integrated memory circuits are formed.

20 In wafer scale integration technology the small area crystal wafer limits the overall size of the integrated circuits which can be formed thereon. In applications requiring large scale areas, such as in the display technology, the crystal wafers can not be manufactured with as large areas

as required or desired. The devices are formed, at least in part, by diffusing p or n-type dopants into the substrate. Further, each device is formed between isolation channels which are diffused into the substrate. Packing density (the number of devices per unit area of wafer surface) is also limited on the silicon wafers, because of the leakage current in each device and the power necessary to operate the devices, each of which generate heat which is undesirable. The silicon wafers do not readily dissipate heat. Also, the leakage current adversely affects the battery or power cell lifetime in portable applications.

Further, the packing density is extremely important because the cell size is exponentially related to the cost of each device. For instance, a decrease in die size by a factor of two results in a decrease in cost on the order of a factor of six. A conventional crystalline ROM utilizing two micron lithography has a bipolar cell size of about .3 to .5 mil² or a MOS cell size of about .2 to .3 mil².

In summary, crystal silicon rectifiers and integrated circuit parameters are not variable as

desired, require large amounts of material, high processing temperatures, are only producible only on relatively small area wafers and are expensive and time consuming to produce. Devices based upon
5 amorphous silicon can eliminate these crystal silicon disadvantages. Amorphous silicon can be made faster, easier, at lower temperatures and in larger areas than can crystal silicon.

Accordingly, a considerable effort has been
10 made to develop processes for readily depositing amorphous semiconductor alloys or films each of which can encompass relatively large areas, if desired, limited only by the size of the deposition equipment, and which could be doped to form p-type
15 and n-type materials to form p-n junction rectifiers and devices superior in cost and/or operation to those produced by their crystalline counterparts. For many years such work was substantially unproductive. Amorphous silicon or germanium (Group IV) films are normally four-fold
20 coordinated and were found to have microvoids and dangling bonds and other defects which produce a high density of localized states in the energy gap thereof. The presence of a high density of local-

ized states in the energy gap of amorphous silicon semiconductor films resulted in such films not being successfully doped or otherwise modified to shift the Fermi level close to the conduction or valence bands making them unsuitable for making p-n junction rectifiers and other current control device applications.

In an attempt to minimize the aforementioned problems involved with amorphous silicon and germanium, W.E. Spear and P. G. Le Comber of Carnegie Laboratory of Physics, University of Dundee, in Dundee, Scotland did some work on "Substitutional Doping of Amorphous Silicon", as reported in a paper published in Solid State Communications, Vol. 17, pp. 1193-1196, 1975, toward the end of reducing the localized states in the energy gap in amorphous silicon or germanium to make the same approximate more closely intrinsic crystalline silicon or germanium and of substitutionally doping the amorphous materials with suitable classic dopants, as in doping crystalline materials, to make them extrinsic and of p or n conduction types.

The reduction of the localized states was accomplished by glow discharge deposition of amor-

phous silicon films wherein a gas of silane (SiH_4) was passed through a reaction tube where the gas was decomposed by an r.f. glow discharge and deposited on a substrate at a substrate temperature of about 500-600°K (227-327°C). The material so deposited on the substrate was an intrinsic amorphous material consisting of silicon and hydrogen. To produce a doped amorphous material a gas of phosphine (PH_3) for n-type conduction or a gas of diborane (B_2H_6) for p-type conduction were premixed with the silane gas and passed through the glow discharge reaction tube under the same operating conditions. The gaseous concentration of the dopants used was between about 5×10^{-6} and 10^{-2} parts per volume. The material so deposited included supposedly substitutional phosphorus or boron dopant and was shown to be extrinsic and of n or p conduction type.

While it was not known by these researchers, it is now known by the work of others that the hydrogen in the silane combines at an optimum temperature with many of the dangling bonds of the silicon during the glow discharge deposition, to substantially reduce the density of the localized

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states in the energy gap toward the end of making the electronic properties of the amorphous material approximate more nearly those of the corresponding crystalline material.

5 D.I. Jones, W.E. Spear, P.G. LeComber, S. Li, and R. Martins also worked on preparing a-Ge:H from GeH_4 using similar deposition techniques. The material obtained gave evidence of a high density of localized states in the energy gap thereof.

10 Although the material could be doped the efficiency was substantially reduced from that obtainable with a-Si:H. In this work reported in Philosophical Magazine B, Vol. 39, p. 147 (1979) the authors conclude that because of the large density of gap states the
15 material obtained is". . . a less attractive material than a-Si for doping experiments and possible applications."

The incorporation of hydrogen in the above silane method not only has limitations based upon
20 the fixed ratio of hydrogen to silicon in silane, but, most importantly, various Si:H bonding configurations introduce new antibonding states which can have deleterious consequences in these materials. Therefore, there are basic limitations in

reducing the density of localized states in these materials which are particularly harmful in terms of effective p as well as n doping. The resulting density of states of the silane deposited materials leads to a narrow depletion width which in turn limits the efficiencies of devices whose operation depends on the drift of free carriers. The method of making these materials by the use of only silicon and hydrogen also results in a high density of surface states which affects all the above parameters.

After the development of the glow discharge deposition of silicon from silane gas was carried out, work was done on the sputter deposition of amorphous silicon films in the atmosphere of a mixture of argon (required by the sputtering deposition process) and molecular hydrogen, to determine the results of such molecular hydrogen on the characteristics of the deposited amorphous silicon film. This research indicated that the hydrogen acted as a compensating agent which bonded in such a way as to reduce the localized states in the energy gap. However, the degree to which the localized states in the energy gap were reduced in

the sputter deposition process was much less than that achieved by the silane deposition process described above. The above described p and n dopant materials also were introduced in the sputtering process to produce p and n doped materials. These materials had a lower doping efficiency than the materials produced in the glow discharge process. Neither process produced efficient p-doped materials with sufficiently high acceptor concentrations for producing commercial p-n junction devices. The n-doping efficiency was below desirable acceptable commercial levels and the p-doping was particularly undesirable since it increased the number of localized states in the band gap.

Heretofore various semiconductor materials, both crystalline and amorphous, have been proposed for utilization in rectifying type devices such as a diode. Also it has been proposed to make a semiconductor or a photoconductive rectifier utilizing an amorphous alloy including silicon and fluoride. U.S. Patent No. 4,217,374, issued August 12, 1980 for Amorphous Semiconductor Equivalent to Crystalline Semiconductor, Stanford R. Ovshinsky and Masatsugu Izu and U.S. Patent No. 4,226,898, issued

October 7, 1980 of the same title, Stanford R. Ovshinsky and Arun Madan.

The present invention provides a diode array including diode means at each cross over point of a
5 conductor of a first group of conductors extending in a first direction over a conductor of a second group of conductors extending in a second direction traversing the first direction, the first group of conductors being insulated from the second group of conductors,
10 and each diode means being coupled to and between a pair of crossing over conductors at one of the cross over points, said diode means including a diode having at least a first region and a second region said regions abutting each other to form a junction there-
15 between and said first region being made of amorphous alloy comprising silicon and hydrogen and/or fluorine.

The present invention further provides a ROM device including open or closed memory circuit means at each circuit cross over point of a conductor of a
20 first group of conductors extending in a first direction over a conductor of a second group of conductors extending in a second direction traversing the first direction, the first group of conductors being insulated from the second group of conductors, and each memory
25 circuit means being coupled to and between a pair of

crossing over conductors at one of the cross over points
and including rectifying means, said rectifying means
including a diode having at least a first region and
a second region, said regions abutting each other to
5 form a junction therebetween and said first region
being made of amorphous alloy.

The present invention further provides an EEPROM
device having memory circuit means at each cross over
point of a conductor of a first group of conductors
10 extending in a first direction over a conductor of a
second group of conductors extending in a second
direction traversing the first direction, the first
group of conductors being insulated from the second
group of conductors, each memory circuit means being
15 coupled to and between a pair of crossing over
conductors at one of the cross over points and including
rectifying means, said rectifying means comprising a
diode having at least a first region and a second
region said regions abutting each other to form a
20 junction therebetween and said first region being
made of an amorphous alloy.

As will be described in greater detail hereinafter,
the diode of the present invention may contain the
amorphous alloy including silicon and fluorine disclosed
25 in the applications identified above in a specific

construction of a diode having at least two regions with at least one region containing the amorphous alloy in combination with ROM or EEPROM device constructions.

A typical ROM device may include a matrix of X and Y axis conductors which are insulated from each other and which have a memory circuit at and coupled between each cross over of an X axis conductor over a Y axis conductor. Each memory circuit may include a memory region and an isolating device such as a transistor or a diode. Typically, such transistors and diodes have been formed in semiconductor substrates with permanently open contact points or permanently closed contact points for establishing logic 1 or logic 0 bits of information which are stored in the ROM device. Such a ROM device may be programmed during the manufacture thereof.

EEPROM (electrically erasible programmable read only memory) devices have been proposed wherein a vertically disposed memory region or cell in the memory circuit is vertically coupled at and between an upper X axis conductor and a lower Y axis conductor in a memory matrix. These devices follow from the storing of information with phase change switch devices first invented by Stanford R. Ovshinsky, as for example, disclosed in U.S. Patent 3,271,591.

Preferably, the amorphous alloy also contains hydrogen and such amorphous alloy is $a\text{-Si}_a\text{F}_b\text{H}_c$, where a is between 80 and 98 atomic percent, b is between 0 and 10 atomic percent and c is between 0 and 10 atomic percent.

The first alloy region may be doped with an N dopant material chosen from an element of Group V of the Periodic Table, e.g., phosphorous, arsenic or others by an amount constituting between a few parts per million (ppm) and five atomic percent and preferably between 10 to 1000 parts per million.

The second region can be a metal, metal alloy, a metallic like material having a high barrier height on the first region so as to create a Schottky barrier.

Alternately, the second region also can be an amorphous alloy including silicon and fluorine and preferably also containing hydrogen. The second alloy region may be doped with a P dopant material chosen from an element of Group III of the Periodic Table, e.g. boron, aluminum or others by an amount constituting between a few parts per million and five atomic percent, and preferably between 10 and 1000 parts per million. Also, the first region could be a P type region with the second region being an N type region.

The packing density utilizing two micron lithography for reference in the thin film ROM and all thin film EEPROM may be of the order of $.1 \text{ mil}^2$ per cell. Further, due to the all thin film deposited structure and the low leakage current the devices can be stacked upon one another to further decrease the packing density. The devices can be formed on various substrates including insulated metal which is utilized as a heat sink for the devices.

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The preferred embodiments of this invention
5 will now be described, by way of example, with
reference to the drawings accompanying this speci-
fication in which:

Fig. 1 is a fragmentary plan view of the de-
posited film side of a substrate which forms a
10 support for an all deposited film ROM device in-
cluding a diode made in accordance with the teach-
ings of the present invention.

Fig. 2 is a sectional view through the memory
circuits of the ROM device shown in Fig. 1 and is
15 taken along line 2-2 of Fig. 1.

Fig. 3 is a schematic circuit diagram of the
memory circuit shown in Fig. 2.

Fig. 4 is a fragmentary plan view of the de-
posited film side of a substrate forming a support
20 for an all deposited thin film EEPROM device in-
cluding memory circuits, each of which include a
diode constructed according to the teachings of the
present invention.

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Fig. 5 is a sectional view through two memory circuits shown in Fig. 4 and is taken along line 5-5 of Fig. 4.

Fig. 6 is a schematic circuit diagram of the memory circuit shown in Fig. 5.

Fig. 7 is a sectional view through a second embodiment of deposited thin film ROM device including a Schottky diode device made in accordance with the teachings of the present invention.

10 Fig. 8 is a schematic circuit diagram of the memory circuit shown in Fig. 7.

Referring to Figs. 1 and 2 there is illustrated therein a ROM device 10 including two dedicated memory circuits 11 and 12 each of which includes a thin film diode or rectifying device 14 (Fig. 2) constructed in accordance with the teachings of the present invention. The memory circuit 11 is a closed circuit which includes the diode 14 which is coupled through an ohmic contact region such as a platinum silicide region 16 to an upper X axis conductor 18 and to a lower Y axis conductor 20.

The memory circuit 12 also includes a diode 14 which is connected on one side to another Y axis

conductor 20' and on the other side is open circuited by reason of a region of insulating material 21 disposed between the upper surface of diode 14 and the X axis conductor 18 as will be described in greater detail below.

In the construction of the ROM device 10, there is deposited on any suitable substrate 22 having an insulating top surface 25, parallel conductors 20 and 20' which form the Y axis conductors and which form a compatible interface with the diode 14. The conductors or bands 20 of conductive material may be made of aluminum, chromium, molybdenum, an alloy of titanium and tungsten (Ti-W) or the like. Also, the conductive bands 20 may include a bottom layer 23 of a highly conductive material like aluminum and an upper layer 24 of a refractory barrier-forming material like molybdenum or Ti-W. The conductive layers 23 and 24 may be formed by conventional vacuum deposition, photo resist masking and etchant techniques.

Next, spaced layers 26 and 28 of amorphous semiconductor alloy including silicon and fluorine are deposited over the conductor bands 20 to form the thin film diodes 14 at each cross over point in

the matrix of X and Y axis conductors 18 and 20 in the ROM device 10. Each such P-N junction diode 14 may be formed from doped N+ and P+ amorphous alloy layers 26 and 28 as shown.

- 5 An insulating layer 30, such as silicon dioxide, is applied over the entire substrate 22 so as to form the insulating region 21 above the diode 14 in the memory circuit 12. However, wherever it is desired to store a data bit which will be indicated
10 by a low resistance condition coupled through the diode 14, an opening 31 is formed in the insulating layer of silicon dioxide.

- 15 The platinum silicide or ohmic contact region 16 can be formed on the outermost amorphous silicon layer 28, where the opening 31 had been formed in the insulating layer 30, such as by applying platinum over the exposed portions of the amorphous alloy layer 28. The rectifier diodes 14 then can have a conductor band 32 formed thereover of a
20 barrier-forming material such as molybdenum or the Ti-W alloy. Subsequently, a band of aluminum is deposited over the conductor band 32 to form the X axis conductor 18. Alternately, the conductor 18 can be deposited over the layer 28 and the in-
25 sulator 30 without the barrier 32.

From the foregoing description, it will be seen that the memory region of each memory circuit 11 and 12 is a predetermined conductive path or a predetermined insulator path between the Y axis conductor 20 through the diode 14 to the X axis conductor 18.

Also, it will be apparent that the memory regions are formed by depositing a thin film of insulating material 30 on one region 28 of each diode 14 followed by depositing a thin film band (band 32 and/or 18) of conductive material to form the X axis conductor 18. For a conductive path memory region, the insulating film layer 30 is cut or etched away such as at 31 in the area above the one region 28 of a selected diode 14 before the thin film conductive band is deposited so that the conductive path is a direct contact of the conductive band 18 with the first region 28 of the selected diode 14.

Also, it is apparent, that each memory circuit 11 or 12 coupled to and between a pair of crossing over conductors 18 and 20 includes not only a conductive path or insulator path memory region but also the diode 14 having a first region 26 and a

second region 28 which abut each other to form a junction therebetween and with at least the first region 26 being made of the amorphous alloy including silicon and fluorine. In the illustrated embodiment in Fig. 2 the second region 28 is also formed of amorphous alloy including silicon and fluorine.

Also, in each memory circuit 11 and 12, the memory region is aligned with the regions 26 and 28 of the diode 14 and all of the regions are juxtaposed and are situated on a line substantially perpendicular to, and extending between each pair of cross-over conductors 18 and 20 at the cross-over thereof to provide a very small center-to-center distance between adjacent memory circuits 11 and 12 thereby to provide a very high packing density of memory circuits 11 and 12 in the ROM device 10 on the order of .1 mil².

In accordance with the teachings of the present invention, the amorphous alloy including silicon and fluorine also preferably contains hydrogen and is preferably an $a\text{-Si}_a\text{:F}_b\text{:H}_c$ alloy, where a is between 80 and 98 atomic percent, b is between 0 and 10 atomic percent and c is between 0 and 10

atomic percent.

The alloy layers 26 and 28 can be between 500 and 20,000 angstroms, one thickness utilized being 1000 angstroms.

5 The first region or layer 26 can be doped with an N type dopant material chosen from an element of Group V of the Periodic Table such as phosphorous or arsenic in an amount between a few parts per million and 5 atomic percent and preferably in an
10 amount constituting 10 to 1000 parts per million. Alternatively, the first region 26 can be doped with a P type dopant material chosen from an element of Group III of the Periodic Table such as boron or aluminum in an amount constituting between
15 a few parts per million and 5 atomic percent and is preferably doped in an amount constituting 10 to 1000 parts per million.

 Alternatively, the second region 28 can be a metal, a metal alloy or a metallic like material
20 having a high barrier height on the first region 26 so as to create a Schottky barrier. There also can be an insulator layer forming an MIS (metal insulator semiconductor) interface.

Further, as another alternative, the second region 28 can be doped with a material chosen from an element of Group III of the Periodic Table or with an element of Group V of the Periodic Table.

5 Still further, one of the regions could be made of a material dissimilar to the amorphous alloy such as to form a heterojunction rectifying device.

In any event, with the thin film diode 14 having at least one region made of the amorphous alloy included in the memory circuit 11 a ROM device 10 is provided which has a low resistance and high conductivity in the forward biased direction and a very high resistance in the reverse biased direction.

15 A schematic circuit diagram of the closed memory circuit 11 and the open memory circuit 12 is shown in Fig. 3 of the drawing.

Referring now to Figs. 4 and 5, there is illustrated therein an EEPROM device 50 and more specifically, two memory circuits 52 thereof which are made in accordance with the teachings of the present invention. As shown, each memory circuit 20 52 includes a memory region 56 made of a reversible resettable memory material as will be described in

more detail hereafter connected in series with a thin film diode 58 between an upper X axis conductor 60 and lower Y axis conductors 62 and 62'.

Referring to Fig. 5, it will be readily apparent that the memory region 56 and the diode 58 are juxtaposed to each other on a line substantially perpendicular to the crossing over conductors 60 and 62 such that the memory circuit 52 formed by each of the memory region 56 and diode 58 have a minimum cell area thereby to provide a maximum packing density of memory cells or memory circuits 56 in the EEPROM device 50.

In the construction of the EEPROM device 50, a substrate 64 such as a metal substrate is provided on which a layer of insulating material 66 is deposited such as by thin film depositing technique. Then parallel bands of conductive material such as metal are laid down to form the Y axis conductors 62.

In accordance with the teachings of the present invention, the P-N junction diode 58 is made of layers of amorphous alloy conductive film 68 and 70 deposited on top of the Y axis conductor bands 60. The isolating diode 58 is formed from success-

fully doped N+ and P+ layers or regions 68 and 70 of amorphous alloy. After these layers have been deposited a layer 72 of insulating material such as silicon dioxide material is deposited over the substrate 66 and the layers 62, 68 and 70 thereon.

Next, an open space 74 is cut or etched out of the layer of insulating material in the area above the upper layer 70 of the diode 58. Preferably, a platinum silicide or ohmic contact region 76 is formed in the upper layer 70 which is exposed through the opening 74 in the manner described above for forming region 16 in ROM device 10.

Then, a thin film of phase change reversible amorphous material is deposited to form memory region 56. Next a thin layer 80 of refractory barrier-forming material like molybdenum or a Ti-W alloy is deposited on the insulating layer 72 and over the memory region 56. Next, a thicker layer 60 of conductive material such as aluminum is deposited in a band over the refractory barrier-forming layer 80 to form the X axis conductor 60. The platinum silicide region 76 can form an ohmic contact or a Schottky barrier interface with the doped outer layer 70.

As provided in the construction of the ROM device 10 described above and in accordance with the teachings of the present invention, the diode 58 has at least the first region or layer 68 and a second region or layer 70 which abut each other to form a junction therebetween with the first region 68 being made of the amorphous alloy.

The second region or layer 70 can also be made of the amorphous alloy and which can be doped with a different dopant material than the material with which the layer 68 is doped. Alternatively, region 70 could be made of a metal, a metal alloy or a metallic like material having a high barrier height on the first region 68 so as to create a Schottky barrier, when the first region 68 is doped with a dopant material chosen from an element of Group V of the Periodic Table. Such a metal can be from the group consisting of gold, platinum, palladium or chromium.

Also, the second region 70 can be made of a material dissimilar to the amorphous material of the first region 68 such as to form a heterojunction. The first region can be N or P doped and the second region can be P or N doped.

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A preferred amorphous alloy is $a\text{-Si}_a\text{:Fb:H}_c$, wherein a is between 80 and 98 atomic percent, b is between 0 and 10 atomic percent and c is between 0 and 10 atomic percent. The dopant material also

5 can be chosen from elements of Group V of the Periodic Table such as phosphorus or arsenic and can constitute between a few parts per million and 5 atomic percent of the region 68 or 70 and preferably 10 to 1000 parts per million.

10 The second region or layer 70 can then be the amorphous alloy as is the first region 68. Then, such material can be doped with a dopant material chosen from an element of Group III of the Periodic Table and can constitute between a few parts per

15 million and 5 atomic percent of the region 70. Such a dopant material can be boron or aluminum and constitute 10 to 1000 parts per million of the region 70. It will be apparent, of course that the doping of the regions 68 and 70 can be reversed if

20 desired. Also, in accordance with the teachings of the present invention, the regions are laid down as deposited thin films.

The memory regions 56 are aligned with the regions 68 and 70 of the diode 58 and all of these

regions are juxtaposed and situated on a line substantially perpendicular to and extending between a pair of cross-over conductors 60 and 62 at a cross-over thereof to provide a very small center-to-center distance between adjacent memory circuits 52 thereby to provide a very high packing density of such memory circuits 52 in the EEPROM device 50. Also, both the memory region and the diode region are thin film depositions.

10 Further, the memory regions 56 comprise a reversible, phase change material which can be set in a highly conductive state or a highly non-conductive state. More specifically, the memory region 56 is formed of a material which is initially
15 amorphous and which can be changed by a set voltage and current to a crystalline conductive state and then reset by a reset voltage and current to an amorphous insulator state. One preferred material from which memory region 56 can be made includes
20 germanium and tellurium such as $\text{Ge}_{20}\text{Te}_{80}$. This material has a good reversibility of up to 10^6 cycles, a maximum processing temperature of approximately 200°C , a maximum storage temperature of 100°C , a threshold voltage of 8 volts, a SET resis-

tance of 300 ohms and OFF resistance (at 175°C) of approximately 10^4 ohms.

The memory region can comprise a memory structure situated between one of the conductors 60 and 62 and one region 68 or 70 of the diode 58 with the memory structure comprising first, second and third regions. The first region is adjacent to the one conductor 60 or 62 or to the one region 70 or 68, whichever is adapted to be coupled to a positive voltage source.

The second region is situated between the first and third regions and the third region is adjacent the one region 70 or 68 or the one conductor 62 or 60, whichever is adapted to be coupled to a negative line of the voltage source and completely separates the second region from the connection to the negative line.

The second region is formed of a tellurium based chalcogenide which has higher electrical resistance in its amorphous state and lower electrical resistance in its crystalline state and can be switched from one state to another upon application to the conductors of an electrical signal of appropriate value.

The first region is formed of a material having a higher percentage of tellurium than the second region. The third region is formed of a material having between 25 and 46 atomic percent germanium with the remaining material being substantially tellurium.

Preferably, the third region contains approximately 33 atomic percent germanium and the second region can contain between 10 and 25 atomic percent germanium and preferably between 15 and 17 percent germanium.

Also, preferably, the first region contains at least 90 atomic percent tellurium.

A schematic circuit diagram of the EEPROM memory circuits 52 is illustrated in Fig. 6 of the drawing.

Fig. 7 illustrates a ROM device 100 similar to that illustrated in Fig. 2 with a Schottky barrier rectifying device in a closed cell 102. An open cell 104 can be formed substantially identical to the cell 12 except for the diode 14 as shown in Fig. 8. The device 100 is formed on a substrate 106 which has an insulating layer 108 formed thereon. Bottom or Y axis conductors 110 are formed on

the layer 108 as before described.

Referring to the cell 102, a heavily doped amorphous alloy contact layer 112 is formed on the conductor 110. An intrinsic or slightly doped alloy layer 114 of the same conductivity type is
5 formed on the layer 112.

An insulator layer 116 is then formed over the cells 102 and 104 with an opening 118 etched or cut through the layer 116 for each closed cell 102. A
10 Schottky barrier 120 is then formed on the alloy 114, such as the barrier 16 described in Fig. 2. A top X axis conductor 122 is formed over the cells 102 and 104 as previously described. The Schottky barrier 120 then forms the cell rectifying device
15 instead of the P-N junction described in Figs. 2 or 5.

A schematic circuit diagram of the ROM closed cell 102 and open cell 104 is illustrated in Fig. 8 of the drawing. The open cell 104 does not have a
20 rectifying device 120 since the insulating material 116 is deposited on the alloy layers.

Both the ROM device 10 and the EEPROM device 50 can be deposited on an insulating layer of material which has first been deposited on a metal

substrate, which metal substrate can form a heat sink and facilitate stacking and heat dissipation of one ROM device on top of another ROM device or an EEPROM device on top of another EEPROM device.

5 Also, if desired, the edges of the metal substrate or substrates can have a heat radiating fin formation thereon for further facilitating heat dissipation.

Of course, metal substrates are not essential
10 and the ROM device 10 or EEPROM device 50 utilizing same have a number of advantages, some of which have been described above and others of which are inherent in the invention. Such diodes and memory regions that form memory circuits in a ROM or EEPROM
15 device can be easily deposited by thin film deposition techniques on a substrate and the devices can be stacked to make a three dimensional memory system. Also, a diode made of two regions of this material, one N doped and one P doped, has a low
20 forward bias resistance and a high reverse bias resistance.

The diode takes up a minimum of space in that it is made by thin film deposition techniques with the amorphous alloy. Such a diode in combination

with a memory region in a ROM device or an EEPROM device takes up a very small space such that the memory circuit or memory cell density can be as low as 0.1 mil^2 with a center-to-center distance between adjacent memory cells or circuits of 8 microns utilizing two micron lithography. In conventional bipolar ROM's, each cell is isolated between a pair of junction diffusion channels. Material to be diffused is deposited two microns wide, but the high temperature process diffuses the material into the substrate. As a result the channels are from four to six microns wide, have a rectifier width of about two microns with six to eight microns allowed between the channels and the rectifier. This results in a bipolar ROM center-to-center distance of about eighteen microns and a cell density of about $.5 \text{ mil}^2$.

Utilizing oxide isolation the rectifiers can be formed, in a best case, adjacent or overlapping the channel's; however, the channels are eight to ten microns wide. This results in a center-to-center distance of about twelve microns and a best cell density of about $.25 \text{ mil}^2$.

The decrease in cell density from .25 mil² to .1 mil² is a very significant cost reduction. Although the conventional junction and oxide isolation ROM's can be reduced in size as photolithography techniques are improved, the corresponding reduction will also take place in the ROM's and EEPROM's utilizing the thin film diode of the invention.

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CLAIMS:

1. A diode array including diode means at each cross over point of a conductor of a first group of conductors extending in a first direction over a conductor of a second group of conductors extending in a second direction traversing the first direction, the first group of conductors being insulated from the second group of conductors, and each diode means being coupled to and between a pair of crossing over conductors at one of the cross over points, said diode means including a diode having at least a first region and a second region said regions abutting each other to form a junction therebetween and said first region being made of amorphous alloy comprising silicon and hydrogen and/or fluorine.

2. A diode array according to claim 1 wherein said amorphous alloy is of the formula $Si_a F_b H_c$ wherein a is between 80 and 98 atomic percent, b is between 0 and 10 atomic percent and c is between 0 and 10 atomic percent.

3. A diode array according to claim 1 or claim 2 wherein said amorphous alloy contains hydrogen and fluorine.



4. A diode array according to any one of claims 1 to 3 wherein said first region of amorphous alloy is doped with an n type dopant material.

5 5. A diode array according to any one of claims 1 to 4 wherein said first region is doped with an amount of dopant material constituting between a few parts per million and five atomic percent.

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6. A diode array according to claims 4 or 5 wherein said dopant material is phosphorus.

7. A diode array according to claims 4 or 5
15 wherein said dopant material is arsenic.

8. A diode array according to any one of claims 1 to 7 wherein said second region is a metal, a metal alloy or a metallic like material having a
20 high barrier height on said first region so as to create a Schottky barrier.

9. A diode array according to any one of claims 1 to 8 wherein said second region is a metal chosen
25 from the group consisting of gold, platinum, paladium



or chromium.

10. A diode array according to claims 1 to 7
wherein said second region is made of an amorphous
5 alloy including silicon and fluorine and/or hydrogen.

11. A diode array according to claim 10 wherein
said amorphous alloy of said second region is $\text{Si}_a\text{F}_b\text{H}_c$
wherein a is between 80 and 98 atomic percent, b is
10 between 0 and 10 atomic percent and c is between 0
and 10 atomic percent.

12. A diode array according to claim 10 or 11
wherein said second region of amorphous material is
15 doped with a p-type dopant material.

13. A diode array according to any one of
claims 1 to 12 wherein said second region is doped
by an amount of dopant material constituting between
20 a few parts per million and five in atomic percent.

14. A diode array according to claim 13 wherein
said dopant material is boron or aluminum.

25 15. A modification of the diode array according
to any one of claims 1 to 14 wherein said first and
second regions have an insulator therebetween.



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16. A diode array according to claim 1 wherein said second region is made of a material dissimilar to said amorphous alloy such as to form a heterojunction.

5 17. A diode array according to claim 1 or 16 wherein said first region is N or P doped and said second region is P or N doped respectively.

10 18. A diode array according to any one of claims 1 to 17 wherein at least said first region is a deposited thin film.

15 19. A ROM device including open or closed memory circuit means at each circuit cross over point of a conductor of a first group of conductors extending in a first direction over a conductor of a second group of conductors extending in a second direction traversing the first direction, the first group of conductors being insulated from the second group of conductors, and each memory circuit means being coupled to and
20 between a pair of crossing over conductors at one of the cross over points and including rectifying means, said rectifying means including a diode having at least a first region and a second region, said regions abut-
25 ting each other to form a junction therebetween and said first region being made of amorphous alloy.



20. The ROM device according to claim 19 wherein said amorphous alloy contains at least silicon, fluorine and/or hydrogen.

21. The ROM device according to claim 20 wherein said amorphous alloy is $\text{Si}_a\text{F}_b\text{H}_c$ wherein a is between 80 and 98 atomic percent, b is between 0 and 10 atomic percent and c is between 0 and 10
5 atomic percent.

22. The ROM device according to any one of claims 19 to 21 wherein said first region of amorphous alloy is doped with an n-type dopant material.

23. The ROM device according to any one of claims 19 to 22 wherein said second region is a metal, a metal alloy or a metallic like material having a high barrier height on said first region
5 so as to create a Schottky barrier.

24. The ROM device according to any one of claims 19 to 22 wherein said second region is made of an amorphous alloy including silicon and fluo-



rine and/or hydrogen.

25. The ROM device according to claim 24 wherein said second region of amorphous alloy is doped with a p-type dopant material.

26. The ROM device according to claim 19 wherein said second region is made of a material dissimilar to said amorphous alloy such as to form a heterojunction.

27. The ROM device according to claim 19 wherein said first region is N or P doped and said second region is P or N doped.

28. The ROM device according to any one of claims 19 to 27 wherein at least said first region is a deposited thin film.

29. The ROM device according to any one of claims 19 to 28 wherein said memory circuit means include a memory region which is aligned with said regions of said diode and all of said regions being
5 juxtaposed and being situated on a line substan-



tially perpendicular to and extending between a pair of cross over conductors at the cross over with deposited oxide isolation being between each cross over thereof to provide a very small center-to-center distance between adjacent memory circuit means thereby to provide a very high packing density of memory circuit means in said ROM device.

30. The ROM device according to claim 29 wherein said memory region and said diode are thin film depositions.

31. The ROM device according to claim 19 or 30 wherein at least some of said memory circuit means are stacked one above the other.

32. The ROM device according to any one of claims 19 to 31 wherein said first and second regions have an insulator therebetween.

33. An EEPROM device having memory circuit means at each cross over point of a conductor of a first group of conductors extending in a first direction over a conductor of a second group of



5 conducto extending in a second direction tra-
versing the first direction, the first group of
conductors being insulated from the second group of
conductors; each memory circuit means being coupled
to and between a pair of crossing over conductors
10 at one of the cross over points and including
rectifying means, said rectifying means comprising a
diode having at least a first region and a second
region said regions abutting each other to form a
junction therebetween and said first region being
15 made of an amorphous alloy.

34. The EEPROM device according to claim 33
wherein said amorphous alloy contains at least
silicon, fluorine and/or hydrogen.

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35. The EEPROM device according to claim 33
or 34 wherein said amorphous alloy is $\text{Si}_a\text{F}_b\text{H}_c$ wherein
a is between 80 and 98 atomic percent, b is between
0 and 10 atomic percent and c is between 0 and 10
25 atomic percent.

36. The EEPROM device according to any one of
claims 33 to 35 wherein said first region of amor-



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phous material is doped with an n-type dopant material.

37. The EEPROM device according to any one of claims 33 to 36 wherein said second region is a metal, metal alloy or metallic like material having a high barrier height on said first region so as to
5 create a Schottky barrier.

38. The EEPROM device according to any one of claims 33 to 36 wherein said second region is made of an amorphous alloy including silicon and fluorine and/or hydrogen.

39. The EEPROM device according to claim 38 wherein said second region of amorphous alloy is doped with a p-type dopant material.

40. The EEPROM device according to any one of claims 33 to 39 wherein said second region is made of a material dissimilar to said amorphous alloy such as to form a heterojunction.



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41. The EEPROM device according to any one of claims 33 to 36 or 38 to 40 wherein said first region is N or P doped and said second region is P or N doped.

42. The EEPROM device according to any one of claims 33 to 41 wherein said first region is doped by an amount of dopant material constituting between a few parts per million and five atomic percent.

43. The EEPROM device according to any one of claims 33 to 42 wherein at least said first region is a deposited thin film.

44. The EEPROM device according to any one of claims 33 to 43 wherein said memory circuit means include a memory region which is aligned with said regions of said diode and all of said regions being juxtaposed and situated on a line substantially perpendicular to and extending between a pair of cross over conductors at a cross over with deposited oxide isolation between each cross over thereof to provide a very small center-to-center dis-



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10 tance between adjacent memory circuit means thereby to provide a very high packing density of memory circuit means in said EEPROM device.

45. The EEPROM device according to claim 44 wherein said memory region and said diode are thin film depositions.

46. The EEPROM device according to claim 45 wherein said memory region comprises a reversible phase change material which can be set in a highly conductive state or a high non-conductive state.

47. The EEPROM device according to any one of claims 44 to 46 wherein each said memory circuit means include a memory region including germanium and tellurium.

48. The EEPROM device according to claim 46 or 47 wherein each memory circuit includes a memory structure situated between one of the conductors and one region of said diode, said memory structure
5 including first, second and third regions, said first regions being adjacent to the one conductor



or said one region whichever is adapted to be coupled to a positive voltage source, said second regions being between said first and third regions, and said third region being adjacent said one region or the one conductor whichever is adapted to be coupled to a negative line of the voltage source and completely separating said second region from the connection to the negative lines and second region being formed of a tellurium based chalcogenide which has higher electrical resistance in its amorphous state and lower electrical resistance in its crystalline state and can be switched from one state to another upon application to the conductors of an electrical signal of appropriate value, said first region being formed of a material having a higher percentage of tellurium than said second region, said third region being formed of a material having between 25 and 45 atomic percent of germanium, the remaining material being substantially tellurium.

49. The EEPROM device according to any one of claims 33 to 48 wherein one or more of the memory circuit means are stacked one above the other.



50. The ROM device according to any one of claims 19 to 32 formed by thin film deposition technique on a thin layer of insulating material which in turn had been deposited on a metal substrate such that heat generated by the active components of the ROM device can be transferred by conduction to the metal substrate which serves as a heat sink for dissipating such heat.

51. The EEPROM device according to any one of claims 33 to 49 formed by thin film deposition technique on a thin layer of insulating material which in turn had been deposited on a metal substrate such that heat generated by the active components of the EEPROM device can be transferred by conduction to the metal substrate which serves as a heat sink for dissipating such heat.

52. A diode array substantially as hereinbefore described.

53. A ROM device substantially as hereinbefore described with reference to and as illustrated in Figures 1 to 3 or Figures 7 and 8 of the accompanying drawings.



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54. An EEPROM device substantially as hereinbefore described with reference to and as illustrated in Figures 4 to 6 of the accompanying drawings.

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