

Description

This invention relates to a synchronizing arrangement such as for a television deflection apparatus.

Television displays of television signals are generated by repetitively scanning an electron beam over the surface of a picture tube viewing screen. The beam intensity is modulated by video signals to form images on the screen representative of the picture to be displayed. In order to synchronize the scanning of the beam with the display information, the scanning or deflection circuits are synchronized with a synchronizing signal combined with the image information in a composite video signal. As received, the synchronizing signal may contain distortions in the form of electrical noise.

As transmitted, the synchronizing signal pulses recur at a rate which is stable. Because of the presence of noise it has become common practice to obtain synchronization of the horizontal deflection circuit with the horizontal synchronizing signal pulses by the use of an oscillator. The oscillator is controlled by and is included in a phase-lock loop (PLL). The oscillator generates a signal at a frequency that is equal to, for example, a high multiple of the synchronizing signal frequency f_H . Because of the PLL operation, when, for example, one synchronizing pulse is obscured by noise, the rate of the oscillator, nevertheless, remains substantially unchanged, and the deflection circuits continue to receive regular deflection control pulses.

It may be desirable, for purposes of stability of the PLL, to use an oscillator operating at a frequency that is greater than f_H that is then followed by a frequency divider arrangement that produces from a signal of the oscillator a horizontal-rate output signal with high stability. The horizontal rate output signal may be locked by the PLL to the average phase of the incoming synchronizing signal.

Such PLL is internal to, for example, an integrated circuit (IC) TA 7777 that is made by Toshiba Co. (the Toshiba IC). The Toshiba IC, or other similar integrated circuits, produces, at a corresponding pair of output terminals, a first output signal at the horizontal frequency f_H and a second output signal at a frequency that is 32 times the horizontal frequency f_H respectively. The first output signal may be used in a television receiver to produce the horizontal rate deflection current.

In the normal operation of a television receiver, a horizontal deflection circuit output stage produces high-voltage retrace pulses. It is customary to derive a high ultor voltage required for operation of a kinescope of the receiver by rectifying and filtering the high-voltage pulses.

The timings of a deflection current in a deflection winding and of the retrace pulses produced by the horizontal deflection circuit output stage may vary in a manner dependent upon loading of the ultor voltage generating circuit. For example, such loading is dependent upon the brightness of the image being displayed on the kinescope. This variation in the timings of the horizontal retrace pulses, disadvantageously, may cause a distortion of the image being displayed.

To prevent the occurrence of variation in a delay of the deflection current relative to the synchronizing signal, a dual feedback loop arrangement may be used. In such arrangement, a horizontal oscillator generates a signal at, for example, a frequency greater than the horizontal frequency. The oscillator generated signal is divided down in a frequency divider and an output signal at approximately horizontal frequency is generated. A PLL having a relatively long time constant controls the oscillator to maintain the output signal in frequency and phase synchronism with horizontal synchronizing signals. The frequency divider may be included in the PLL. In order to compensate for load-dependent variations in the delay of the horizontal deflection circuit output stage, a phase-control loop circuit (PCL) may be used. The PCL includes a phase detector, a first input terminal of which is coupled to an output of the PLL and a second input terminal of which is coupled to the deflection circuit output stage for responding to the retrace pulses. The phase detector produces a phase difference indicative signal from the signals at the first and second input terminals. A loop filter is coupled to an output of the phase detector to form a control signal. A controllable phase shifter is responsive to the control signal that is generated by the loop filter for producing horizontal-rate drive pulses at a variable delay which makes the retrace pulses synchronous with the output signal of the PLL even when variations of beam current loading occur.

An example of a dual loop controlled system is disclosed in GB-A-2 034 137 (RCA CORPORATION) which describes a television apparatus comprising:

a source of synchronising input signal at a frequency that is related to a deflection frequency; means responsive to said input signal for generating at a first terminal a first signal that is synchronised to said input signal at a first frequency that is related to that of said input signal; and

first frequency dividing means responsive to said first signal for generating at a second terminal a second signal at a second frequency that is related to said deflection frequency and that is lower than said first frequency. This disclosure corresponds to the preamble to claim 1.

In some applications, the PCL requires, for its internal operation, timing signals at various multiple frequencies of the horizontal frequency that are at corresponding predetermined constant phases relative to the horizontal rate output signal of the PLL. It may be desirable to generate each of such timing signals from, for example, a signal that is generated in the PLL that is at a high multiple of the horizontal frequency.

According to the invention there is provided a television apparatus, comprising:

a source of synchronising input signal at a frequency that is related to a deflection frequency; means responsive to said input signal for generating at a first terminal a first signal that is synchronised to said input signal at a first frequency that is related to that of said input signal;

first frequency dividing means responsive to said first signal for generating at a second terminal a second signal at a second frequency that is related to said deflection frequency and that is lower than said first frequency; characterised by:

second frequency dividing means responsive to said first signal for generating a third signal at a frequency that is lower than said first frequency;

means for initialising said second frequency dividing means, said initialising means being responsive to said second signal for generating a phase initialisation signal that is coupled to said second frequency dividing means for varying a phase of said third signal to correspond with that of said second signal; and

a utilisation circuit responsive to said third signal, said utilisation circuit requiring, for its proper operation, said phase of said third signal to correspond with that of said second signal.

In the above cited apparatus the second loop operates at the horizontal frequency. As a result, the various timing signals which are needed in the second loop are not as precisely generated as they would be if derived from a divided multiple of the horizontal frequency as in the present invention.

In the Drawing:

The sole FIGURE illustrates a phase-lock-loop circuit and a phase-control-loop circuit, embodying the invention, that control the phase of a deflection current in a deflection winding.

Horizontal sync pulses S_H having a period H , that in a NTSC standard is 63.5 microseconds, and having a corresponding frequency f_H , are coupled, illustratively, from a conventional sync separator of a television receiver, not shown in the FIGURE, to an input terminal 30a of a phase detector 30. A signal O_H that during steady state operation is at the frequency f_H is coupled via a capacitor C_C to a second input terminal 30b of phase detector 30. A phase difference indicative signal PH that is indicative of the phase difference between signal S_H and

signal O_H is generated by phase detector 30 and coupled to a frequency control input terminal 31a of a voltage controlled oscillator 31. Oscillator 31 generates an output signal O_{32H} at a frequency $32xf_H$. Signal O_{32H} is frequency divided by 32 in a frequency divider 32 to produce signal O_H . Detector 30, oscillator 31 and frequency divider 32 form a phase-lock-loop circuit (PLL) 20 that may be included in a first integrated circuit 100 such as, for example, the Toshiba IC. The operation of PLL 20 causes signals O_H and O_{32H} to be synchronized with signal S_H .

A phase-control-loop (PCL) 70, having a control section that may be internal to a second integrated circuit 200, generates a signal D_H at the frequency f_H . Signal D_H is coupled via an inverter 133 to a horizontal driver 33 that generates a signal 33a that is coupled to a base electrode of a switching transistor Q1. Transistor Q1 is included in, for example, a conventional horizontal output stage 99. Output stage 99 produces, in a winding 34 of a flyback transformer T0, a retrace pulse at a high voltage that is used, in a high voltage supply 35, for generating an ultor voltage U at terminal 35a. Voltage U is coupled to an ultor electrode of a cathode ray tube, not shown in the FIGURE, of the television receiver. PCL 70 is synchronized to signal O_H in such a way that deflection current I_Y in a deflection winding L_Y is maintained in a constant phase relationship relative to signal O_H despite varying beam current loading that loads winding 34 in a manner to be described in detail.

IC 200 includes a frequency dividing arrangement 45, embodying an aspect of the invention. Arrangement 45 includes a flip-flop 40 having a clock receiving terminal 40a that receives signal O_{32H} that is at the frequency $32xf_H$. Flip-flop 40 generates an output signal E_{16H} that toggles, or changes states, each time a clocking edge of signal O_{32H} occurs. Signal E_{16H} is at a frequency $16xf_H$ that is one-half of the frequency of signal O_{32H} . Flip-flop 40 forms the first stage in five-stage cascaded-coupled frequency dividing arrangement 45 that includes flip-flops 40-44. Note that none of the frequency dividing stages of arrangement 45 is in common with any stage of frequency divider 32. Arrangement 45 generates corresponding output signals E_{16H} , E_{8H} , E_{4H} , E_{2H} and E_H at frequencies $16xf_H$, $8xf_H$, $4xf_H$, $2xf_H$ and f_H , respectively, at corresponding output terminals of flip-flops 40-44.

Embodying an aspect of the invention, horizontal rate signal O_H is coupled via an "AND" gate 52 to a corresponding reset pulse receiving terminal RESET of each of flip-flops 40-44 for abruptly resetting the phase of each of signals E_{16H} , E_{8H} , E_{4H} , E_{2H} and E_H to insure that they conform to that of signal O_H . Resetting the phase of such signals is done by causing each of flip-flops 40-44 to assume

abruptly a FALSE state when a leading edge O_{Ha} of signal O_H occurs, as described later on. In this way, flip-flops 40-44 are initialized. Initializing flip-flops 40-44 is required because flip-flops 40-44 are outside the feedback loop of PLL 20. The phase of each of the output signals of flip-flops 40-44, if flip-flops 40-44 were not initialized, disadvantageously, would not be predetermined. If the phase of the output signals of flip-flops 40-44 were not predetermined, PCL 30 would operate, disadvantageously, improperly.

A flip-flop 51 delays signal O_H by approximately one microsecond to form a delayed signal 51a that is also inverted. The one microsecond delay time is caused by using, for clocking flip-flop 51, a transition edge of signal O_{32H} that occurs between the transition edges used for clocking frequency divider 32. The delayed signal 51a that is coupled to an input terminal 52a of "AND" gate 52 disables gate 52 one microsecond after leading edge O_{Ha} of signal O_H . Thus a pulse 50 is generated on a conductor 49 when both signals 51a and O_H are simultaneously at corresponding TRUE state. Pulse 50 that has a duration of approximately one microsecond and that is at the horizontal rate f_H is synchronized to signal O_H . When pulse 50 occurs, each of flip-flops 40-44 is initialized to provide the corresponding output signal at a corresponding predetermined state such as, for example, a FALSE state. Without the initialization operation performed by pulse 50, the phase of the signals at the output terminals of flip-flops 40-44, disadvantageously, would not have been predetermined.

Each of the output signals of flip-flops 40-44 is also periodic at the frequency f_H of signals O_H and 50. Therefore, if no significant phase perturbation in signals O_H and O_{32H} of PLL 20 occurs, once initialized by signal 50, each of the corresponding output signals of flip-flops 40-44 will remain, in each subsequent period H , in a corresponding constant phase relationship with respect to signal O_H . It should be understood that flip-flops 40-44, 51 and gate 52 are located outside the feedback loop of PLL 20.

Embodying an aspect of the invention, by having signals E_{16H} , E_{8H} , E_{4H} , E_{2H} and E_H thus synchronized to signal O_H , these signals may be used to provide timing signals with edges that occur at predetermined instants during each period H of signal O_H . The resolution by which each such timing pulse or signal is provided is determined by the period of signal O_{32H} . A horizontal rate signal 36 produced at an output terminal 53a of a flip-flop 53 that is used for generating a sawtooth reference signal in PCL 70 is a representative example of such timing signals.

To generate signal 36, signals E_{4H} , E_{2H} and E_H are coupled to corresponding input terminals of an AND gate 54 that produces a signal 54a having the TRUE state when each of such signals is at the TRUE state simultaneously with the other ones. Signal 54a is coupled to a data input receiving terminal 53c of a flip-flop 53. Signal E_{8H} is coupled to a clock input receiving terminal 53b of flip-flop 53. Flip-flop 53 delays signal 54a by an interval having a duration that is determined by signal E_{8H} to form signal 36. Signal 36 is at the TRUE state during approximately 8 microseconds and at the FALSE state during the rest of period H . By means of gate 54 and flip-flop 53, signal 36 is delayed relative to signal O_H by a predetermined delay of, for example, 4 microseconds that is determined by signals E_{8H} , E_{4H} , E_{2H} and E_H . Signal 36 is used for controlling the timing of a ramp generator 37 of IC 200 that is used by PCL 70, as described below.

Ramp generator 37 generates a sawtooth signal 37a that is coupled to an input terminal 38a of a voltage comparator 38. Generator 37 includes a current source i_{cs} that is coupled to a capacitor C_{37} that may be external to IC 200. A switch 37b of generator 37 is coupled across capacitor C_{37} for discharging capacitor C_{37} and for maintaining, afterward, sawtooth signal 37a across capacitor C_{37} at a constant level as long as horizontal rate control signal 36 is at the TRUE state. When signal 36 is at the FALSE state, current source i_{cs} charges capacitor C_{37} to form an upramping portion 37c of signal 37a.

Signal O_H is also coupled via a flip-flop 39 to an input terminal 57a of a second phase detector 57. Flip-flop 39 is clocked by signal E_{8H} to provide a delayed signal 39a that is delayed relative to signal O_H by approximately 4 microseconds. The purpose of utilizing the 4 microsecond delay is to compensate for various delays in PCL 70 such as in a delay and pulse shaping network 58 that is discussed below. A signal F_H , developed in a winding 136 of flyback transformer TO, is coupled via delay and pulse shaping network 58 to a second input terminal 57b of second phase detector 57. Signal F_H is indicative of the phase of deflection current i_y in deflection winding L_y . An output signal 59 of second phase detector 57 that is indicative of the phase difference between signal 39a and signal F_H is coupled via low-pass filter 66 to form a control signal 66a at a second input terminal 38b of comparator 38.

When, during a given period H , ramping portion 37c of signal 37a becomes greater than signal 66a at terminal 38b of comparator 38, comparator 38 generates a signal transition edge of an output signal 60 that is coupled to a triggering input terminal 61a of a one-shot flip-flop 61. Flip-flop 61 then generates a pulse D_{Ha} having, illustratively, a

constant duration that is coupled to horizontal driver 33 through inverter 133 to cause transistor Q1 to become nonconductive, for example. Comparator 38 varies a phase of pulse D_{Hh} relative to that of signal O_H in such a manner that signal F_H will have a constant phase relationship relative to signal O_H . Thus, a change in the ultor loading at a terminal 35a of a high voltage supply 35 that tends to cause a change in the phase of signal F_H , will cause a corresponding change to control signal 66a that will vary the phase in the delay of pulse D_{Hh} in a negative feedback manner. The change in the phase of pulse D_{Hh} will maintain the phase of signal F_H and of deflection current i_y constant relative to signal O_H despite the change in phase of signal F_H .

The tracking response time, in PCL 70 with respect to phase variations of retrace signal F_H is faster than the corresponding tracking response in PLL 20 with respect to phase variations of synchronizing input signal S_H because PCL 70 is optimized to accommodate fast switching time variations in output stage 99 that may occur because of fast changing electron beam current. PLL 20 is optimized to reject noise or jitter accompanying the sync pulses in signal S_H .

Thus, frequency dividing arrangement 45 that is located outside the feedback loop of PLL 20 generates timing signals that are maintained in phase with signal O_H , generated by frequency divider 32. As indicated before, frequency divider 32 is included in the feedback loop of PLL 20. Maintaining the phase of the timing signals of frequency dividing arrangement 45 is accomplished, embodying a preferred aspect of the invention, by utilizing pulse 50 that initializes flip-flops 40-44 of frequency dividing arrangement 45.

Claims

1. A television apparatus, comprising:
 - a source of synchronising input signal (S_H) at a frequency that is related to a deflection frequency (f_H); means (20) responsive to said input signal (S_H) for generating at a first terminal a first signal (O_{32H}) that is synchronised to said input signal at a first frequency ($32f_H$) that is related to that of said input signal (S_H);
 - first frequency dividing means (32) responsive to said first signal (O_{32H}) for generating at a second terminal a second signal (O_H) at a second frequency (f_H) that is related to said deflection frequency and that is lower than said first frequency ($32f_H$); characterised by:
 - second frequency dividing means (45) responsive to said first signal (O_{32H}) for generating a third signal at a frequency (f_H) that is lower than said first frequency ($32f_H$);
 - means (51,52) for initialising said second

frequency dividing means (45) said initialising means being responsive to said second signal (O_H) for generating a phase initialisation signal that is coupled to said second frequency dividing means for varying a phase of said third signal (54a) to correspond with that of said second signal (O_H); and

a utilisation circuit (99) responsive to said third signal (54a), said utilisation circuit (99) requiring, for its proper operation, said phase of said third signal (54a) to correspond with that of said second signal (O_H).

2. An apparatus according to claim 1 characterised in that said first (O_{32H}) and second (O_H) signals are generated in a phase-lock-loop circuit (20) such that each of said first (O_{32H}) and second (O_H) signals is synchronised to said input signal (S_H).
3. An apparatus according to claim 2 characterised in that said phase-lock-loop circuit (20) is included in a first integrated circuit (100) and wherein said second frequency dividing means (45) is located outside said first integrated circuit (100).
4. An apparatus according to Claim 2 characterized by a phase-control-loop circuit (70) responsive to said third signal (54a) for generating a control signal (D_H) at a controllable phase, wherein said utilization circuit (99) comprises a deflection circuit output stage that is responsive to said control signal (D_H), said output stage (99) generating a deflection cycle indicative signal (F_H) that is indicative of a phase of a deflection current (i_y) in a deflection winding (L_y), said deflection cycle indicative signal (F_H) being coupled to a phase detector (57) of said phase-control-loop circuit (70) that varies a phase of said control signal (D_H) in accordance with a phase difference between said deflection cycle indicative signal (F_H) and said second signal (O_H).
5. An apparatus according to Claim 4 characterized by means (37) responsive to said third signal (54a) for generating a sawtooth waveform (37a) that is synchronized to said third signal (54a), and a comparator (38) responsive to said sawtooth waveform (37a) and to an output signal (66a) of said phase detector (57) for generating said control signal (D_H) when said sawtooth waveform (37a) is at a level that corresponds with that of said output signal (59) of said phase detector (57).

constant duration that is coupled to horizontal driver 33 through inverter 133 to cause transistor Q1 to become nonconductive, for example. Comparator 38 varies a phase of pulse D_{Ha} relative to that of signal O_H in such a manner that signal F_H will have a constant phase relationship relative to signal O_H . Thus, a change in the ultor loading at a terminal 35a of a high voltage supply 35 that tends to cause a change in the phase of signal F_H , will cause a corresponding change to control signal 66a that will vary the phase in the delay of pulse D_{Ha} in a negative feedback manner. The change in the phase of pulse D_{Ha} will maintain the phase of signal F_H and of deflection current i_y constant relative to signal O_H despite the change in phase of signal F_H .

The tracking response time, in PCL 70 with respect to phase variations of retrace signal F_H is faster than the corresponding tracking response in PLL 20 with respect to phase variations of synchronizing input signal S_H because PCL 70 is optimized to accommodate fast switching time variations in output stage 99 that may occur because of fast changing electron beam current. PLL 20 is optimized to reject noise or jitter accompanying the sync pulses in signal S_H .

Thus, frequency dividing arrangement 45 that is located outside the feedback loop of PLL 20 generates timing signals that are maintained in phase with signal O_H , generated by frequency divider 32. As indicated before, frequency divider 32 is included in the feedback loop of PLL 20. Maintaining the phase of the timing signals of frequency dividing arrangement 45 is accomplished, embodying a preferred aspect of the invention, by utilizing pulse 50 that initializes flip-flops 40-44 of frequency dividing arrangement 45.

Claims

1. A television apparatus, comprising:

a source of synchronising input signal (S_H) at a frequency that is related to a deflection frequency (f_H); means (20) responsive to said input signal (S_H) for generating at a first terminal a first signal (O_{32H}) that is synchronised to said input signal at a first frequency ($32f_H$) that is related to that of said input signal (S_H);

first frequency dividing means (32) responsive to said first signal (O_{32H}) for generating at a second terminal a second signal (O_H) at a second frequency (f_H) that is related to said deflection frequency and that is lower than said first frequency ($32f_H$); characterised by:

second frequency dividing means (45) responsive to said first signal (O_{32H}) for generating a third signal at a frequency (f_H) that is lower than said first frequency ($32f_H$);

means (51,52) for initialising said second

frequency dividing means (45) said initialising means being responsive to said second signal (O_H) for generating a phase initialisation signal that is coupled to said second frequency dividing means for varying a phase of said third signal (54a) to correspond with that of said second signal (O_H); and

a utilisation circuit (99) responsive to said third signal (54a), said utilisation circuit (99) requiring, for its proper operation, said phase of said third signal (54a) to correspond with that of said second signal (O_H).

2. An apparatus according to claim 1 characterised in that said first (O_{32H}) and second (O_H) signals are generated in a phase-lock-loop circuit (20) such that each of said first (O_{32H}) and second (O_H) signals is synchronised to said input signal (S_H).
3. An apparatus according to claim 2 characterised in that said phase-lock-loop circuit (20) is included in a first integrated circuit (100) and wherein said second frequency dividing means (45) is located outside said first integrated circuit (100).
4. An apparatus according to Claim 2 characterized by a phase-control-loop circuit (70) responsive to said third signal (54a) for generating a control signal (D_H) at a controllable phase, wherein said utilization circuit (99) comprises a deflection circuit output stage that is responsive to said control signal (D_H), said output stage (99) generating a deflection cycle indicative signal (F_H) that is indicative of a phase of a deflection current (i_y) in a deflection winding (L_y), said deflection cycle indicative signal (F_H) being coupled to a phase detector (57) of said phase-control-loop circuit (70) that varies a phase of said control signal (D_H) in accordance with a phase difference between said deflection cycle indicative signal (F_H) and said second signal (O_H).
5. An apparatus according to Claim 4 characterized by means (37) responsive to said third signal (54a) for generating a sawtooth waveform (37a) that is synchronized to said third signal (54a), and a comparator (38) responsive to said sawtooth waveform (37a) and to an output signal (66a) of said phase detector (57) for generating said control signal (D_H) when said sawtooth waveform (37a) is at a level that corresponds with that of said output signal (59) of said phase detector (57).



6. An apparatus according to claim 2 characterised in that a feedback loop signal path of said phase-lock-loop circuit (20) includes said first frequency dividing means (32) and wherein said second frequency dividing means (45) is located outside said feedback loop signal path of said phase-lock-loop circuit (20). 5
7. An apparatus according to claim 1 characterised in that said means (51,52) for initialising said second frequency dividing means (45) comprises means (51) responsive to said first signal (O_{32H}) for delaying said second signal (O_H) in accordance with said first signal (O_{32H}) to generate a delayed signal (51a), and means (52) responsive to said undelayed second (O_H) and delayed (51a) signals for generating therefrom said phase initialisation signal (50). 10 15
8. An apparatus according to Claim 7 characterized in that said signal delaying means (51) comprises a flip-flop having a clock receiving terminal that is coupled to said first signal (O_{32H}), an input terminal (D) that is coupled to said second signal (O_H) and an output terminal (Q) where said delayed signal (51a) is generated, wherein said delayed signal (51a) at said output terminal (Q) of said flip-flop (51) and said second signal (O_H) are coupled to corresponding input terminals of a gate (52) that generates said phase synchronization signal (50) at an output terminal of said gate (52). 20 25 30
9. An apparatus according to Claim 1 characterized in that said first signal (O_{32H}) is coupled to a clock receiving terminal (40a) of said second frequency dividing means (45) that has a plurality of frequency dividing stages, and wherein said phase initialization signal (50) is coupled to a second input terminal (49) of said second frequency dividing means (45) to initialize abruptly each frequency dividing stage of said second frequency dividing means (45) to a corresponding predetermined state when said phase initialization signal (50) occurs. 35 40 45
10. An apparatus according to Claim 1 characterized in that said second frequency dividing means (45) is located outside said first frequency dividing means (32). 50
11. An apparatus according to Claim 1 characterized in that said phase initialization signal (50) causes a phase difference between said third (54a) and second (O_H) signals to remain constant irrespective of a phase variation that occurs in said input signal (S_H). 55

Patentansprüche

1. Fernsehgerät mit
einer Quelle eines synchronisierenden Eingangssignals (S_H) mit einer Frequenz, die auf eine Ablenkfrequenz (f_H) bezogen ist; einer durch dieses Eingangssignal (S_H) gesteuerten Schaltung (20), welche an einem ersten Anschluß ein erstes Signal (O_{32H}) erzeugt, das mit dem Eingangssignal synchronisiert ist und eine erste Frequenz ($32f_H$) hat, welche auf diejenige des Eingangssignals (S_H) bezogen ist;
einer ersten Frequenzteilerschaltung (32), welche unter Steuerung durch das erste Signal (O_{32H}) an einem zweiten Anschluß ein zweites Signal (O_H) mit einer zweiten Frequenz (f_H) erzeugt, die auf die Ablenkfrequenz bezogen ist und niedriger als die erste Frequenz ($32f_H$) ist; **gekennzeichnet durch:**
eine zweite Frequenzteilerschaltung (45), die unter Steuerung durch das erste Signal (O_{32H}) ein drittes Signal mit einer Frequenz (f_H) erzeugt, die niedriger als die erste Frequenz ($32f_H$) ist,
eine der Initialisierung der zweiten Frequenzteilerschaltung (45) dienende Schaltung (51,52), welche unter Steuerung durch das zweite Signal (O_H) ein Phaseninitialisierungssignal erzeugt, das der zweiten Frequenzteilerschaltung zugeführt wird zur Veränderung der Phasenlage des dritten Signals (54a) derart, daß sie mit derjenigen des zweiten Signals (O_H) übereinstimmt, und
eine auf das zweite Signal (O_H) und das dritte Signal (54a) ansprechende Nutzschaltung (99), zu deren richtigem Betrieb die Phasenlage des dritten Signals (54a) derjenigen des zweiten Signals (O_H) entsprechen muß. 5 10 15 20 25 30 35 40 45
2. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß das erste Signal (O_{32H}) und das zweite Signal (O_H) in einer Phasenverriegelungsschleifenschaltung (20) derart erzeugt werden, daß diese beiden Signale mit dem Eingangssignal (S_H) synchronisiert sind. 50
3. Gerät nach Anspruch 2, **dadurch gekennzeichnet**, daß die Phasenverriegelungsschleifenschaltung (20) in einer ersten integrierten Schaltung (100) enthalten ist und daß die zweite Frequenzteilerschaltung (45) sich außerhalb der ersten integrierten Schaltung (100) befindet. 55
4. Gerät nach Anspruch 2, **dadurch gekennzeichnet**, daß eine Phasensteuerschleifenschaltung (70) vorgesehen ist, welche unter Steuerung durch das dritte Signal (54a) ein 5



Steuersignal (D_H) mit steuerbarer Phasenlage erzeugt und daß die Nutzschaltung (99) eine Ablenkschaltungsendstufe aufweist, die in Abhängigkeit von dem Steuersignal (D_H) ein Ablenkzyklusanzeigesignal (F_H) als Maß für die Phasenlage eines Ablenkstroms (I_y) in einer Ablenkwicklung (L_y) erzeugt, welches einem Phasendetektor (57) der Phasensteuerschleifenschaltung (70) zugeführt wird, die ihrerseits die Phasenlage des Steuersignals (D_H) entsprechend der Phasendifferenz zwischen dem Ablenkzyklusanzeigesignal (F_H) und dem zweiten Signal (O_H) verändert.

5. Gerät nach Anspruch 4, **gekennzeichnet** durch eine auf das dritte Signal (54a) ansprechende Schaltung zur Erzeugung eines mit dem dritten Signal (54a) synchronisierten Sägezahnsignals (37a) und durch eine Vergleichsschaltung (38), die in Abhängigkeit von dem Sägezahnsignal (37a) und einem Ausgangssignal (68a) des Phasendetektors (57) das Steuersignal (D_H) erzeugt, wenn das Sägezahnsignal (37a) einen Wert hat, der demjenigen des Ausgangssignals (59) des Phasendetektors (57) entspricht.
6. Gerät nach Anspruch 2, **dadurch gekennzeichnet**, daß ein Rückkopplungsschleifensignalweg der Phasenverriegelungsschleifenschaltung (20) eine erste Frequenzteilerschaltung (32) enthält und daß eine zweite Frequenzteilerschaltung (45) außerhalb des Rückkopplungsschleifensignalweges der Phasenverriegelungsschleifenschaltung (20) liegt.
7. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die Schaltung (51,52) zur Initialisierung der zweiten Frequenzteilerschaltung (45) eine durch das erste Signal (O_{32H}) steuerbare Schaltung (51) enthält, die in Abhängigkeit von dem ersten Signal (O_{32H}) das zweite Signal (O_H) in Übereinstimmung mit dem ersten Signal (O_{32H}) zu einem verzögerten Signal (51a) verzögert, sowie eine aus dem unverzögerten zweiten Signal (O_H) und dem verzögerten Signal (51a) das Phaseninitialisierungssignal (50) erzeugende Schaltung (52).
8. Gerät nach Anspruch 7, **dadurch gekennzeichnet**, daß die Signalverzögerungsschaltung (51) ein Flipflop aufweist, dem an einem Takteingang das erste Signal (O_{32H}) zugeführt wird und dem an einem Eingang (D) das zweite Signal (O_H) zugeführt wird, und das an einem Ausgang (Q) das verzögerte Signal (51a) liefert, wobei dieses verzögerte Signal (51a) vom Ausgang (Q) des Flipflops (51) und das

zweite Signal (O_H) entsprechenden Eingängen eines Tores (52) zugeführt werden, das seinerseits das Phasensynchronsignal (50) an einem Torausgang liefert.

9. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß das erste Signal (O_{32H}) einem Takteingang (40a) der zweiten Frequenzteilerschaltung (45) zugeführt wird, die eine Mehrzahl von Frequenzteilerstufen aufweist, und daß das Phaseninitialisierungssignal (50) einem zweiten Eingang (49) der zweiten Frequenzteilerschaltung (45) zugeführt wird zur momentanen Initialisierung jeder Frequenzteilerstufe der zweiten Frequenzteilerschaltung (45) auf einen entsprechenden vorbestimmten Zustand, wenn das Phaseninitialisierungssignal (50) auftritt.
10. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die zweite Frequenzteilerschaltung (45) sich außerhalb der ersten Frequenzteilerschaltung (32) befindet.
11. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß das Phaseninitialisierungssignal (50) eine Phasendifferenz zwischen dem dritten Signal (54a) und dem zweiten Signal (O_H) unabhängig von im Eingangssignal (S_H) auftretenden Phasenänderungen konstant hält.

Revendications

1. Appareil de télévision comprenant :
 - une source de signal d'entrée de synchronisation (S_H) à une fréquence qui est en relation avec une fréquence de déviation (f_H); des moyens (20) agissant en réponse audit signal d'entrée (S_H) pour générer sur une première borne, un premier signal (O_{32H}) qui est synchronisé audit signal d'entrée à une première fréquence ($32 f_H$) qui est en relation avec celle dudit signal d'entrée (S_H);
 - des premiers moyens de division de fréquence (32) agissant en réponse audit premier signal (O_{32H}) pour générer sur une seconde borne un second signal (O_H) à une seconde fréquence (f_H) qui est en relation avec ladite fréquence de déviation et qui est inférieure à ladite première fréquence ($32f_H$), caractérisé par :
 - des seconds moyens de division de fréquence (45), agissant en réponse audit premier signal (O_{32H}) pour générer un troisième signal à une fréquence (f_H) qui est inférieure à ladite première fréquence ($32f_H$);



- des moyens (51,52) pour initialiser lesdits seconds moyens de division de fréquence (45), lesdits moyens d'initialisation agissant en réponse audit second signal (O_H) pour générer un signal d'initialisation de phase qui est couplé aux dits seconds moyens de division de fréquence pour faire varier une phase dudit troisième signal (54a) pour qu'elle corresponde à celle du second signal (O_H); et
 - un circuit d'utilisation (99) agissant en réponse audit troisième signal (54a), ledit circuit d'utilisation (99) nécessitant, pour son propre fonctionnement, que ladite phase dudit troisième signal (54a) corresponde à celle dudit second signal (O_H).
2. Appareil selon la revendication 1, caractérisé en ce que lesdits premier (O_{32H}) et second (O_H) signaux sont générés dans un circuit en boucle à verrouillage de phase (20) tel que chacun des premier (O_{32H}) et second (O_H) signaux sont synchronisés audit signal d'entrée (S_H).
3. Appareil selon la revendication 2, caractérisé en ce que ledit circuit en boucle à verrouillage de phase (20) est inclus dans un premier circuit intégré (100) et, dans lequel lesdits seconds moyens diviseurs de fréquence (45) sont situés à l'extérieur dudit premier circuit intégré (100).
4. Appareil selon la revendication 2, caractérisé par un circuit en boucle à commande de phase (70) agissant en réponse audit troisième signal (54a) pour générer un signal de commande (D_H) à une phase commandable, dans lequel ledit circuit d'utilisation (99) comprend un étage de sortie du circuit de déviation qui agit en réponse audit signal de commande (D_H), ledit étage de sortie (99) générant un signal indicatif de cycle de déviation (F_H) qui constitue une indication d'une phase d'un courant de déviation (i_y) dans un enroulement de déviation (L_y), ledit signal indicatif du cycle de déviation (F_H) étant couplé à un détecteur de phase (57) dudit circuit en boucle à commande de phase (70) qui fait varier une phase dudit signal de commande (D_H) selon une différence de phase entre ledit signal indicatif de cycle de déviation (F_H) et ledit second signal (O_H).
5. Appareil selon la revendication 4, caractérisé par des moyens (37), agissant en réponse audit troisième signal (54a) pour générer une
- forme d'onde en dents de scie (37a) qui est synchronisée audit troisième signal (54a), et un comparateur (38) agissant en réponse à ladite forme d'onde en dents de scie (37a) et à un signal de sortie (66a) dudit détecteur de phase (57) pour générer ledit signal de commande (D_H) lorsque ladite forme d'onde en dents de scie (37a) est à un niveau qui correspond à celui dudit signal de sortie (59) dudit détecteur de phase (57).
6. Appareil selon la revendication 2, caractérisé en ce qu'une trajectoire de signal en boucle de réaction du circuit en boucle à verrouillage de phase (20) comprend lesdits premiers moyens diviseurs de fréquence (32) et dans lequel lesdits seconds moyens diviseurs de fréquence (45) sont situés à l'extérieur de ladite trajectoire de signal en boucle de réaction dudit circuit en boucle à verrouillage de phase (20).
7. Appareil selon la revendication 1, caractérisé en ce que lesdits moyens (51,52) pour initialiser lesdits seconds moyens diviseurs de fréquence (45) comprennent des moyens (51) agissant en réponse audit premier signal (O_{32H}) pour retarder ledit second signal (O_H) en fonction dudit premier signal (O_{32H}) pour générer un signal retardé (51a), et des moyens (52) agissant en réponse auxdits seconds signaux non retardés (O_H) et retardés (51a) pour générer à partir de ceux-ci ledit signal d'initialisation de phase (50).
8. Appareil selon la revendication 7, caractérisé en ce que lesdits moyens retardateurs de signaux (51) comprennent un flip-flop ayant une borne de réception d'horloge qui est couplée audit premier signal (O_{32H}), une borne d'entrée (D) qui est couplée audit second signal (O_H) et une borne de sortie (Q) où est généré ledit signal retardé (51a), dans lequel ledit signal retardé (51a), sur ladite borne de sortie (Q) dudit flip-flop (51), et ledit second signal (O_H) sont couplés aux bornes d'entrée correspondantes d'une grille (52) qui génère ledit signal de synchronisation de phase (50), sur une borne de sortie de ladite grille (52).
9. Appareil selon la revendication 1, caractérisé en ce que ledit premier signal (O_{32H}) est couplé à une borne de réception d'horloge (40a) des seconds moyens diviseurs de fréquence (45) qui possèdent une pluralité d'étages de division de fréquence et dans lequel ledit signal d'initialisation de phase (50) est couplé à une seconde borne d'entrée (49) desdits seconds moyens de division de fréquence (45)



pour initialiser de façon abrupte, chaque étage de division de fréquence desdits seconds moyens diviseurs de fréquence (45), à un étage prédéterminé correspondant lorsque apparaît ledit signal d'initialisation de phase (50).

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10. Appareil selon la revendication 1, caractérisé en ce que lesdits seconds moyens diviseurs de fréquence (45) sont situés à l'extérieur desdits premiers moyens diviseurs de fréquence (32).

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11. Appareil selon la revendication 1, caractérisé en ce que ledit signal d'initialisation de phase (50) provoque une différence de phase, entre ledit troisième (54a) et ledit second (O_H) signaux, qui demeure constante quelle que soit la variation de phase qui survient dans ledit signal d'entrée (S_H).

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