CLAIMS

1. A method for preparing a final substrate comprising a thick buried dielectric layer, the method comprising:

- a step of preparing a support substrate comprising an electric-charge trapping layer disposed on a base substrate;
- a step of forming the dielectric layer having a thickness greater than 200 nm on the electric-charge trapping layer;
- a step of transferring an upper layer comprising a semiconductor material to the dielectric layer;
- a step of finishing the exposed face of the upper layer;

the preparation method being characterized in that the step of forming the dielectric layer is carried out by high-density plasma chemical vapour deposition and in that the finishing step comprises a first anneal performed in a neutral or reducing atmosphere at a temperature above 1050°C for a duration greater than 30 minutes.

2. The method according to claim 1, wherein the step of forming the dielectric layer comprises, after the high-density plasma chemical vapour deposition of the dielectric layer, a densifying anneal of the support substrate.

3. The method according to claim 2, wherein the densifying anneal is carried out in a neutral atmosphere at a temperature below 1000°C and for a duration less than 1 h.

4. The method according to one of the preceding claims, wherein the finishing step comprises a thinning of the upper layer before and/or after the first anneal.

5. The method according to one of the preceding claims, wherein the finishing step comprises a second anneal, the second anneal being performed in a neutral or reducing atmosphere at a temperature above 1050°C for a duration less than 2 minutes.

6. The method according to one of the preceding claims, wherein the neutral or reducing atmosphere of the first anneal comprises or is made up of argon.

7. The method according to one of the preceding claims, wherein the step of forming the dielectric layer does not include polishing the exposed face of the dielectric layer.

8. The method according to one of the preceding claims, wherein the semiconductor material of the upper layer is silicon.

9. The method according to one of the preceding claims, wherein the dielectric layer is made of silicon dioxide.

10. The method according to one of the preceding claims, wherein the dielectric layer has a thickness greater than or equal to 400 nm.

11. The method according to one of the preceding claims, wherein the step of transferring the upper layer comprises a step of implanting species referred to as “light” species in a donor substrate so as to form a weakened plane there, joining the donor substrate to the support substrate, and fracturing the donor substrate in the weakened plane.

12. A final substrate comprising the following in succession and in contact with one another: an upper layer made of semiconductor material, a dielectric layer having a thickness greater than 200 nm, an electric-charge trapping layer, and a base substrate, the final substrate being characterized in that it has a bow less than 60 micrometres, preferably less than 40 micrometres, and in that an exposed surface of the upper layer exhibits a roughness less than 0.3 nm measured in root mean square terms over a field of 30 micrometres by 30 micrometres.

13. The final substrate according to claim 12, wherein the upper layer is made of silicon.

14. The final substrate according to claim 12 or 13, wherein the dielectric layer is made of silicon oxide.

15. The final substrate according to one of claims 12 to 14, having a total length of planes or lines of dislocations, measured by deflectometry, of less than 20 mm.