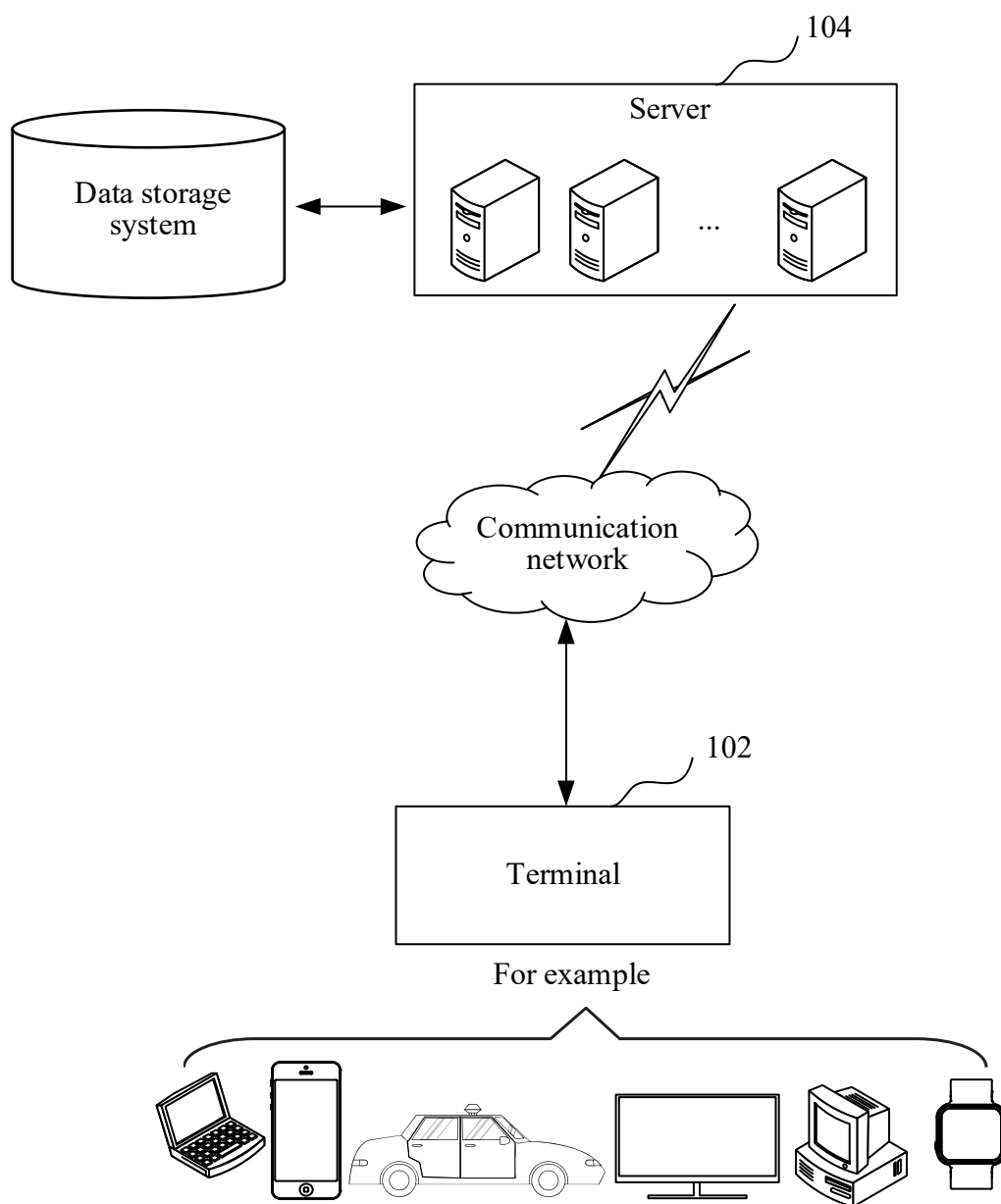




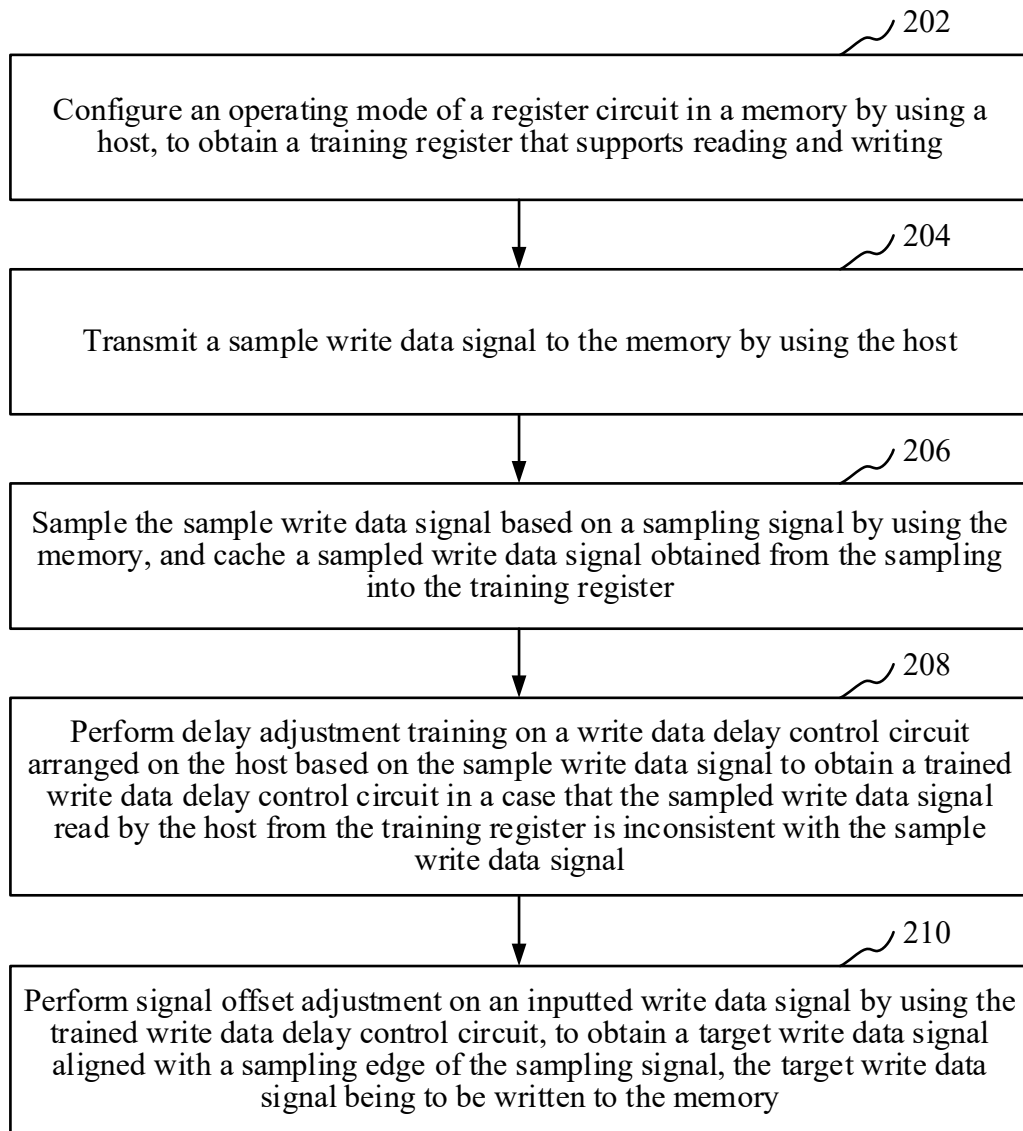


FIG. 2

Function	Data bit width	Functional description
Bus data	128 bits	Write data bus signal of memory
Mask data	16 bits	Mask signal for write data
Bus inversion data	16 bits	Data bus inversion signal

FIG. 3

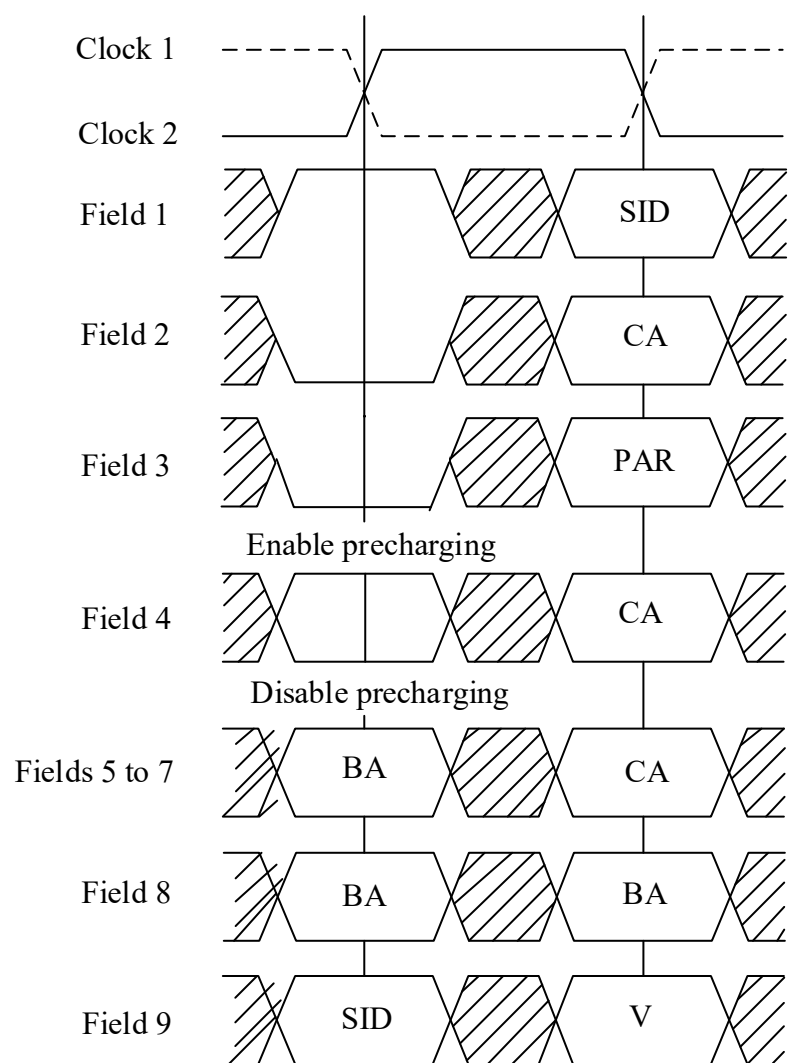


FIG. 4

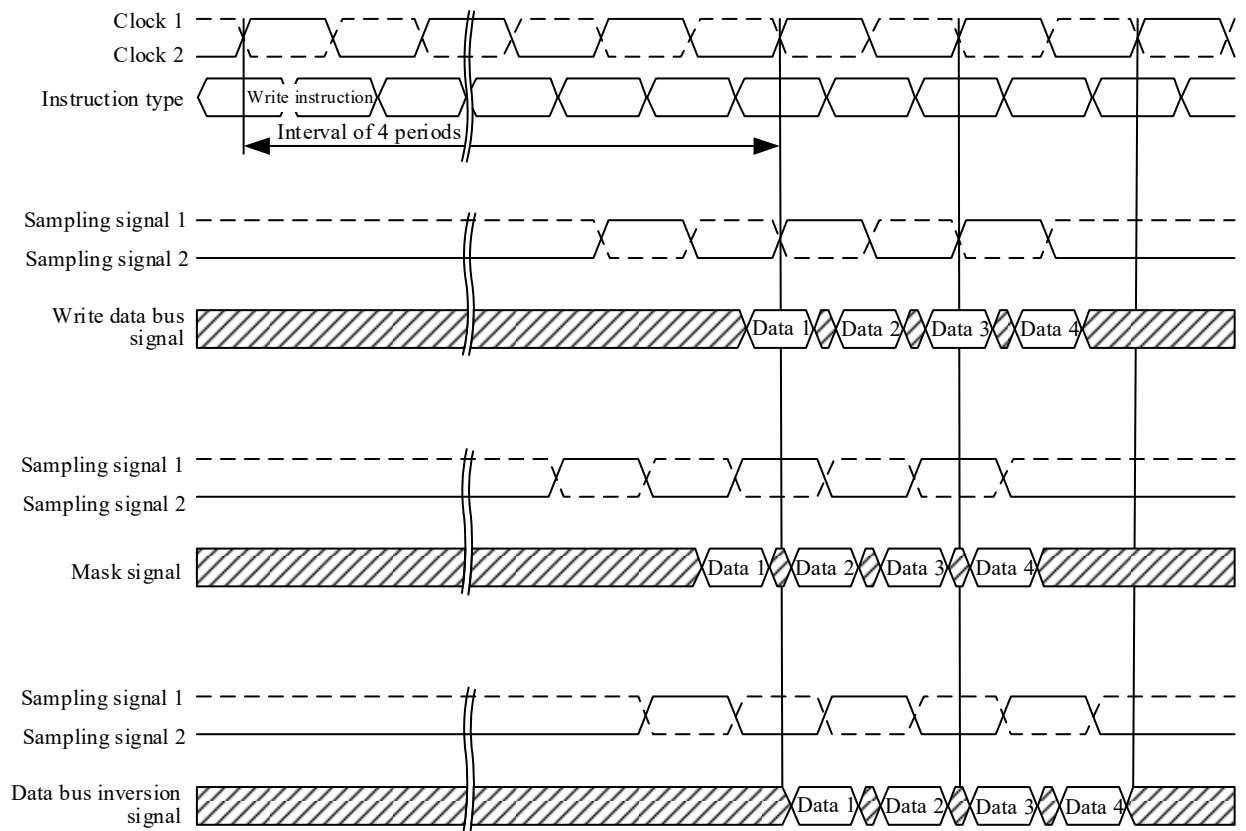


FIG. 5

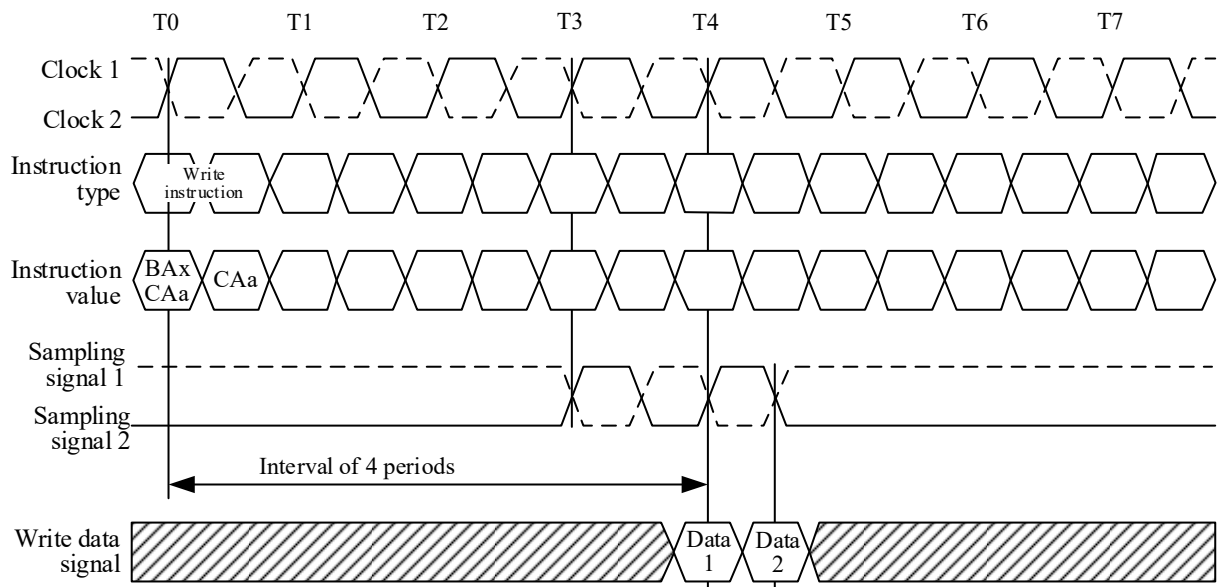


FIG. 6

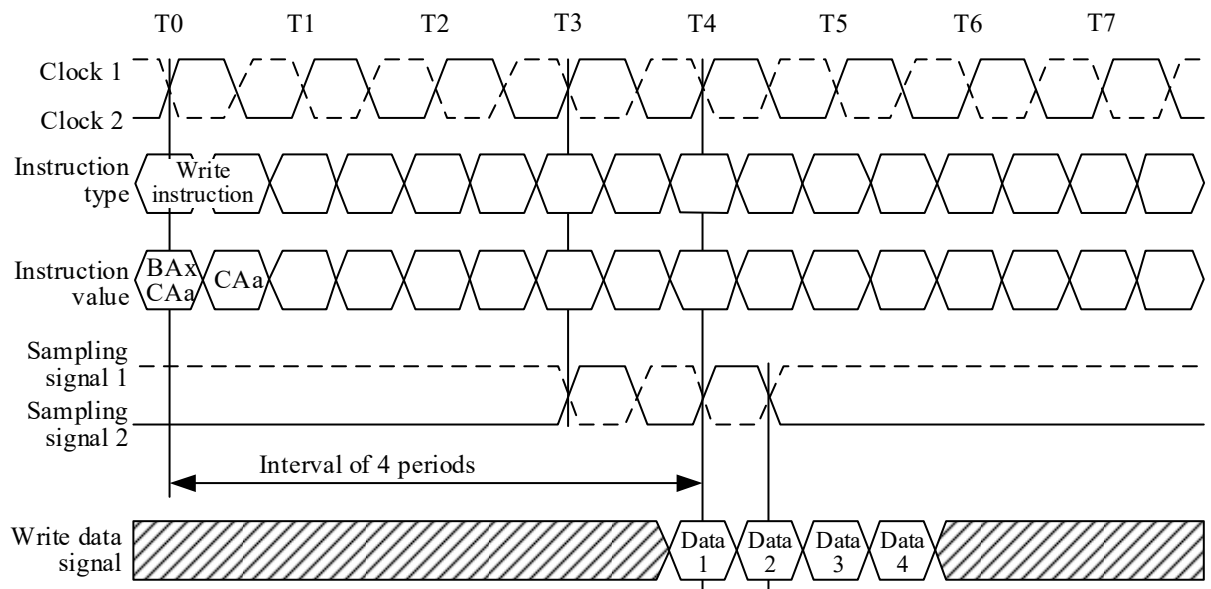


FIG. 7

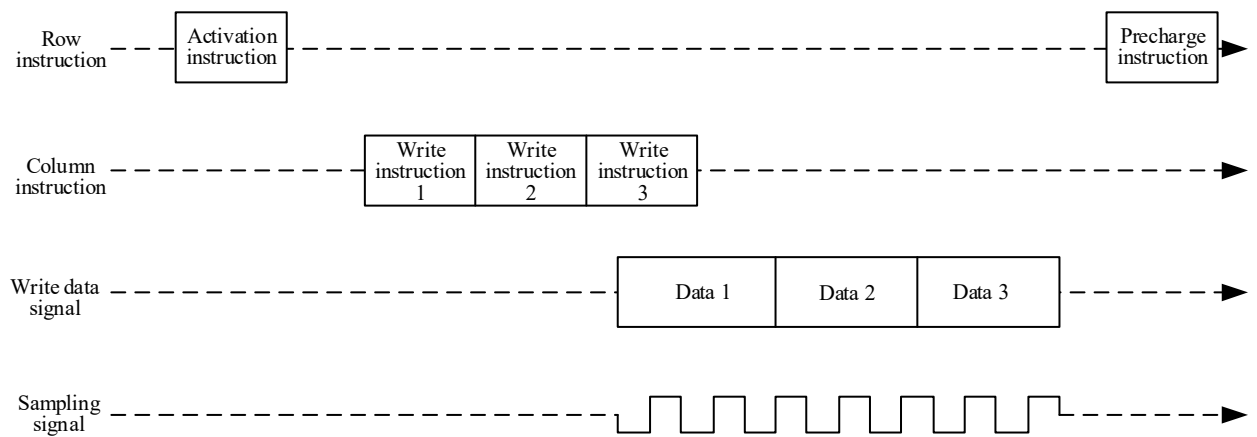


FIG. 8

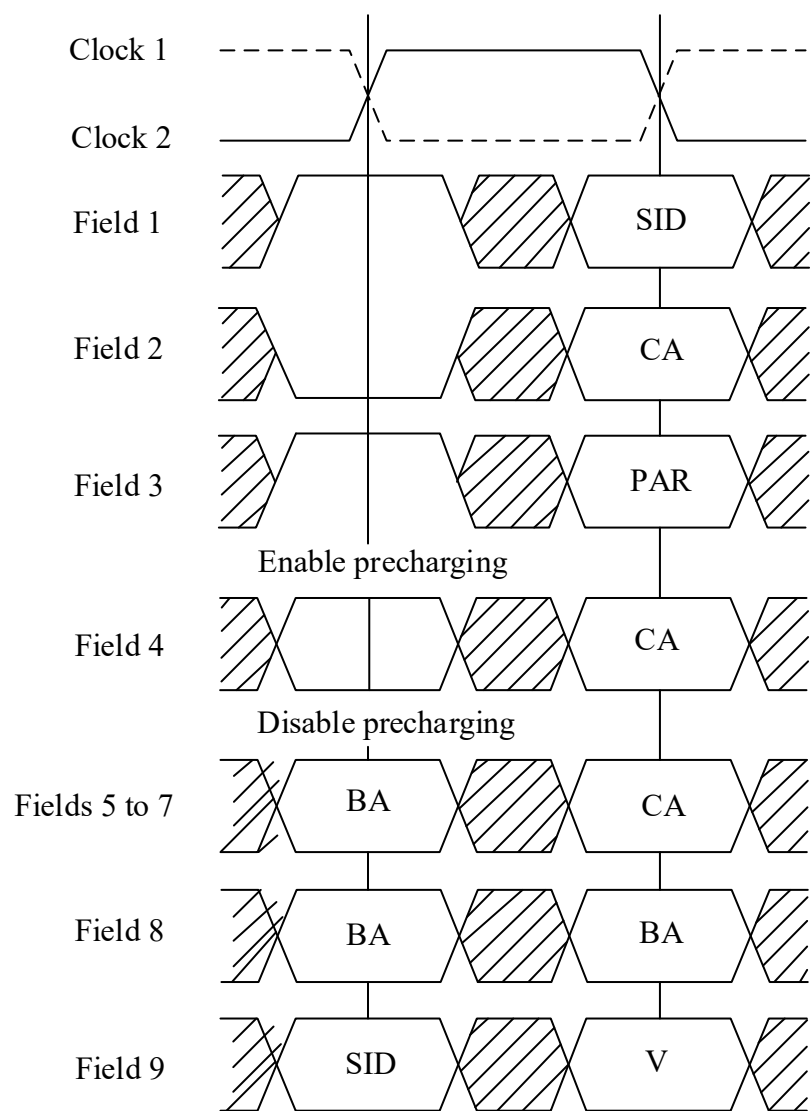


FIG. 9

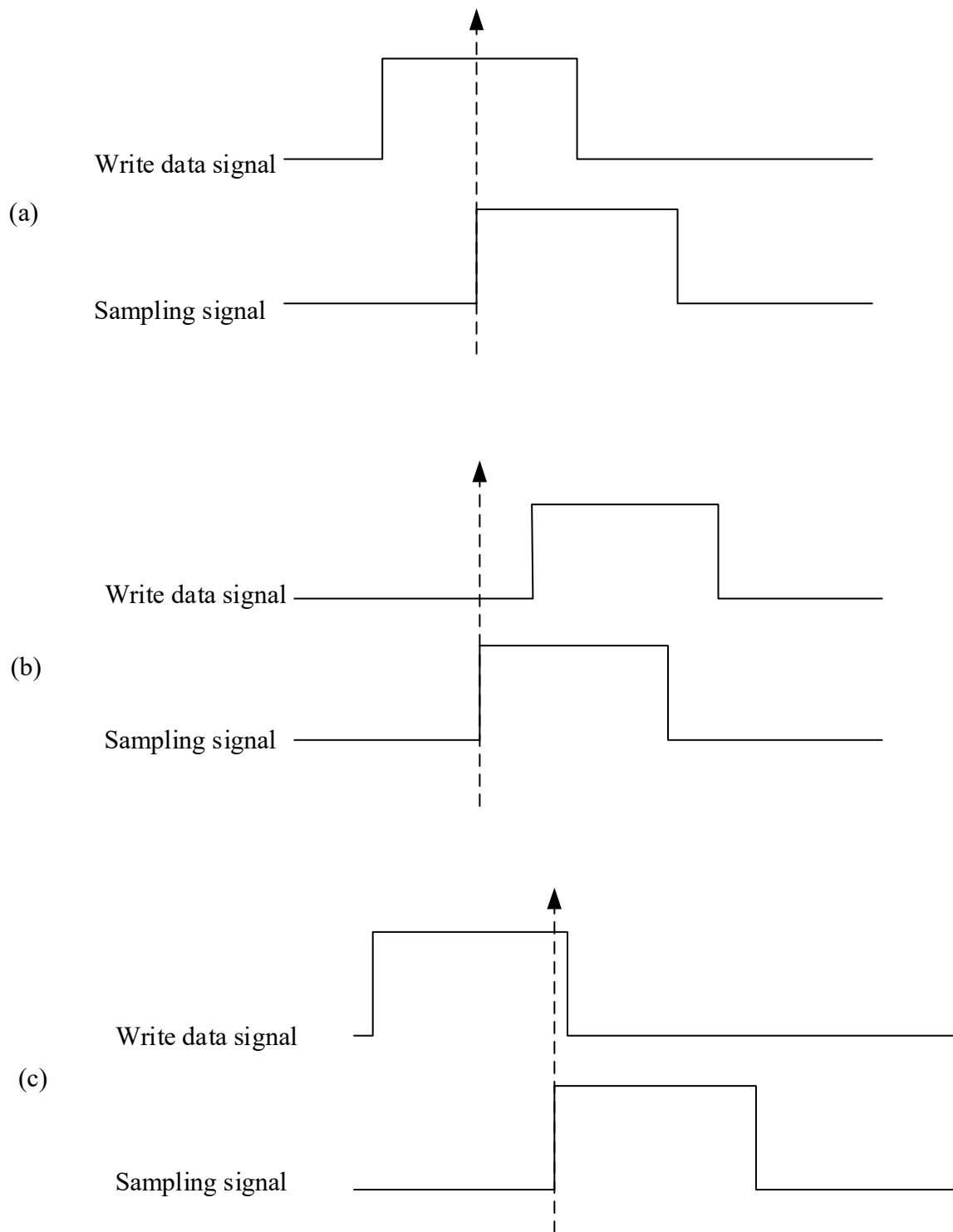


FIG. 10

Domain	Bit	Description
CATTRIP pin	8 th bit	0-Clear the CATTRIP pin (default) 1-Set the CATTRIP pin to "1"
Reserved	7 th bit	0
Data word multi-input shift register control	4 th bit to 6 th bit	Used only when the 1 st bit is enabled 000-Preset Data word multi-input shift register is set to 0xAAAAh, and data word linear feedback shift register_compare_flag bit is set to all zeros. 001-Linear feedback shift register mode (read direction) 010-Register mode (read-write direction), in which content written by a data word is directly sampled into the multi-input shift register without compression, and the content of the multi-input shift register is updated to the latest written data. 011-Multi-input shift register mode (write direction) 100-Linear feedback shift register comparison mode (write direction).
Data word read multiplexer control	2 nd bit to 3 rd bit	Used only when the 1 st bit is enabled 00-Reserved 01-Return data from a multi-input shift register (default) 10-Return data from a receiving path sampler 11-Return linear feedback shift register_compare_flag bit (optional)
Data word self-loop test	1 st bit	0-Disable (default) 1-Enable, enable a link test circuit mode. All write data (or read data) are to be written to the multi-input shift register (or read from the multi-input shift register) (that is writable/readable without any additional activation - a column address is ignored in this mode).

FIG. 11

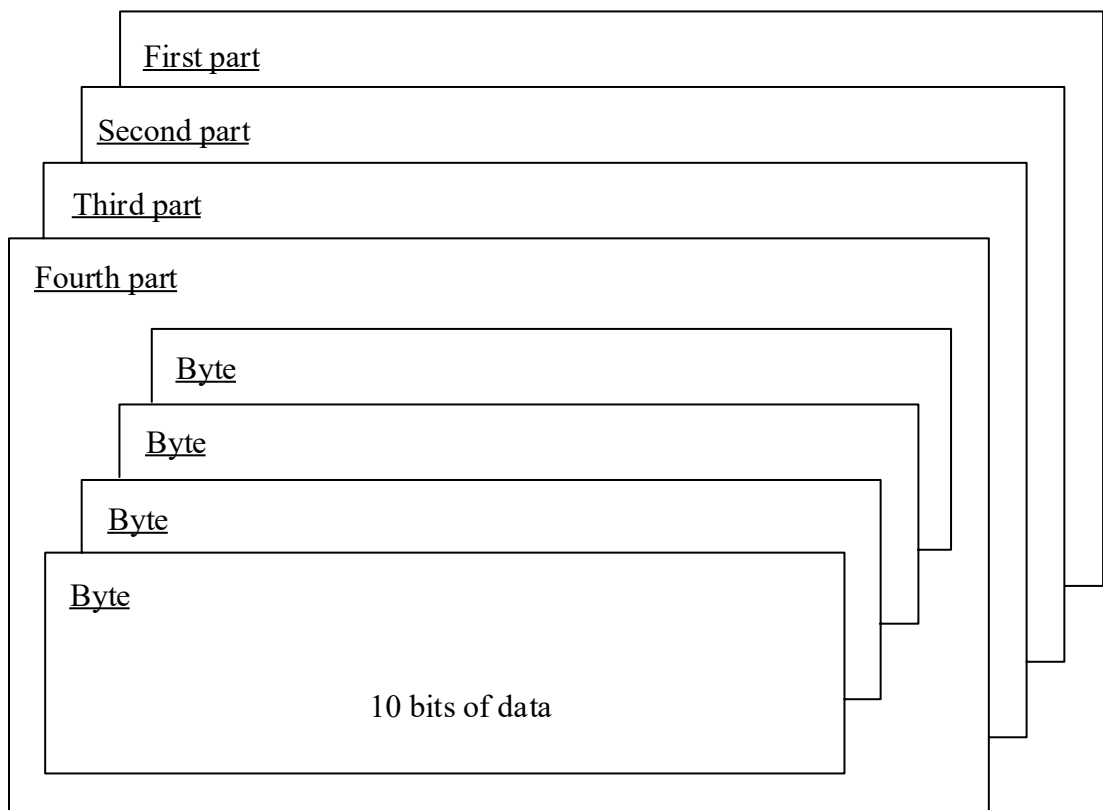


FIG. 12

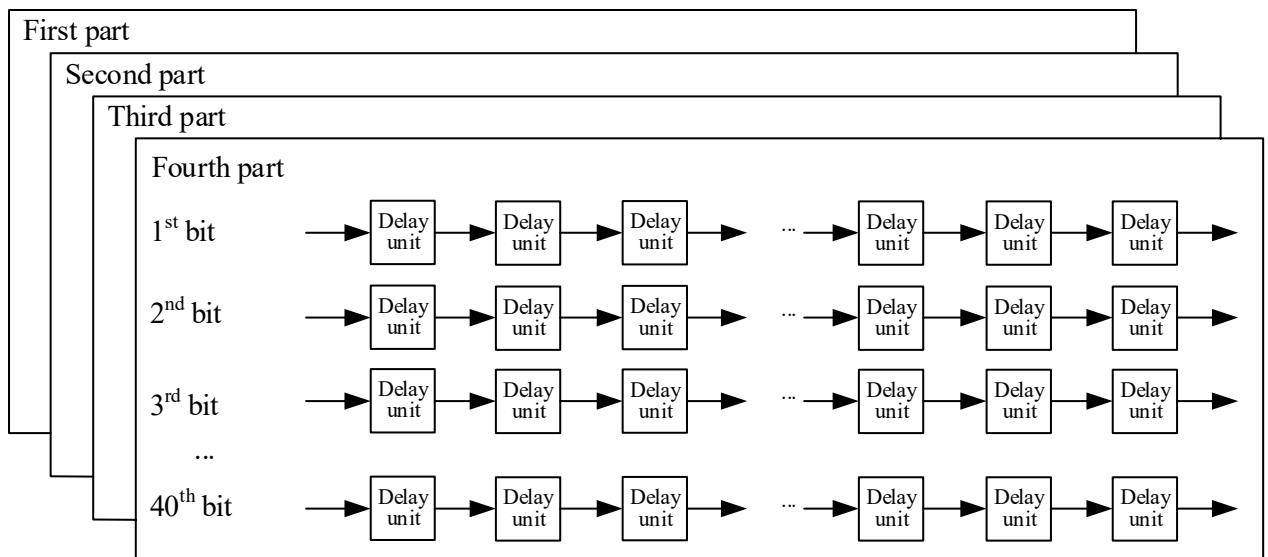


FIG. 13

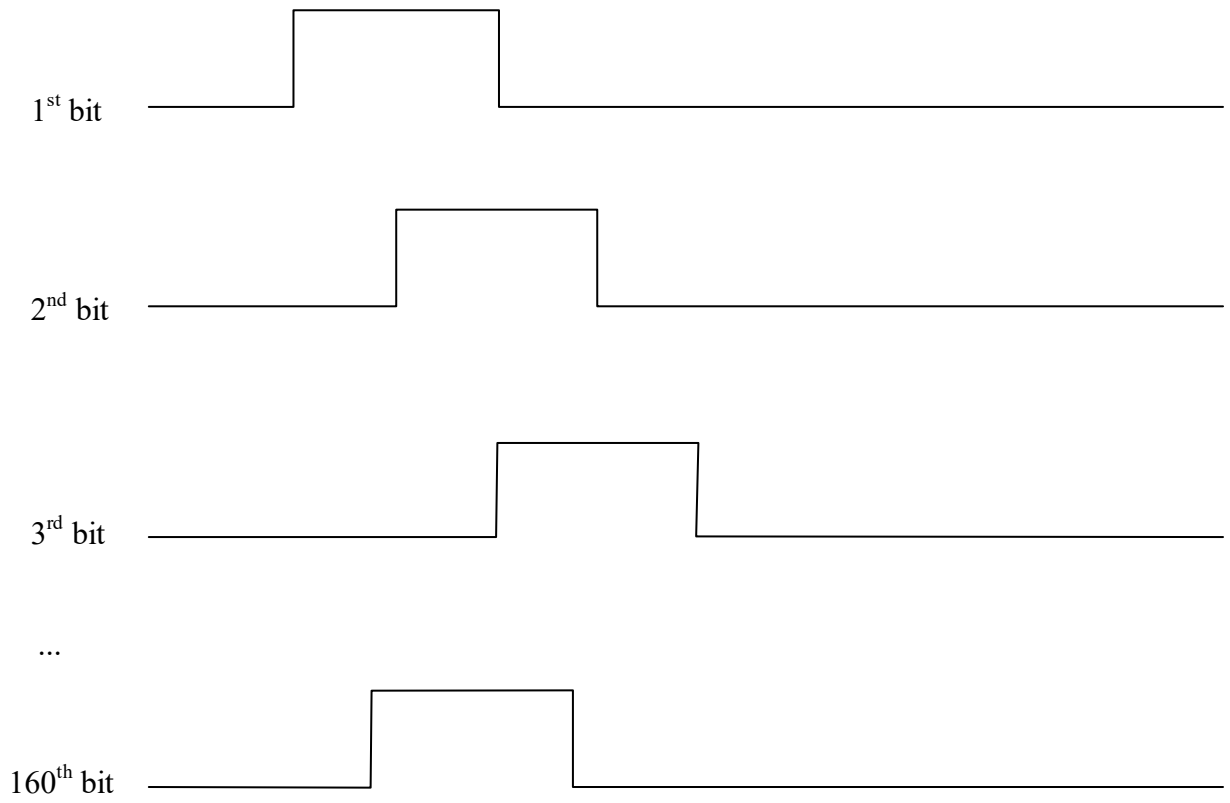


FIG. 14

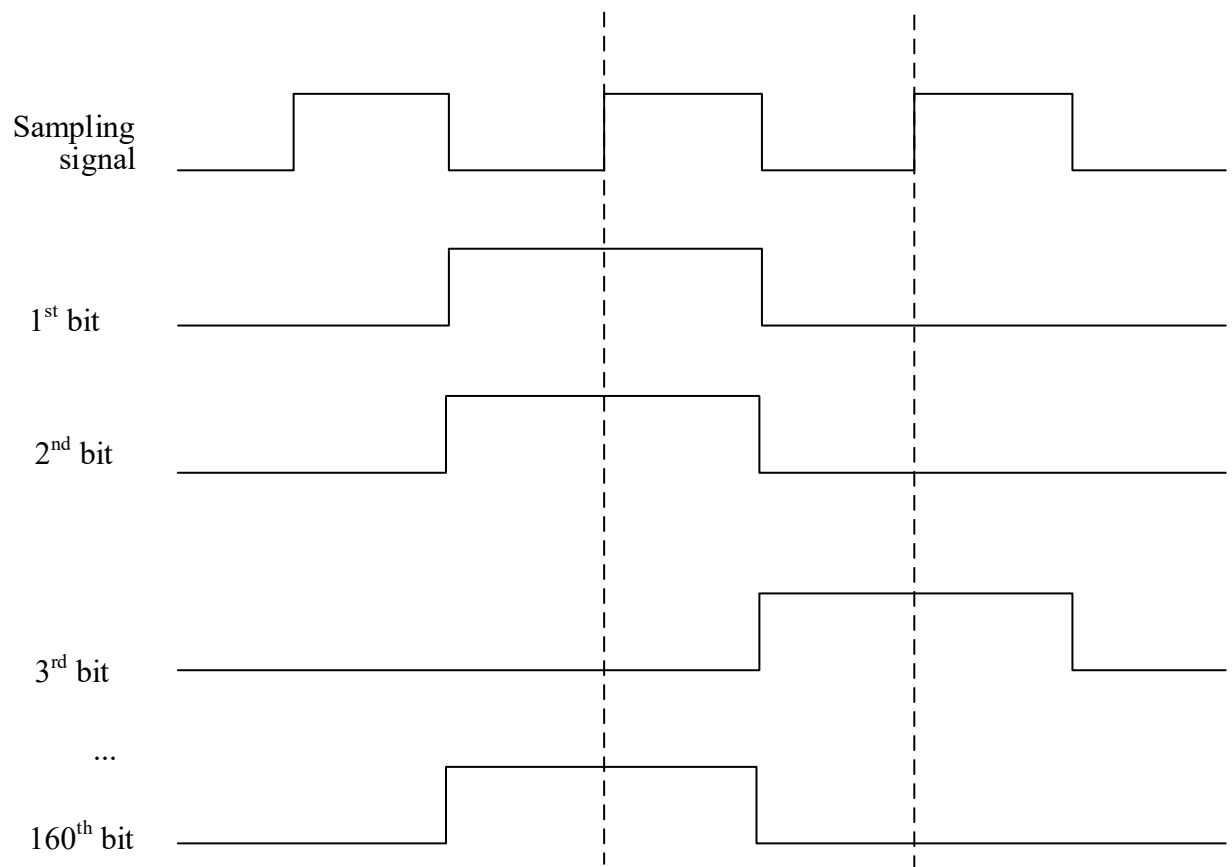


FIG. 15

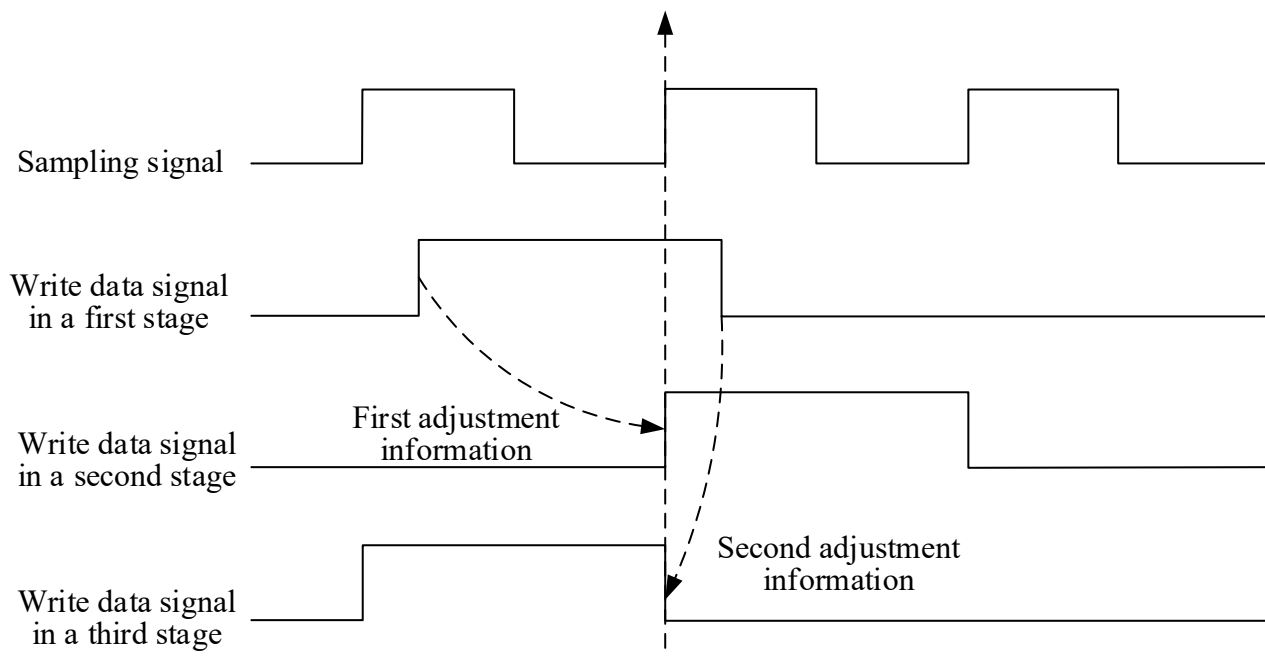


FIG. 16

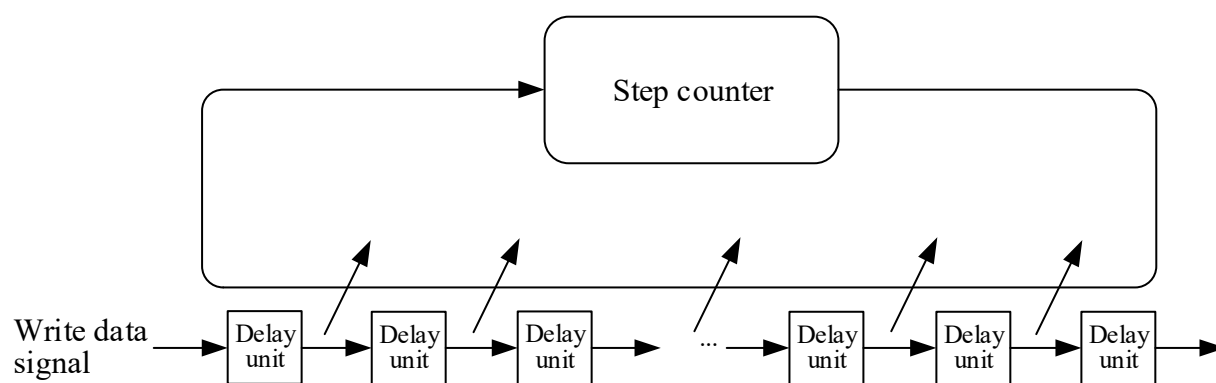


FIG. 17

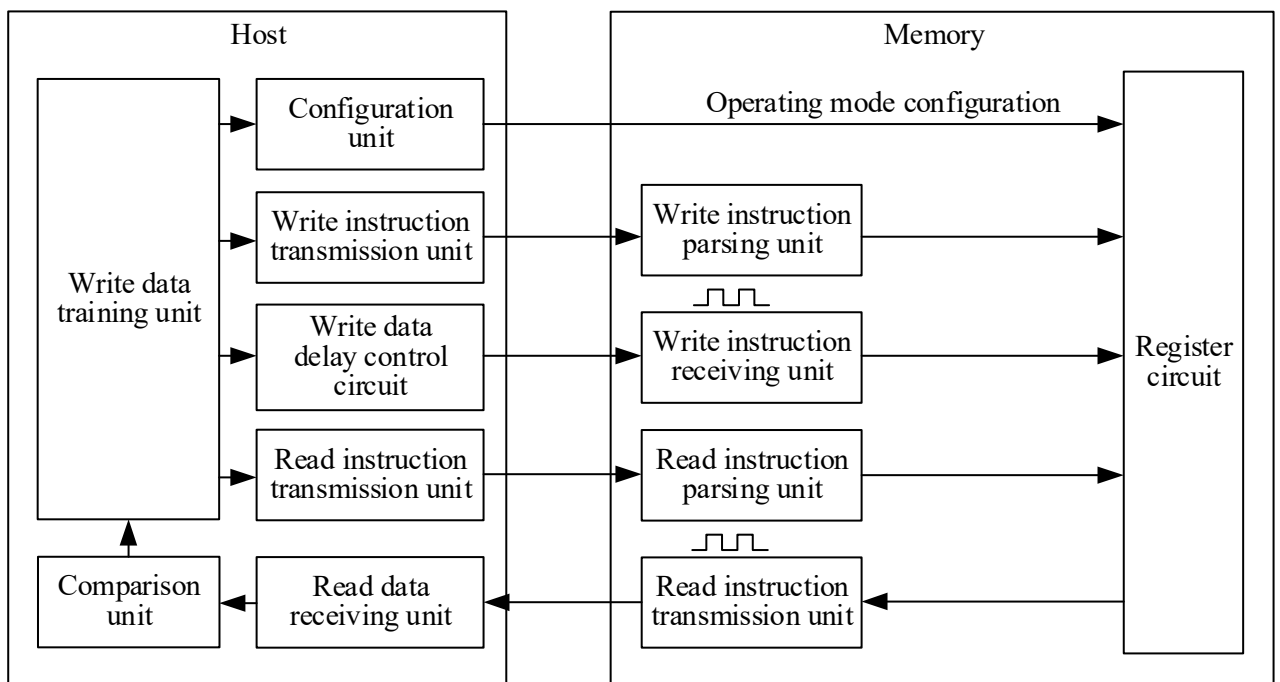


FIG. 18

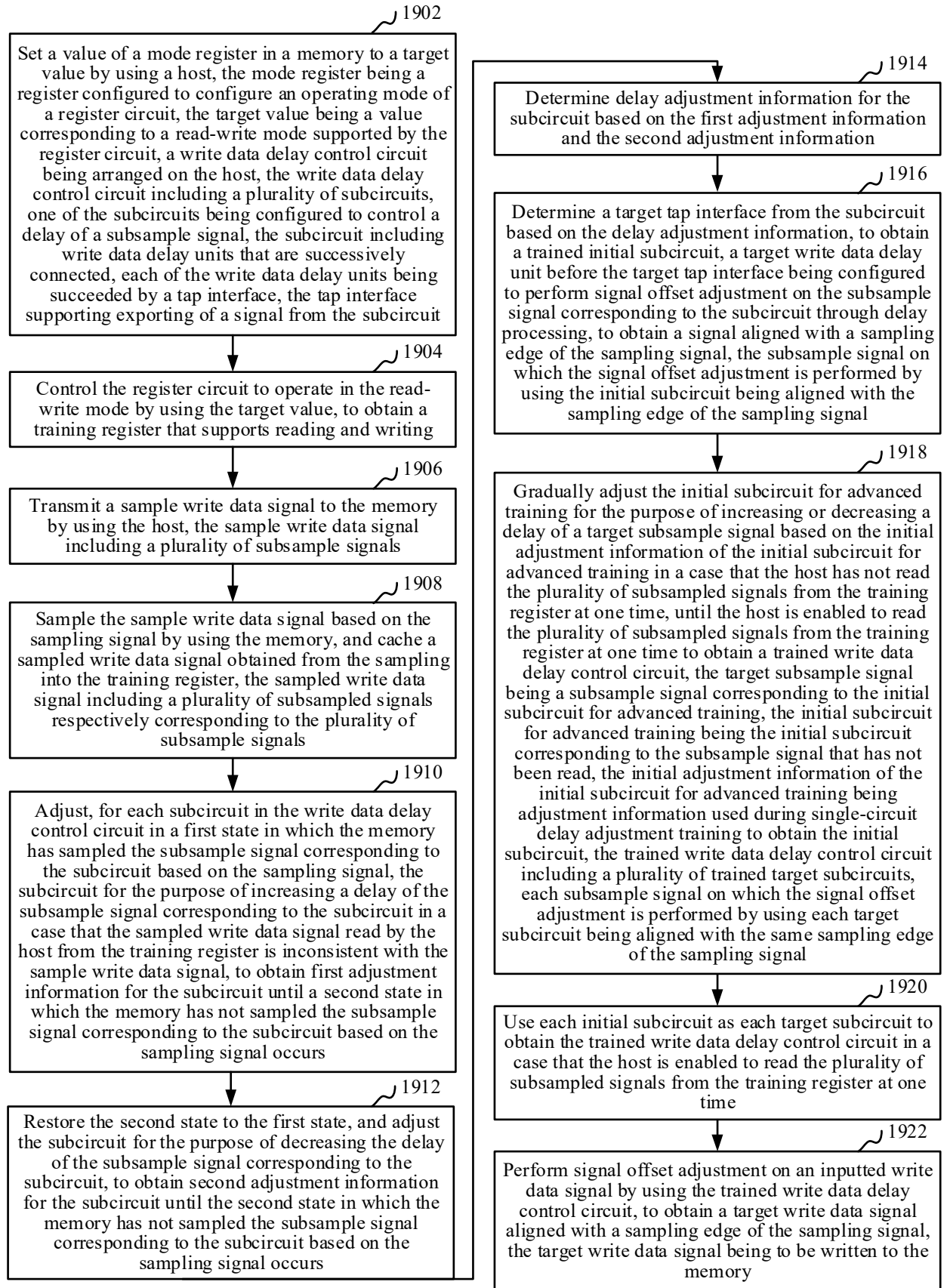


FIG. 19

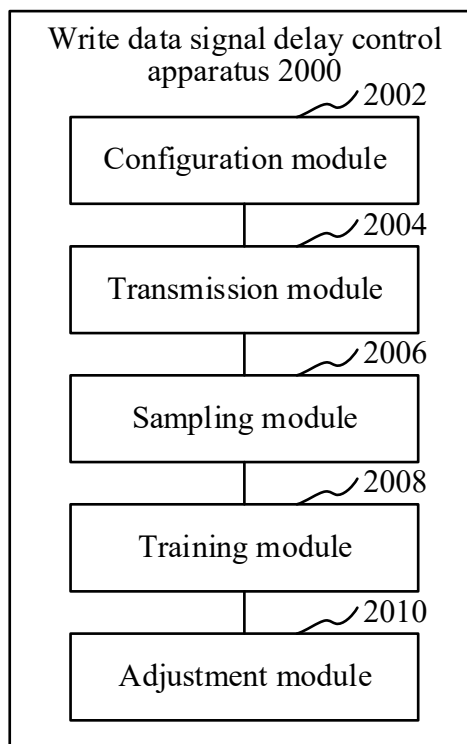


FIG. 20

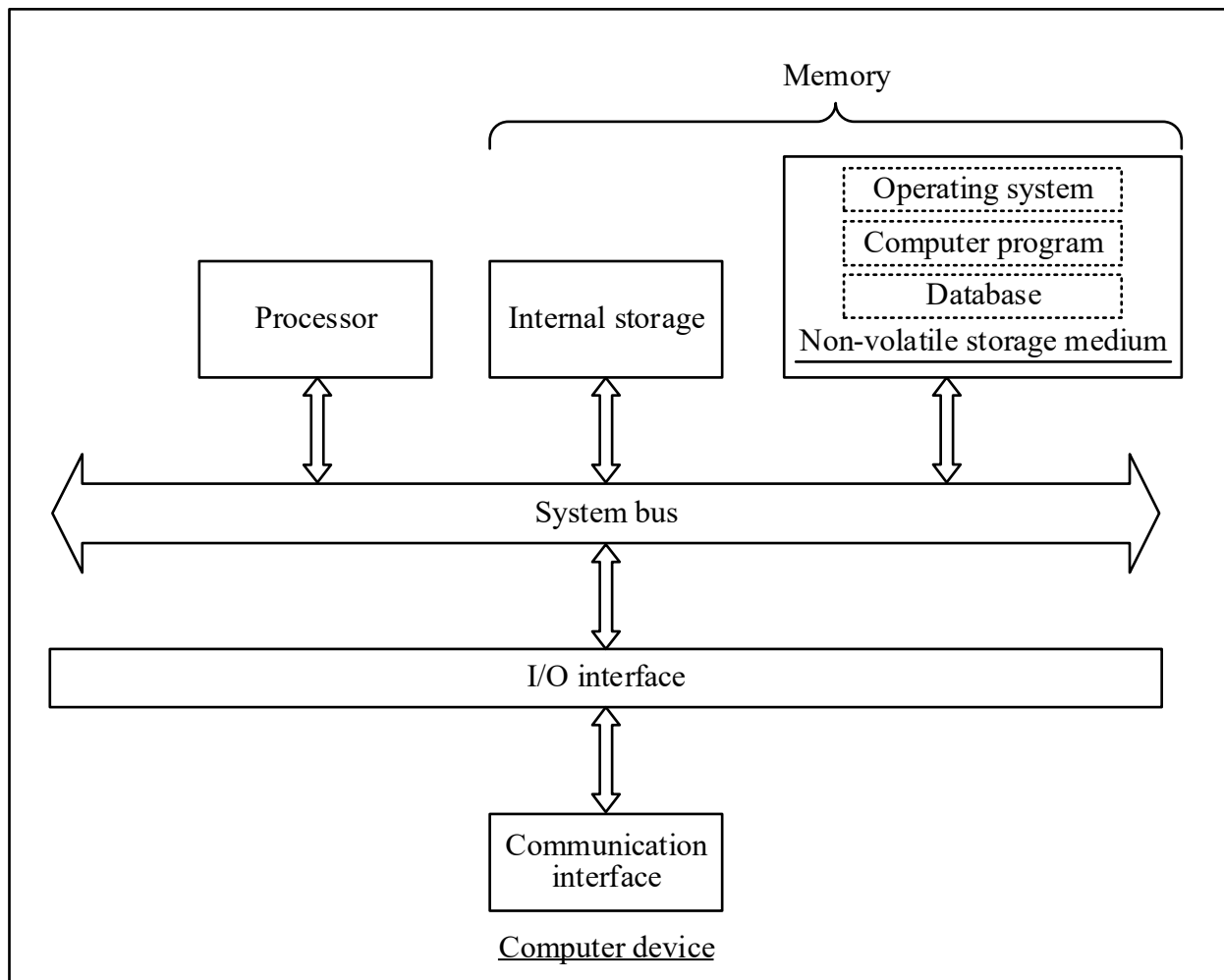


FIG. 21

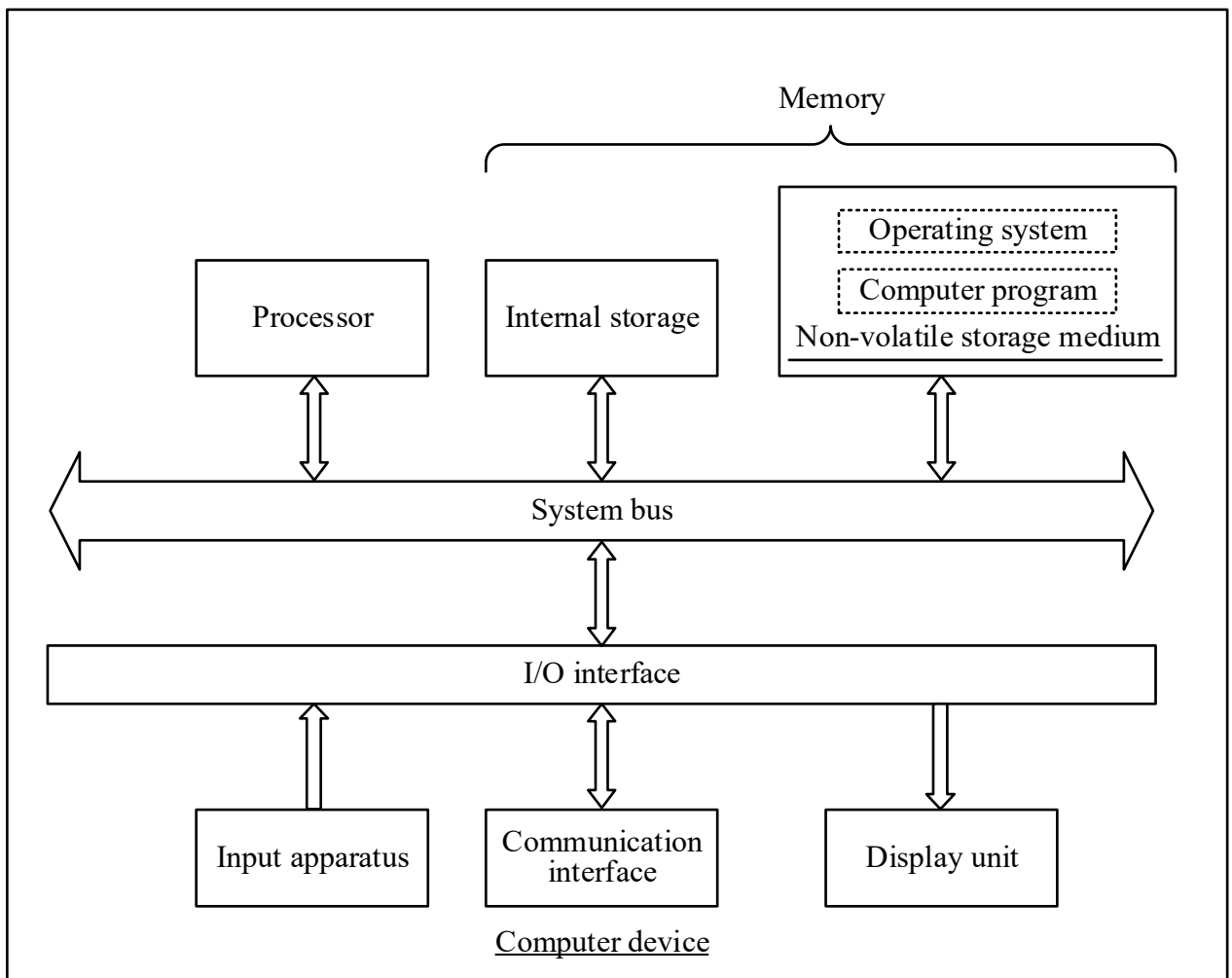


FIG. 22