

TITLE OF THE INVENTION:

THIN FILM TRANSISTORS WITH POLY(ARYLENE ETHER) POLYMERS AS
GATE DIELECTRICS AND PASSIVATION LAYERS

This application claims the benefit of Provisional Application No. 60/810,534, filed June 02, 2006. The disclosure of this Provisional Application is incorporated by reference.

CROSS-REFERENCE TO RELATED APPLICATIONS

- 5 **[0001]** The subject matter of the instant invention is related to U.S. Patent No. 6,716,955; the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

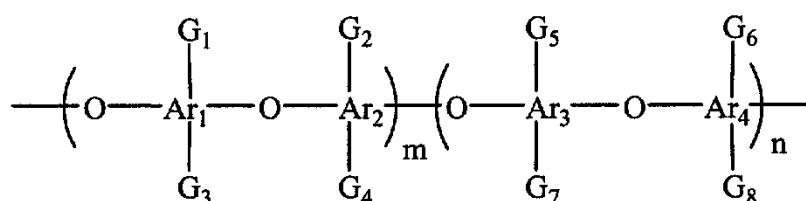
- 10 **[0002]** This invention relates to the use of poly(arylene ether) polymers, and more particularly to the use of grafted functional groups onto the backbone of poly(arylene ether) polymers, to provide cross-linkable polymers with a range of glass transition temperatures and low moisture uptake having particular utility as gate dielectric layers in multilayer electronic devices such as thin film transistors. The invention also relates to methods for applying the polymers in order to form thin film transistors (TFT).
- 15 **[0003]** The electronics industry is seeking gate dielectric materials for use in fabricating multilayer electronic devices such as thin film transistors at low temperatures, particularly for printed transistors. However, the need for materials compatibility, processability, and good electrical properties over a wide range of conditions and deposition techniques and temperatures has presented a significant problem. This problem has been a very difficult
- 20 one to solve for polymers since the desired temperature for their use in flexible or lightweight transistors (i.e. cure) is below 400°C and more preferably below about 180°C.
- 25 **[0004]** Therefore, there is a need in the multilayer electronic device fabrication industry for the replacement of silicon nitride-based gate dielectric materials with materials of lower processing temperatures that may be deposited via solution casting techniques such as spin-coating, slot extrusion, or printing. Silicon nitride and its modified versions are typically processed at temperatures greater than 300°C and are typically deposited

- via chemical vapor deposition techniques. While polymeric materials have been discussed as replacements for silica as interlayer dielectrics (ILDs), shallow trench isolation (STI) materials, or stop layer dielectrics (SLDs), they have not traditionally been reported to be used as gate dielectrics due to their lack of hydrophobicity or their inability to crosslink at low temperatures. In particular, polymeric systems such as the ones of the invention described below have not been employed as gate dielectrics that are resistant to solvents, that may be printed or slot extruded, are processable at or below 180°C, and give electrical properties needed in a gate dielectric. Many of the polymers that have been tested as gate dielectric materials for thin film transistors lack the hydrophobicity need to avoid moisture absorption and the ability to withstand contact with other solvents that may be used in depositing subsequent layers and that may damage the gate dielectric layer. Thus, a gate dielectric material that meets that criteria above combined with the cross-linking needed to give good solvent resistance is desirable.
- 15 **[0005]** Past attempts to crosslink poly(arylene ethers) utilized various high temperature crosslinking groups to give high T_g polymer and this chemistry may be used as an intra- or interlayer dielectric material for amorphous silicon or low temperature poly-silicon thin film transistors. A detailed summary of these chemistries is provided in U.S. Patent No. 6,060,170; hereby incorporated by reference This patent teaches using
- 20 poly(arylene ether) polymer compositions having aromatic groups grafted on the poly(arylene ether) backbone, which grafts allow for crosslinking of the polymers in a temperature range of 200 to 450°C. A further reduction in crosslinking temperature would, however, be desirable for dielectric and passivation materials for thin film transistors on flexible substrates or organic thin film transistors.
- 25 **[0006]** Display and imaging backplane or thin film transistor manufacturing require suitable coatings, especially gate dielectric insulating layers. These layers can have low or high dielectric constants and are required to have low leakage current values, good solvent resistance, and low moisture absorption. In addition, it is desired to provide the solutions that form these layers with unlimited storage stability at 25°C, storage stability
- 30 at 40°C sufficient to weather transportation in non-refrigerated vehicles, and cure temperatures of 130 to 180°C or below 300°C. After cure, it is desirable to have solvent resistance, a dielectric constant below 3.5, and low moisture absorption.

[0007] All references cited herein are incorporated herein by reference in their entireties.

BRIEF SUMMARY OF THE INVENTION

- 5 [0008] The instant invention solves problems associated with conventional materials by providing a poly(arylene ether) polymer as a passivation or gate dielectric layer in thin film transistors, and methods for applying the layer or film in TFTs. This poly(arylene ether) polymer includes polymer repeat units of the following structure:



- 10 where Ar_1 , Ar_2 , Ar_3 , and Ar_4 are identical or different arylene radicals, m is 0 to 1, n is 1- m , and where G_{1-8} are individually : H, alkyl, alkylene, or functionalized alkylene, or the radicals represented by Figure A below:

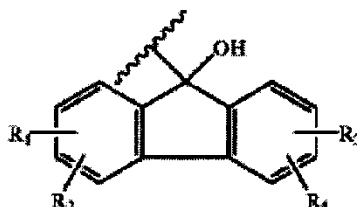
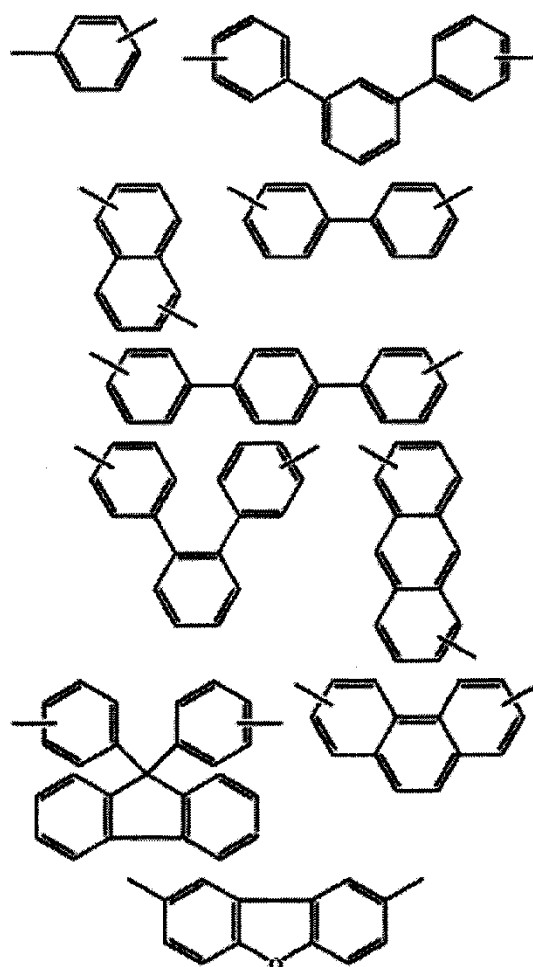


Figure A

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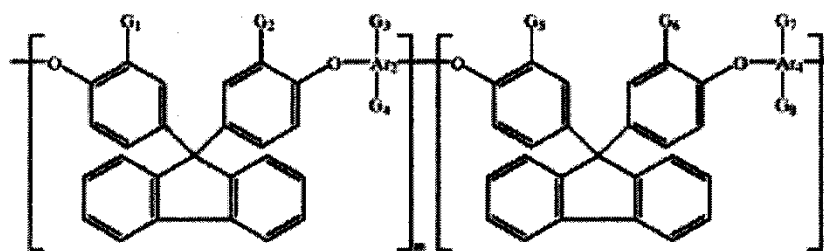
or mixtures thereof, wherein Z is the average number of G radicals per repeating unit of said polymer and Z is in the range of 0.1 to 4.0, where R_1 , R_2 , R_3 , R_4 are individually H, alkyl, or alkoxy radical, wherein the alkoxy radical can have a normal or branched alkyl radical of C_{1-8} .

- 20 [0009] In one aspect of the invention, the poly(arylene ether) polymer consists essentially of non-functional repeating units wherein Ar_1 , Ar_2 , Ar_3 , Ar_4 are individually arylene radicals selected from the consisting of:



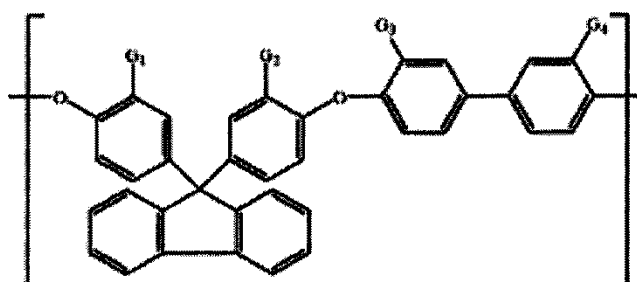
and mixtures thereof, but Ar_1 and Ar_2 or Ar_3 and Ar_4 , other than the diradical 9,9-diphenylfluorene, are not isomeric equivalents. In some cases, the grafted polymer has repeating units of a structure:

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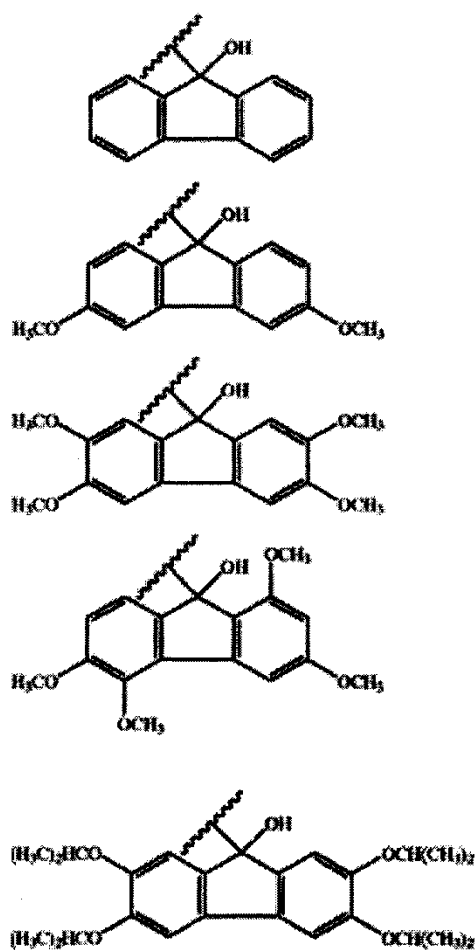
[0010] The grafted polymer can comprise a repeating polymer unit:

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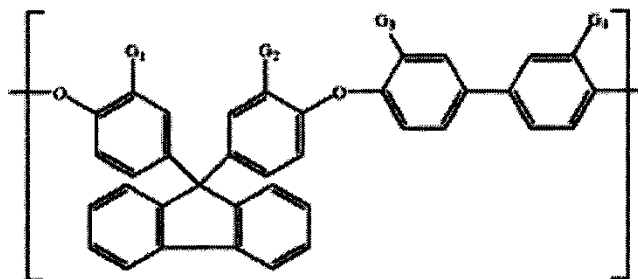


wherein grafts G_{1-4} are individually selected from the group consisting of : H, alkyl, alkylene, functional alkylene, or the radicals represented below:

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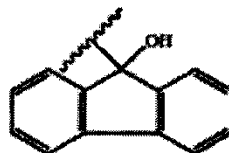


and mixtures thereof, where Z is the average number of G radicals per polymer unit and Z is in the range of 0.1 to 4.0. The grafted polymer can comprise a repeating polymer unit:



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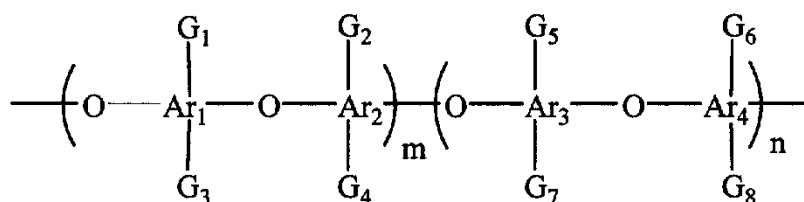
wherein G_{1-4} are individually H, alkyl, alkylene, functional alkylene or:



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where Z is the average number of G radicals per polymer unit and Z is in the range of 0.1 to 4.0.

[0011] Also provided is an optional grafted poly(arylene ether) polymer for use as a passivation or gate dielectric layer for thin film transistors where each of the aryl radicals of the polymer repeat units is grafted to two unsaturated groups, G, as shown in the structure:



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where $G_1, G_2, G_3, G_4, G_5, G_6, G_7,$ and G_8 are identical or different non-aromatic unsaturated groups and these groups are adapted to crosslink at a curing temperature below 200°C without producing volatiles during curing and without providing functional groups after curing.

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[0012] The average number of unsaturated groups G per polymer repeat unit is 0.1 to 4.0. This average is calculated as the total number of unsaturated groups G per polymer divided by the total number of polymer repeat units per polymer.

5 [0013] Further provided is a gate dielectric or passivation composition for thin film transistor fabrication comprising the polymer, and optionally, a diluent, which does not afford a functional group or interfere with the mechanical or electrical properties of the composition.

10 [0014] Still further provided is a method for providing a gate dielectric substrate with a poly(arylene ether) film having a crosslinking temperature from about 130°C to about 180°C, a dielectric constant below 3.5, a maximum moisture absorption of less than about 0.2 wt%. The method comprises applying the polymer of the invention to the gate dielectric substrate via either spin coating, slot extrusion, or printing and heating the polymer to a curing temperature at or below about 300°C or usually, below about 250°C, or, , below about 180°C.

15 [0015] Further provided is a multilayer electronic device that contains a film of grafted poly(arylene ether) polymer as the gate dielectric and/or passivation layer.

[0016] Still further provided is a thin film transistor device that contains a film of grafted poly(arylene ether) polymer as the gate dielectric and/or passivation layer.

20 [0017] Also provided is a printed thin film transistor device that contains a film of grafted poly(arylene ether) polymer as the gate dielectric and/or passivation layer.

[0018] The invention also relates to gate dielectric compositions (cured and uncured) comprising at least one polymer of the invention. The compositions, like the polymers themselves, can be useful as gate dielectrics and passivation layers. In addition to the at least one polymer, the compositions can further contain additional ingredients, including
25 but not limited to, at least one solvent, one reactive solvent or diluent, at least one surfactant or at least one inorganic filler. Such compositions can be applied onto a substrate by any suitable method such as spin coating, printing, among other methods.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

30 [0019] The invention will be described in conjunction with the following drawings which are not intended to limit the invention but to serve as representative examples wherein:

[0020] Figure 1 is a drawing of a one embodiment of a multilayer electronic device that comprises a bottom gate thin film transistor containing the gate dielectric film of the invention.

5 [0021] Figure 2 is a drawing of a second embodiment of a multilayer electronic device that comprises a bottom gate thin film transistor containing the film of the invention.

[0022] Figure 3 is a drawing of a third embodiment of a multilayer electronic device that comprises a top gate thin film transistor containing the film of the invention.

DETAILED DESCRIPTION OF THE INVENTION

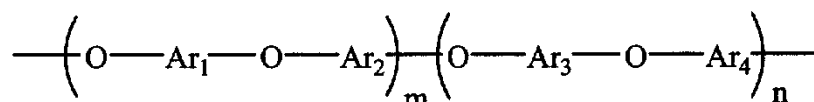
10 [0023] The aforementioned drawbacks of the prior art are overcome by utilizing a polymer with the capability of being processed at low temperatures and exhibiting the other characteristics of a gate dielectric layer or passivation material for thin film transistors. The term "gate dielectric layer" is defined as a horizontally oriented insulating film or layer that is positioned between a horizontally oriented gate electrode
15 and a horizontally oriented semiconductor layer such as shown in Figures 1-3. The gate dielectric layer can be in direct contact with at least one of the gate electrode and semiconductor layer, or at least one other layer can be positioned between the gate dielectric layer and at least one of the gate electrode and semiconductor layer.

[0024] The polymer of the invention is prepared by grafting onto poly(arylene ether)
20 polymers either unsaturated or saturated groups (i.e., grafts (G)), which can crosslink at a curing temperature of less than 300°C, or usually below 250°C, or below about 180°C. The invention thus relates to specific poly(arylene ether) polymers and compositions containing them, their use as gate dielectrics and passivation layers, a microelectronic device comprising the same, a method of applying the polymers, and a gate dielectric or
25 passivation layer comprising such poly(arylene ether) polymers, optionally in combination with a solvent or a reactive diluent. Curing can be accomplished by heating or by UV irradiation or a combination of the two.

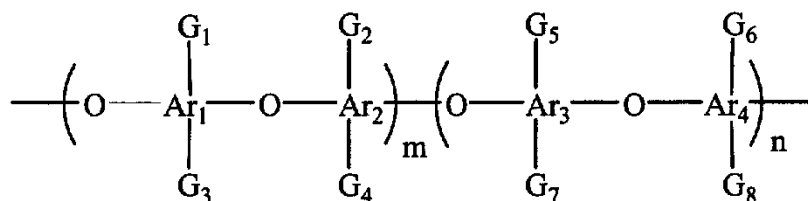
[0025] The invention also relates to gate dielectric compositions (cured and uncured) comprising at least one polymer of the invention. The compositions, like the polymers
30 themselves, are useful as gate dielectric or passivation layers. In addition to the at least one polymer, the compositions can further contain additional components, including but not limited to, at least one solvent, at least one reactive solvent or diluent, at least one

plasticizer, at least one surfactant, or at least one inorganic filler. Such compositions can be applied onto a substrate by any suitable method such as spin coating, slot extrusion, printing, among other methods.

- 5 [0026] Polymers of the invention can comprise polymer repeat units represented by the following structure:



- 10 where Ar₁, Ar₂, Ar₃, and Ar₄ are identical or different aryl radicals, m is 0 to 1, n is 1-m, and at least one of the aryl radicals is grafted to at least one saturated or unsaturated group (G), which is not aromatic and is adapted to crosslink at a curing temperature less than about 200°C without producing volatiles during curing and without providing functional groups after curing. In certain embodiments, each of the aryl radicals of the polymer repeat units is grafted to two unsaturated groups G, as shown in the following structure:



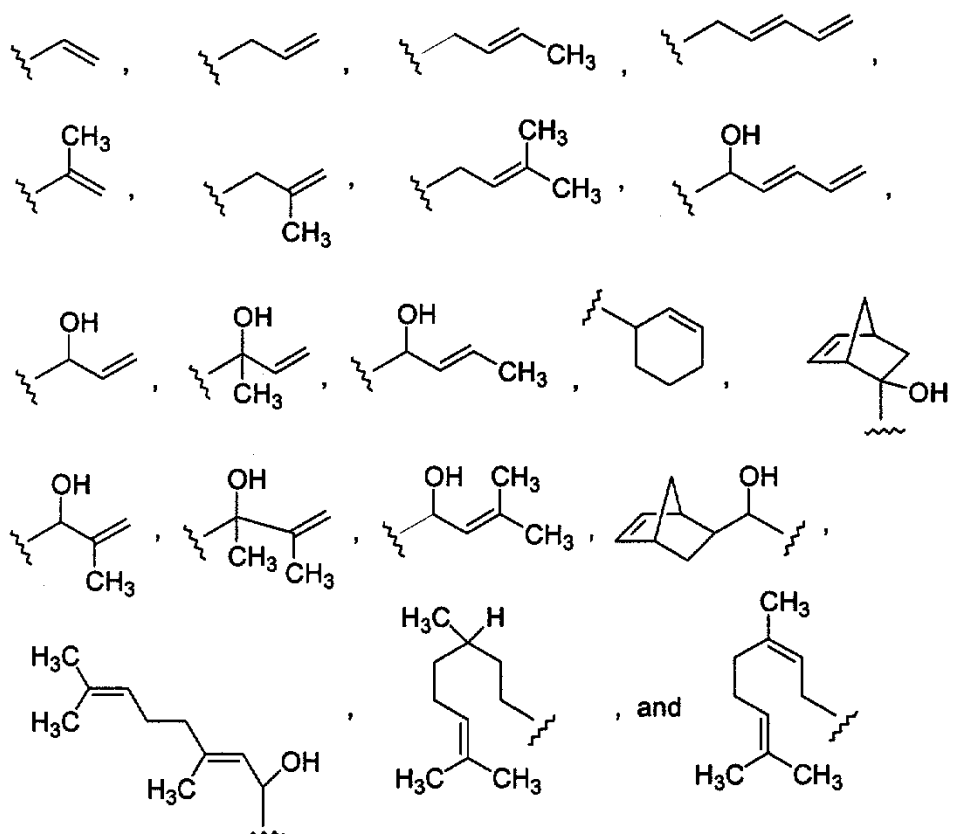
- 15 where G₁, G₂, G₃, G₄, G₅, G₆, G₇ and G₈ are identical or different unsaturated groups.

- [0027] Polymers of the invention do not necessarily consist only of these polymer repeat units (i.e., G-containing polymer repeat units). In addition to embodiments wherein the polymer is built solely from the G-containing polymer repeat units, the invention also encompasses polymers comprising other polymer repeat units in addition to the G-containing polymer repeat units, such as, e.g., poly(arylene ether) polymer repeat units lacking any unsaturated grafts (i.e., G-free polymer repeat units). The sequence in which different polymer repeat units can be combined to form the polymer of the invention is not particularly limited. Thus, polymers of the invention can be, e.g., random, alternating, or block copolymers of the different polymer repeat units.

- 25 [0028] The average number of unsaturated groups G per polymer repeat unit can range from about 0.01 to about 8.0, usually about 0.1 to about 4. This average is

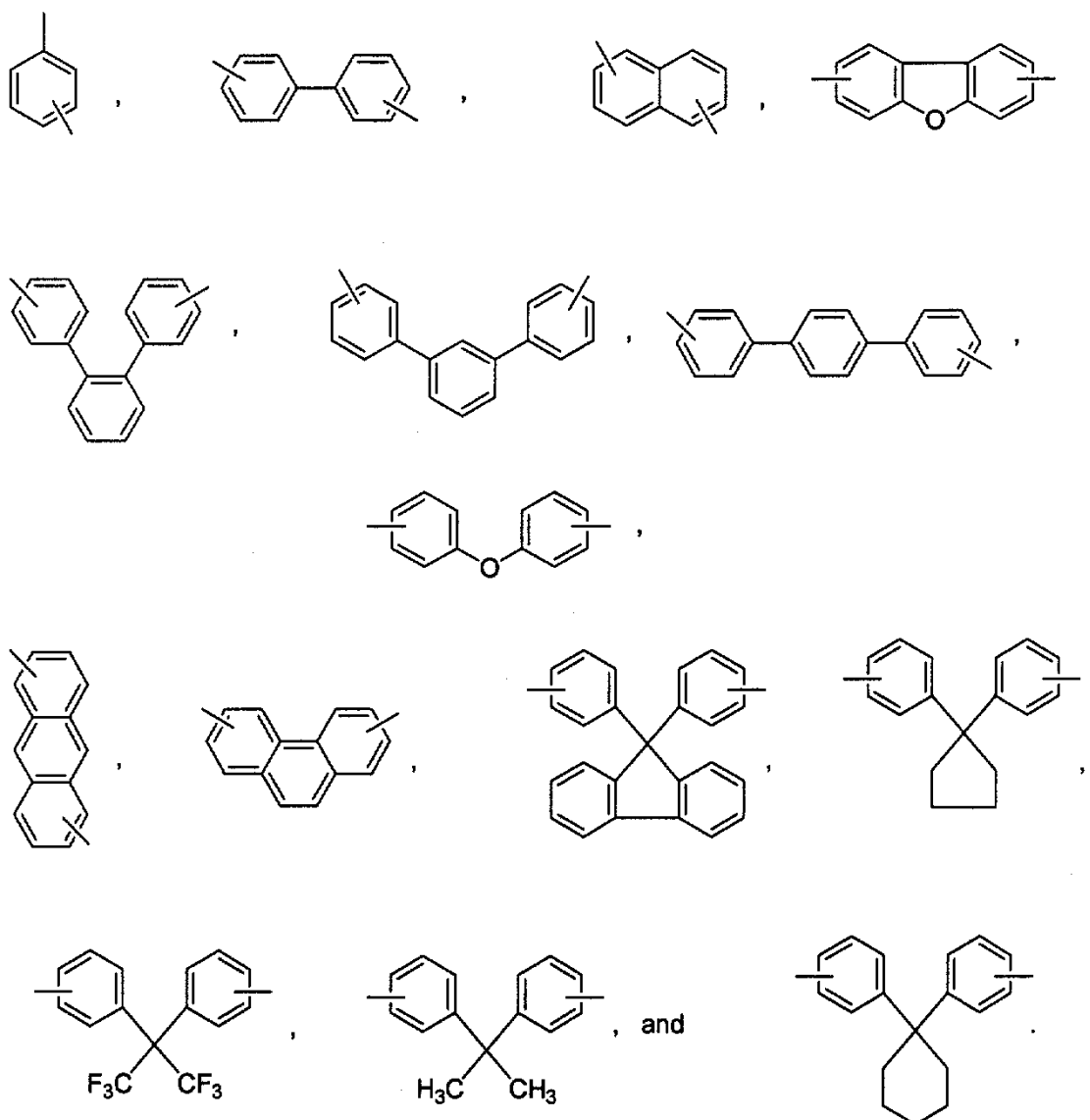
calculated as the total number of unsaturated groups G per polymer divided by the total number of polymer repeat units per polymer.

- [0029]** In one aspect of the invention, the unsaturated groups G comprise olefins independently selected from the group consisting of an alkylene radical, an alkyldiene radical, an α -hydroxyalkylene radical and an α -hydroxyalkyldiene radical. In certain embodiments, the unsaturated groups G are derived from isoprene units. The unsaturated groups G are typically independently selected from the group consisting of:



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- [0030]** In another aspect of the invention, the aryl radicals Ar_1 , Ar_2 , Ar_3 , and Ar_4 are independently selected from the group consisting of:

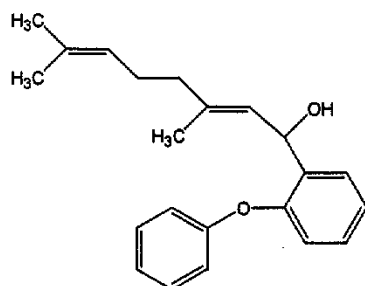


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[0031] Usually at least one of aryl radicals Ar_1 , Ar_2 , Ar_3 and Ar_4 is (and in some cases, each of Ar_1 and Ar_3 is independently) 9,9-bis(4-hydroxyphenyl)-fluorene, 2,2-diphenylhexafluoropropane or 2,2-diphenylpropane.

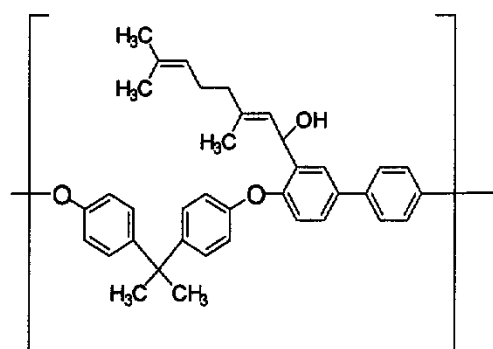
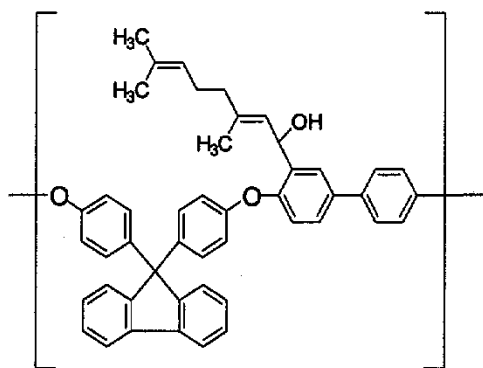
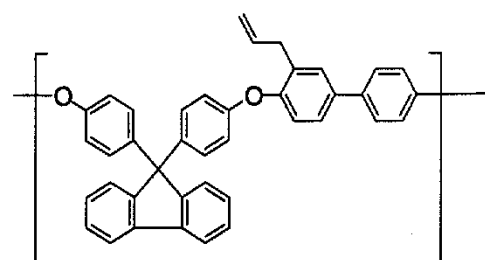
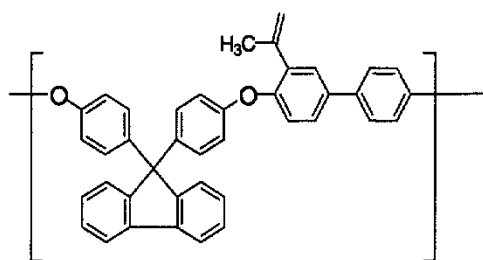
[0032] An additional useful aryl radical comprises :

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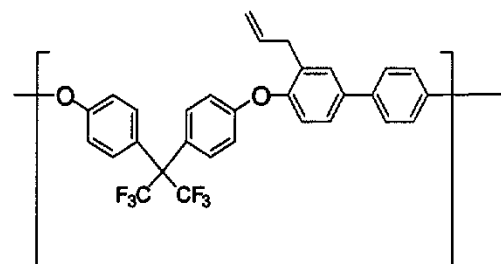
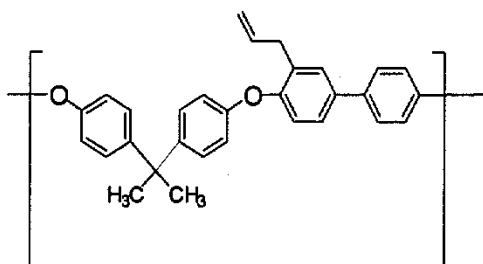


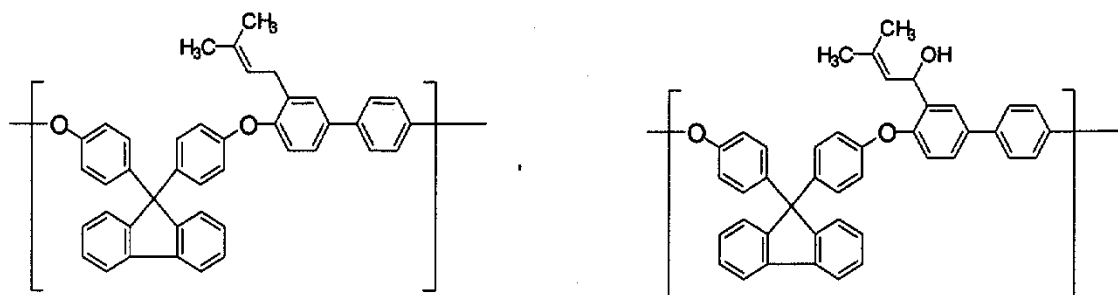
[0033] Useful examples of aryl radicals having unsaturated group(s) grafted thereto comprise :

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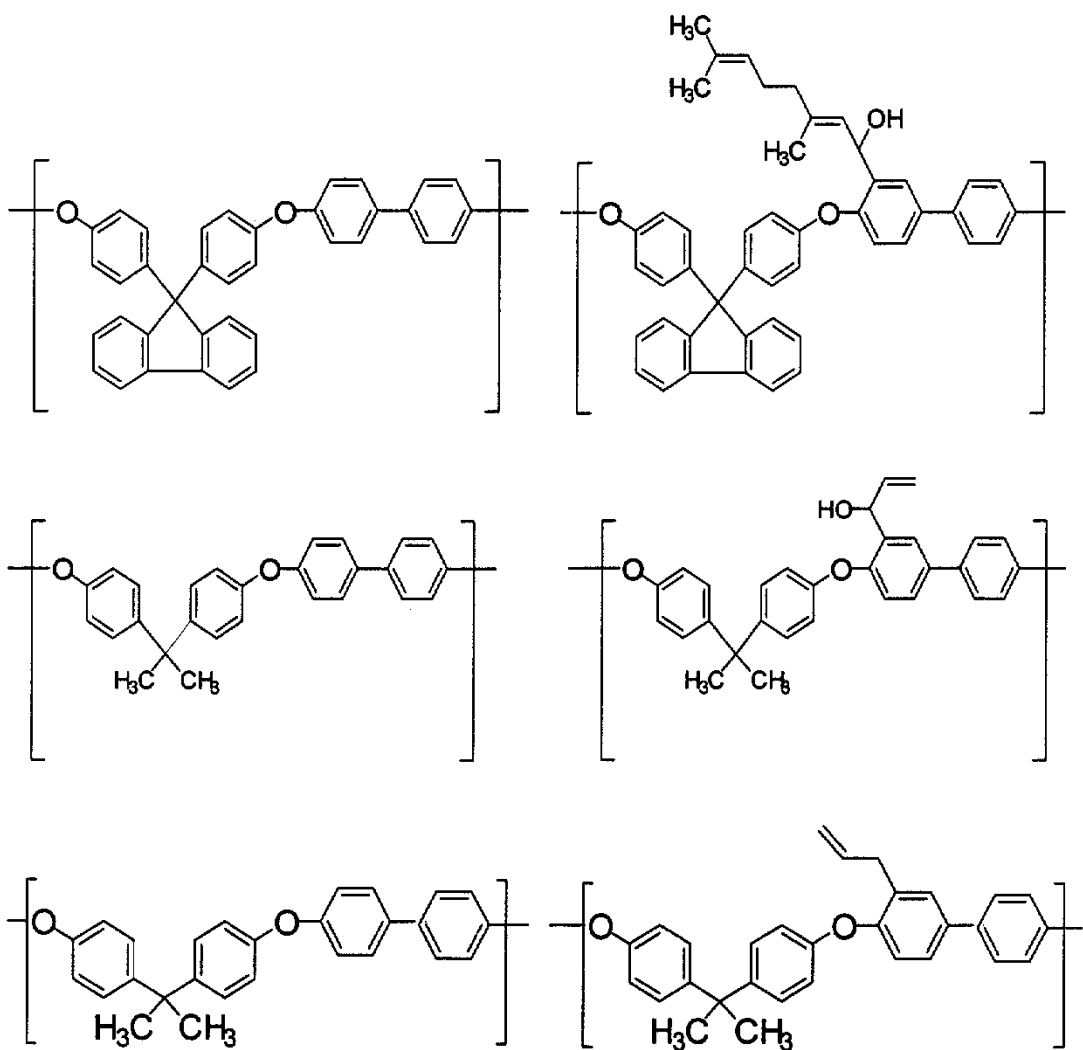
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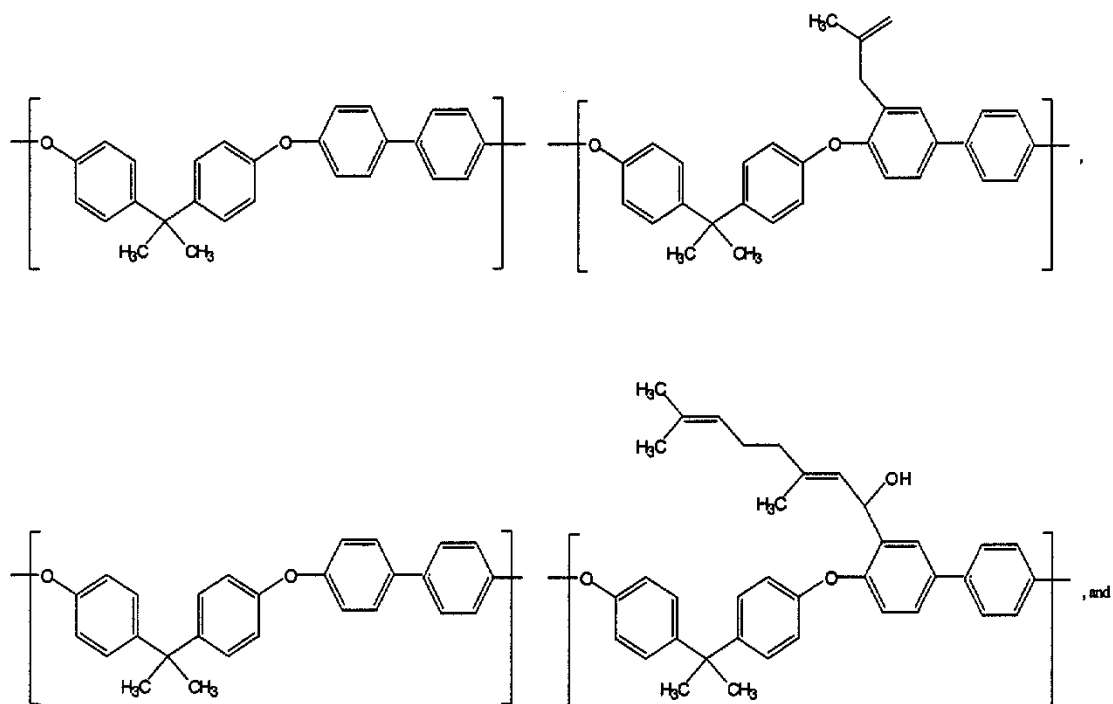




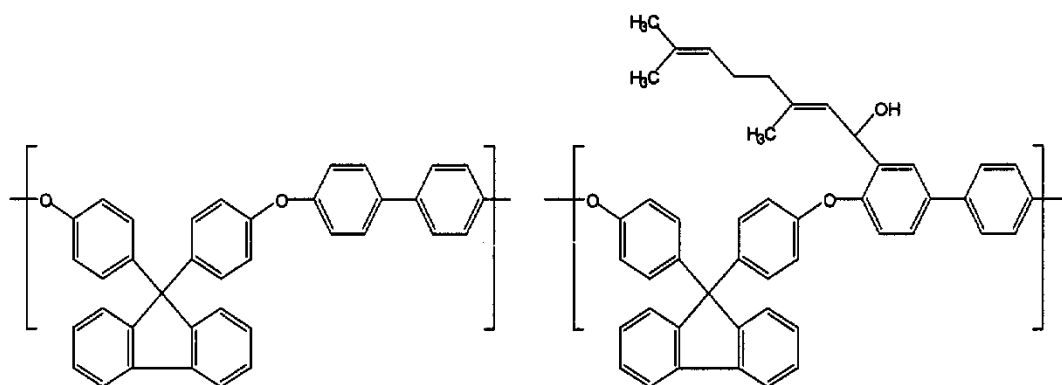
and the corresponding non-grafted polymer repeat units.

[0034] In one aspect of the invention, polymer repeat units of the invention comprise :

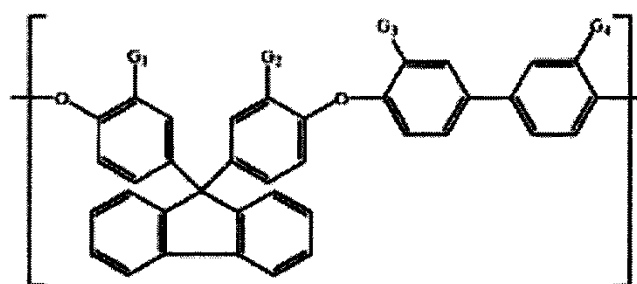




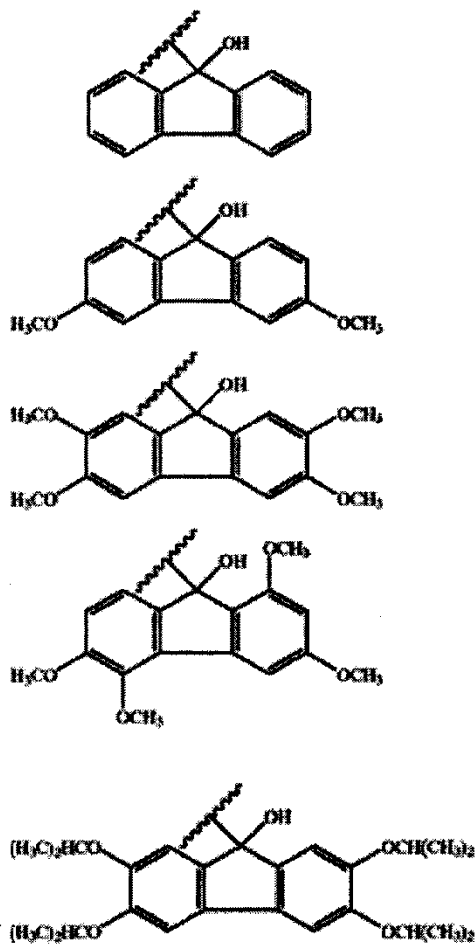
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10 [0035] The grafted polymer can comprise a repeating polymer unit:

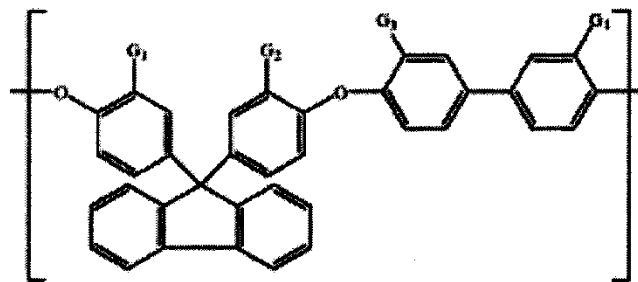


wherein grafts G_{1-4} are individually selected from the group consisting of : H, alkyl, alkylene, functional alkylene, or the radicals represented below:



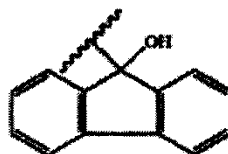
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and mixtures thereof, where Z is the average number of G radicals per polymer unit and Z is in the range of about 0.1 to about 4.0. The grafted polymer can comprise a repeating polymer unit:



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wherein G_{1-4} are individually H, alkyl, alkylene, functional alkylene or:



where Z is the average number of G radicals per polymer unit and Z is in the range of about 0.1 to about 4.0.

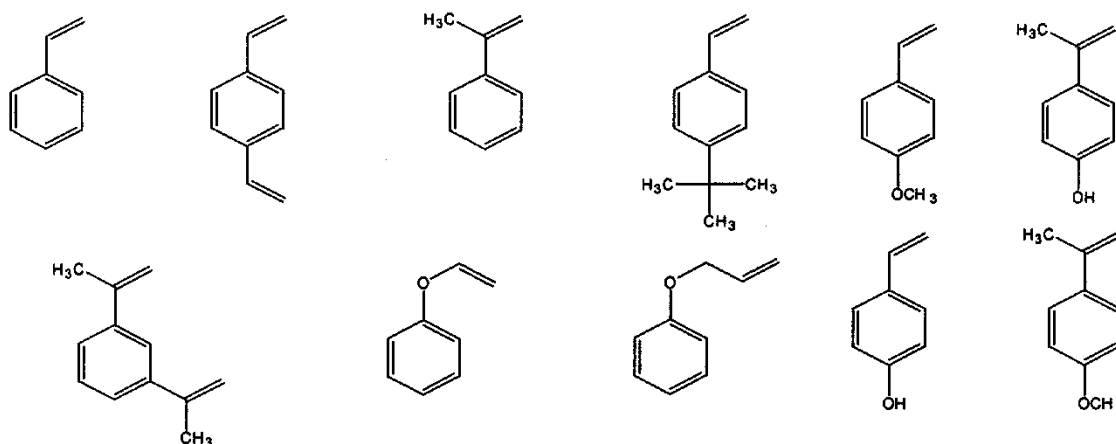
[0036] The invention encompasses the foregoing gate dielectric polymers in cured (crosslinked) condition and uncured condition. Polymers of the invention can be thermally cured by heating to a temperature of at least about 90°C, typically about 100°C to less than about 250°C, usually about 130°C to about 180°C. Optionally, crosslinking is induced in the presence of a catalyst selected from the group consisting of a mineral acid, an organic acid, a free radical starter, an azo-initiator and mixtures thereof.

[0037] Optionally, crosslinking is induced in the presence of sources of radiation in combination with thermal treatment where the radiation may be comprised of ultraviolet (UV) light (e.g., ranging from deep UV up to visible light), electron beam, X-ray, laser, and/or ion beams. The ionizing radiation source may have a wavelength range of from about 1 nanometer (nm) to about 700 nm, or more specifically from about 157 nm to about 500 nm. In embodiments wherein the ionizing radiation source comprises ultraviolet light, the exposure energy may range from about 1 to about 500 mJ/cm². However, the specific energy level can vary and is dependent upon the exposure tool and/or the components of the coating.

[0038] The invention also relates to gate dielectric compositions (cured and uncured) comprising at least one polymer of the invention. The compositions, like the polymers themselves, are useful as gate dielectrics and passivation layers. In addition to the at least one polymer, the compositions can further contain additional ingredients, including but not limited to, at least one solvent, at least one reactive diluent or solvent, at least one plasticizer, at least one surfactant, or at least one inorganic filler. Such compositions can be applied onto a substrate by any suitable method such as spin coating, printing, among other methods. Another method for applying the inventive compositions is disclosed in U.S. Patent Application Publication No. 2006/0079034; hereby incorporated by reference. The inventive compositions can be applied upon a wide range of

substrates such as at least one member selected from the group of silicon, glass, plastic, metal, organic and inorganic semiconductors, and paper, among other substrates.

- [0039]** Reactive diluents and solvents can be incorporated into the composition upon cross-linking, but may not afford a functional group or interfere with the mechanical or electrical properties of the composition. Hence, reactive diluents can allow for a layer that can be applied as a thin film or via printing and can reduce the cost of overall system. Non-limiting examples of suitable reactive diluents comprise at least one member from the group of:



- 10 **[0040]** The amount of solvent typically ranges from about 2wt% to about 95wt% of the composition prior to drying or curing. While any suitable solvent can be used, examples of suitable solvents comprise at least one member selected from the group of toluene, xylene, tetrahydrofuran, cyclohexanone, and dichlorobenzene, among others.

- [0041]** The composition can also comprise at least one reactive solvent or diluent.
- 15 While any suitable reactive solvent or diluent can be used, examples of suitable solvents comprise at least one member selected from the group of styrene, and divinylbenzene, among others. The amount of reactive solvent or diluent typically ranges from about 0.01wt% to about 80wt% of the composition.

- [0042]** The composition can also comprise at least one filler. While any suitable filler
- 20 can be used, examples of suitable fillers comprise at least one inorganic filler selected from the group of silica and alumina, among others. The amount of filler typically ranges from about 0.01wt% to about 50wt% of the composition.

[0043] Polymers of the invention can be provided by modifying the poly(arylene ether) grafting process described in the inventor's earlier U.S. Patent No. 6,060,170, hereby

incorporated by reference, to graft to the poly(arylene ether) backbone non-aromatic unsaturated groups G, rather than the specified aromatic groups of the 6,060,170 patent.

[0044] The resulting polymers, when cured as discussed above, possess such desirable properties as a crosslink temperature from below about 250°C, a dielectric constant below 3.0 with frequency independence, and a maximum moisture absorption of less than 0.17 wt%. These polymers can also be used to produce a film or layer possessing a dielectric constant value of less than about 3; a leakage current value of less than about 1×10^{-8} A/cm² and a breakdown voltage of greater than about 1.5MV/cm. Consequently, the polymers and polymer-containing compositions of the invention are particularly suitable for use as gate dielectrics or passivation layers. The invention therefore further encompasses such gate dielectric or passivation layers and methods for applying them to substrates.

[0045] In addition the invention relates to any multilayer electronic device such as a thin film transistor device comprising the polymer or polymer-containing composition as defined above. In one aspect of the invention, the thin film transistor device contains the polymer in cured form as a gate dielectric or a passivation layer. The thin film transistor may be used for any number of electronic devices including, but not limited to, displays, sensors, imaging devices, RFID tags, memory devices, and other electronic devices utilizing thin film transistors.

[0046] Films formed in accordance with the instant invention typically have a thickness of about 0.05μ to about 1.0μ. Such films can achieve a capacitance of about 5 to about 500nF/cm² and a dielectric constant of about 2.7 to about 3.5.

[0047] Figure 1 illustrates a microelectronic device of one embodiment comprising a bottom gate thin film transistor (TFT1) containing the film of the instant invention. Figure 1 shows TFT 1 comprising substrate 1 over which is applied a gate electrode 2 to give a gate dielectric substrate and a dielectric layer 3. Semiconductor layer 4 is deposited over dielectric layer 3 such that dielectric layer 3 is between the gate electrode and the semiconductor layer. In many embodiments of the invention, the gate dielectric layer 3 is also in direct contact with the substrate 1. This thin film transistor also includes a source electrode 5 and drain electrode 6. The inventive film comprises layer 3 of Figure 1.

[0048] Figure 2 illustrates a different bottom gate structure TFT, TFT2, including a substrate 7, a gate electrode 8 in contact with substrate 7, and a dielectric layer 9 formed

over the substrate and the gate electrode. Two metal contacts, source electrode 10 and drain electrode 11, are deposited on top of the dielectric layer 9. Over and between the metal contacts 10 and 11 is a semiconductor layer 12. The inventive film comprises layer 9 of Figure 2 which is deposited between the gate electrode and the semiconductor. A difference between Figure 1 and Figure 2, is that in Figure 1, the gate dielectric layer is not in direct contact with the source and drain, but in Figure 2 it is in contact with both the semiconductor layer and the gate electrode,

[0049] Figure 3 illustrates a top gate structure TFT, TFT3, which is similar to Figure 2, but inverted to have the gate electrode as the top layer instead of the bottom layer. In this figure, the same components are present with layer 13 as the substrate, layer 14 as the semiconductor, 15 and 16 as the source and drain electrodes, with the gate dielectric layer 17 between the semiconductor and the top gate electrode 18. The gate dielectric layer 17 is between the semiconductor layer 14 and the gate electrode 18, but in this example, the gate dielectric is not in direct contact with the substrate layer 13.

[0050] Additional examples regarding usage of the inventive gate dielectric with TFTs can be found in U.S. Patent Application Publication No. 2005/0224922 A1; hereby incorporated by reference.

[0051] The invention will be illustrated in more detail with reference to the following Examples, but it should be understood that the present invention is not deemed to be limited thereto.

EXAMPLES

[0052] Leakage current density value (LCDV) measurements can be made using the Hg probe method:

[0053] The mercury probe was made by MSI electronics model Hg-401. The contact area of the mercury probe is 0.7 mm^2 with $\pm 2\%$ of uncertainty. The power source and current meter is a Keithley 6517A. The mercury probe is placed in a Faraday cage to reduce the electric noise. The connection between the controller and mercury probe are BNC cables. The noise level of the system is less than 100 fA.

[0054] Thin films were coated on a low resistance silicon (Si) wafer (0.01 ohm) before the measurement. The thicknesses of the films were typically about 50nm to about 500nm. The film sample on Si was placed face down on the mercury probe so that the gate dielectric film was in contact with the mercury and a metal disk was in contact with

the backside of the wafer. LCDV measurements were made by applying a constant voltage on the sample and measuring the current through the film. The reported LCDV is the current that was measured 3 minutes after applied a voltage to a film to avoid the charging current between the wafer and the insulated plate of the mercury probe.

- 5 **[0055]** LCDV leakage current density value measurement can also be made by using the metal dot method (e.g., to avoid background charging issue). Instead of using mercury as the contact electrode for the LCDV measurement, a small disk of metal film was deposited on top of the dielectric sample. A 0.5mm and 1.0 mm shadow mask was used to aid in the deposit of 147 nm thick silver (Ag) dots by vapor deposition (Deposited
- 10 at a rate of 4-5 Å/sec at 20 V under 4.3×10^{-7} torr). The thickness of the deposited metal disk is about typically 100-200 nm. Typical deposit metals are silver, aluminum, or gold. A gold wire (1 mm in diameter) is used to contact the metal disk. The measurements were done by applying stepping voltages and measuring the current. The stepping voltage started at 0V and ended at 300V. Each step is 5V with holding time of 1 second.
- 15 The leakage current was recorded at 1.5 MV/cm.

Example 1: Fabrication and Characterization of Thin Film Transistors

- [0056]** A solution for use as a gate dielectric layer was prepared by dissolving 10
- 20 grams of 9-fluorenone-graft poly(arylene ether) in 90 grams of cyclohexanone solvent. The polyarylene ether solution was filtered by through a 1μ filter. This filtered solution was deposited on a silicon wafer by spin coating at 1650rpm for 1 minute and baked at 250°C . The capacitance of the resulting 0.5μ layer was measured as 5 nF/cm^2 , via a mercury probe with a dielectric constant value of 3.0.

25

Example 2: A Thin Film Transistor with Poly(arylene Ether) as the Gate Dielectric

- [0057]** A bottom gate thin film transistor similar to Figure 1 is fabricated by depositing an metal layer (Mo, Al, or Au) and then depositing a photoresist on top of the metal layer. The photoresist is patterned and developed to leave open the areas around where the
- 30 gate electrode will be present and the metal areas adjacent to the gate electrode are etched away. Using a poly(arylene ether) solutions of Example 4, a gate dielectric layer is deposited onto the gate electrode via spin-coating this solution. On top of the gate dielectric layer is deposited an organic semiconductor layer such as P3HT or a doped

polythiophene polymer. On top of the semiconductor is deposited a metal layer of Mo, Al, or Au which is then patterned in a manner similar to the gate electrode to give the source and drain electrodes on top of the semiconductor layer

5 **Example 3: Preparation and Characterization of Poly(arylene ether) Gate Dielectric Layer for Use in the Thin Film Transistors**

[0058] A solution for use as a gate dielectric layer was prepared by dissolving 10 grams of 9-fluorenone-grafted poly(arylene ether) in 90 grams of cyclohexanone solvent. The dissolved grafted polyarylene ether) was filtered by through a 1 μ filter. This filtered
10 solution was deposited on a silicon wafer by spin coating at 3000 rpm for 40 seconds. Film 3a was then baked at 250°C for 3 min. on a hot plate to give a 491 nm thick film. The leakage current density value (LCDV) for this film 3a on a silicon wafer was 3.0×10^{-10} A/cm² at 1.5 MV/cm when measured in N₂ and the LCDV was 4.7×10^{-10} A/cm² at 1.5 MV/cm when measured in air at constant temperature and humidity (CTH) set at 71 °F
15 and 42% humidity. Film 3b was then baked at 135°C for 3 min. on a hot plate to give a 522 nm thick film. The leakage current density value (LCDV) for this film 2b on a silicon wafer was 3.0×10^{-10} A/cm² at 1.5 MV/cm when measured in N₂. LCDV values were obtained via a mercury probe.

20 **Example 4: Preparation and Characterization of Low temperature Cured Poly(arylene ether) for Use in Thin Film Transistors**

[0059] A solution for use as a gate dielectric layer was prepared by dissolving 0.5 grams of citral-grafted poly(arylene ether) (Citral/poly(arylene ether) ratio= 0.83:1) in 8.93 grams of cyclohexanone solvent. The citral poly(arylene ether) solution in
25 cyclohexanone was filtered through a 3 μ m PTFE filter followed by passing through a 0.45 μ m PVDF filter. This filtered solution was deposited on a silicon wafer by spin coating it at 1500rpm for 1 minute to give film 4a and the coating procedure was repeated to give film 4b. Film 4a was then baked at 180°C for 60 min. on a hot plate to give a 356nm thick film. Film 4a was determined to be crosslinked under the heating
30 conditions above by measuring the film thickness before (356nm) and after (356nm) exposure to dichlorobenzene for 15 minutes, with a water wash and a 180C bake for 6 minutes carried out after the solvent exposure. Film 4b was baked at 250°C for 6 min.

on a hot plate to give a 365 nm thick film. The leakage current density value (LCDV) for this film 4b on a silicon wafer was

- [0060]** 1.5×10^{-9} A/cm² at 1.5 MV/cm when measured in air at constant temperature and humidity (CTH: 71 °F and 42% humidity). LCDV values were obtained via a 0.5 mm and 1.0 mm silver metal dots.

Example 5: Viscosity Measurements on Low Temperature Curing, Ink-Jet Capable Poly(arylene Ether) Gate Dielectric Solution

- [0061]** Viscosity measurements were run at two different polymer solution concentrations which were prepared by dissolving 0.506 grams of citral-graft poly(arylene ether) (Citral/poly(arylene ether) ratio= 0.63:1) in 8.5 grams of cyclohexanone solvent to give a 5.6 weight % solution, 5a and by dissolving 0.506 grams of this same polymer in 10.73 grams of cyclohexanone solvent to give a 4.5 weight % solution, 5b. The following viscosities were obtained from these solutions. These solutions have a viscosity within a range that is useful for deposition via ink jet printing.

Temperature (°C)	Viscosity (cps) Solution 5a	Viscosity (cps) Solution 5b
20	18.6	12.4
25	16.7	11.2
30	14.8	10.1
35	13.2	9.1
40	11.9	8.2
45	10.7	7.5
50	9.7	6.7

Example 6: Preparation and Characterization of Low Temperature and UV Cured Poly(arylene Ether) Polymer Gate Dielectric

- [0062]** A solution for use as a gate dielectric layer was prepared by dissolving 0.5 grams of citral-graft poly(arylene ether) (citral/poly(arylene ether) ratio= 0.42:1) in 8.93 grams of cyclohexanone solvent. The citral poly(arylene ether) solution was filtered through a 0.2 µm PTFE filter. This filtered solution was deposited on a silicon wafer by spin coating at 1500rpm for 1 minute to give film 6a and this deposition procedure was

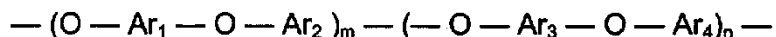
repeated five times to produce films 6b, 6c, 6d, 6e, and 6f. Film 6a was baked at 250°C for 6 minutes on a hot plate to give a 341 nm thick film. Film 6a was determined to be crosslinked under the heating conditions above by measuring the film thickness before (341nm) and after (343nm) exposure to dichlorobenzene for 15 minutes, with a water wash and a 250C bake for 6 minutes carried out after the solvent exposure. Film 6b was baked at 185°C for 60 minutes on a hot plate to give a 353nm thick film. The resulting polymer layer was only partially crosslinked under these conditions as evidenced by Film 6b measuring 175nm (50% loss in thickness) after exposure to dichlorobenzene for 15 minutes followed by a wash with DI water and a bake at 185 °C for 6 minutes. Film 6c was exposed to broad band UV for 20 seconds then baked at 185°C for 60 minutes on a hot plate to give a 338nm thick film. We determined that this polymer was crosslinked under these conditions as evidenced by Film 6c measuring 338 nm after its exposure to dichlorobenzene for 15 minutes. Film 6d was exposed to a broad band UV lamp for 1 minute then baked at 180°C for 30 minutes on a hot plate to give a 334nm thick film. We determined that this polymer was crosslinked under these conditions as evidenced by Film 6d measuring 334nm after exposure to dichlorobenzene for 15 minutes followed by a wash with DI water and a bake at 180 °C for 3 minutes. Film 6e was exposed to a broad band UV lamp for 1 minute then baked at 180°C for 7.5 min. on a hot plate to give a 334 nm thick film. We determined that this polymer was crosslinked under these conditions as evidenced by Film 6e measuring 334nm after exposure to dichlorobenzene for 15 minutes followed by a wash with DI water and a bake at 180 °C for 3 minutes. Film 6f was exposed to a broad band UV lamp for 1 minute then baked at 150°C for 7.5 min. on a hot plate to give a 341nm thick film. We determined that this polymer was crosslinked under these conditions as evidenced by Film 6f measuring 339nm after exposure to dichlorobenzene for 15 minutes followed by a wash with DI water and a bake at 150 °C for 3 minutes.

Film	UV Exposure (seconds)	Bake Temp (°C)	Bake Time (minutes)	Thickness before chemical exposure (nm)	Thickness after chemical exposure (nm)	% Thickness Change
6a	0	250	6	340.8	342.9	+ 0.63
6b	0	185	60	352.7	174.7	- 50.50
6c	20	185	60	338.0	337.8	- 0.04
6d	60	180	30	334.0	334.0	+ 0.01
6e	60	180	7.5	334.2	334.1	- 0.04
6f	60	150	7.5	340.9	339.2	- 0.48

- [0063]** Although certain aspects of the invention are illustrated and described herein with reference to given embodiments, it is not intended that the appended claims be
- 5 limited to the details shown. Rather, it is expected that various modifications may be made in these details by those skilled in the art, which modifications may still be within the spirit and scope of the claimed subject matter and it is intended that these claims be construed accordingly.

CLAIMS

1. A gate dielectric layer or passivation layer in a thin film transistor wherein the layer comprises at least one polymer comprising repeat units of the following structure:



5 where Ar_1 , Ar_2 , Ar_3 , and Ar_4 are identical or different aryl radicals, m is 0 to 1, n is 1- m , and at least one of the aryl radicals is grafted to at least one unsaturated or saturated group that is non-aromatic and is adapted to crosslink at a curing temperature below 200°C without producing volatiles during curing and without providing functional groups after curing.

10

2. The gate dielectric or passivation layer of Claim 1 capable of being cured at temperatures less than about 250 °C.

15

3. The gate dielectric or passivation layer of Claim 1 capable of being cured at about 180 °C.

4. The gate dielectric or passivation layer of Claim 1 capable of being cured by a method comprising exposing the layer to a source of radiation and heating to at temperature of less than about 180 °C.

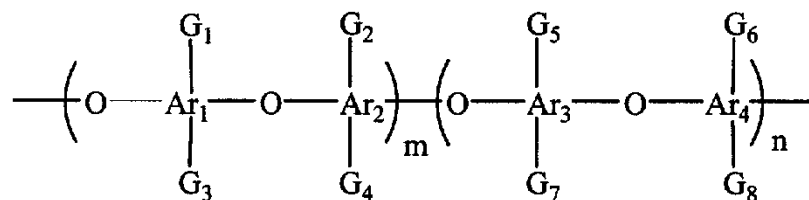
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5. The gate dielectric or passivation layer of claim 4 wherein the exposing comprises exposing the layer to a source of radiation comprising at least one members elected from the group consisting of electron beam, photon, ultraviolet light, visible light, X-ray, thermal, and combinations thereof.

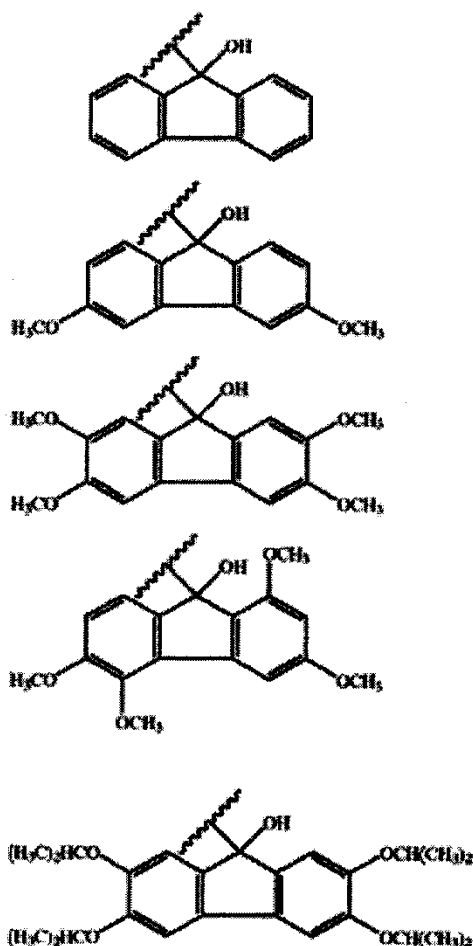
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6. The gate dielectric or passivation layer of claim 5 , wherein the exposing comprising exposing the layer to ultraviolet or visible light.

7. A poly(arylene ether) polymer for use as a gate dielectric or passivation layer for a thin film transistor wherein the polymer comprises polymer repeat units of the following structure:



- 5 where $G_1, G_2, G_3, G_4, G_5, G_6, G_7$ and G_8 are identical or different and are H or aryl-containing groups:



8. The polymer of claim 7 wherein said polymer has a dielectric constant lower than about 3.0

9. The polymer of claim 7 wherein said polymer has a dielectric constant higher than about 2.7.

10. A multilayer electronic device comprising:

5 at least one gate electrode comprising at least one gate dielectric layer comprising at least one poly(arylene ether) polymer

 at least one source electrode;

 at least one drain electrode;

 at least one semiconductor layer;

10 wherein the gate dielectric layer has a dielectric constant greater than about 2.7.

11. A thin film transistor comprising:

 at least one gate electrode;

15 at least one gate dielectric layer comprising at least one poly(arylene ether) polymer

 at least one source electrode;

 at least one drain electrode;

 at least one semiconductor layer;

20 wherein the gate dielectric layer has a dielectric constant of greater than about 2.7.

12. The thin film transistor according to claim 11 , wherein the poly(arylene ether) polymer is grafted.

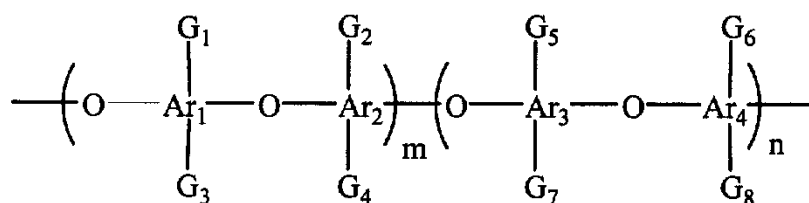
25 13. The thin film transistor according to claim 11 , wherein the poly(arylene ether) polymer is grafted to at least one unsaturated group.

14. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer is grafted to more than one unsaturated group.

15. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer is grafted with an aryl-containing graft.

16. The thin film transistor according to claim 11, wherein the poly(arylene ether) is not fluorinated.

17. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer repeat units have the following structure:



where G_1 , G_2 , G_3 , G_4 , G_5 , G_6 , G_7 and G_8 are identical or different species of the at least one unsaturated group.

15

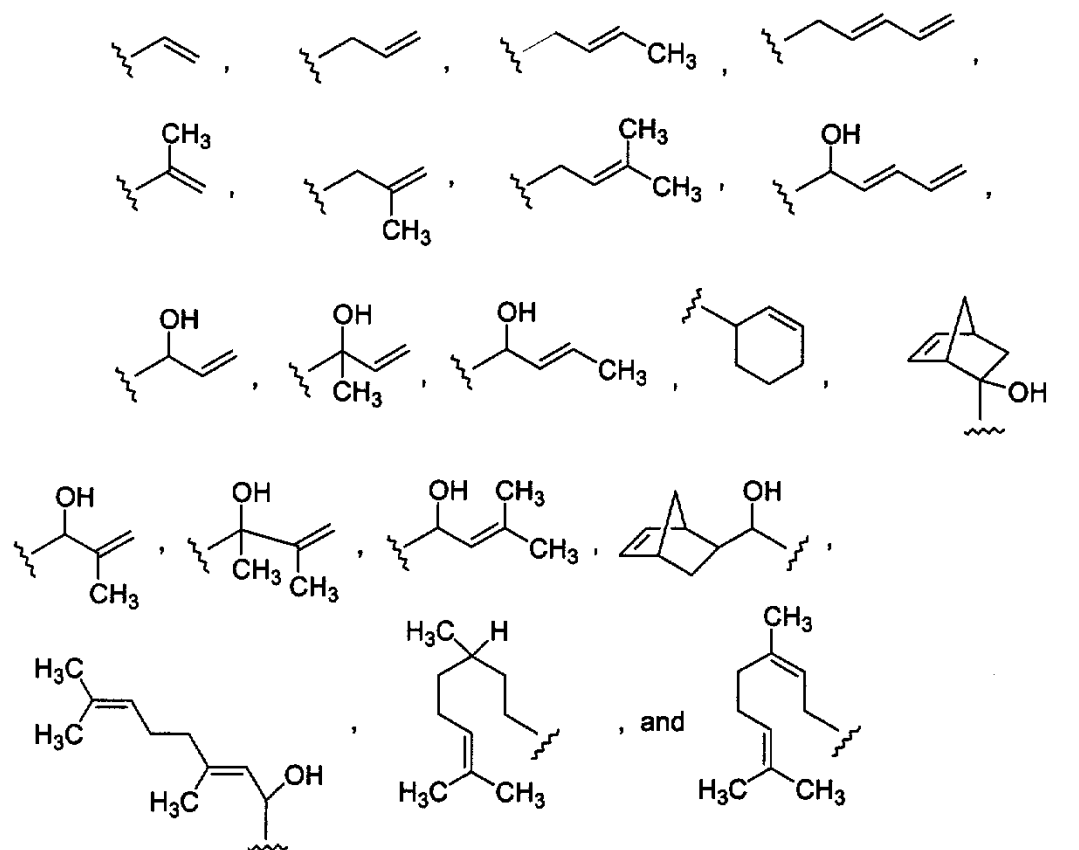
18. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer contains an average number of unsaturated groups per polymer repeat unit of 0.1 to 4.

19. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer contains an average number of unsaturated groups per polymer repeat unit of 1 to 2.

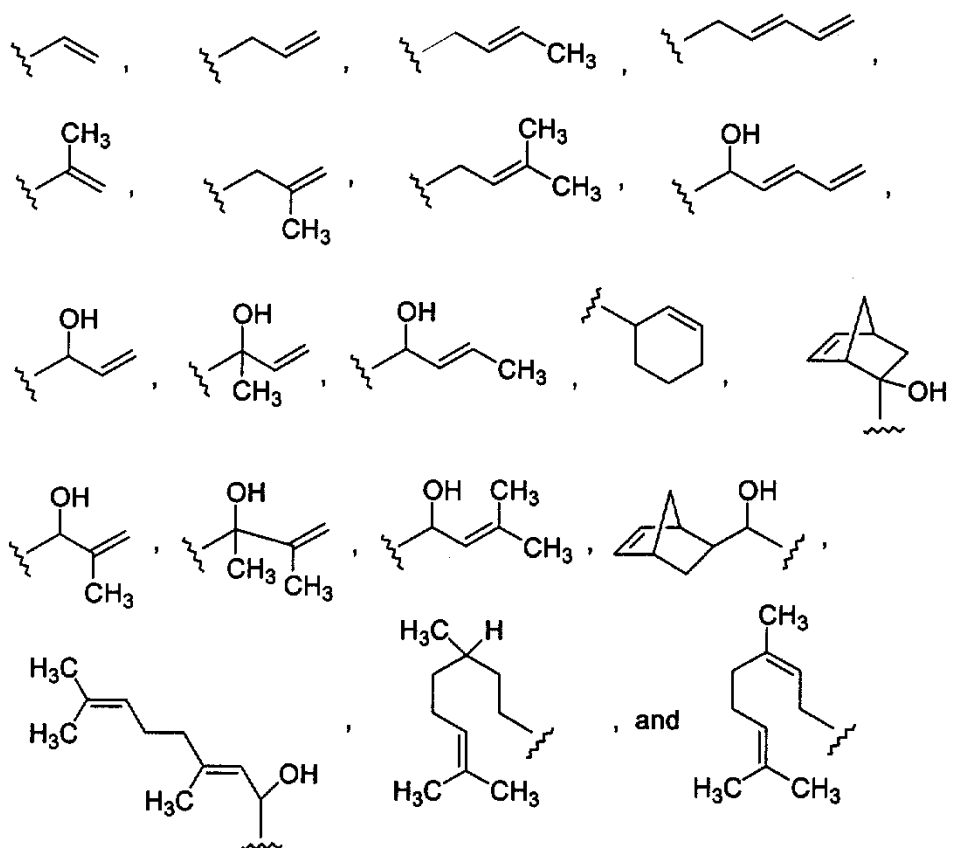
20. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer comprises at least one unsaturated group comprising at least one member

selected from the group consisting of an alkylene radical, an alkyldiene radical, an α -hydroxyalkylene radical and an α -hydroxyalkyldiene radical.

21. The multilayer electronic device according to claim 10 wherein the poly(arylene ether) polymer comprises at least one unsaturated group comprising at least one member selected from the group consisting of:

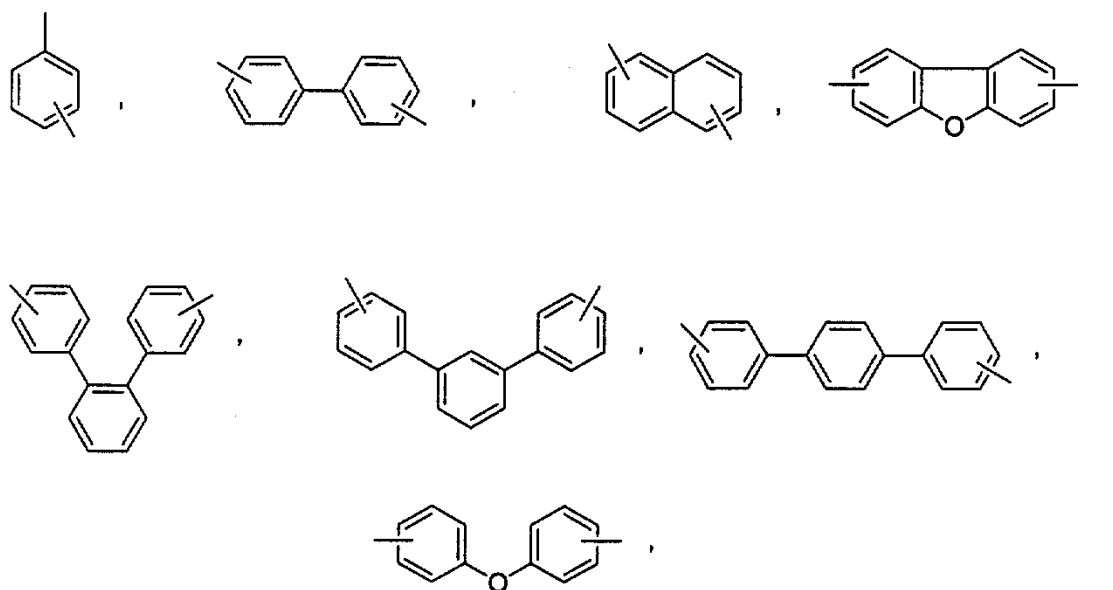


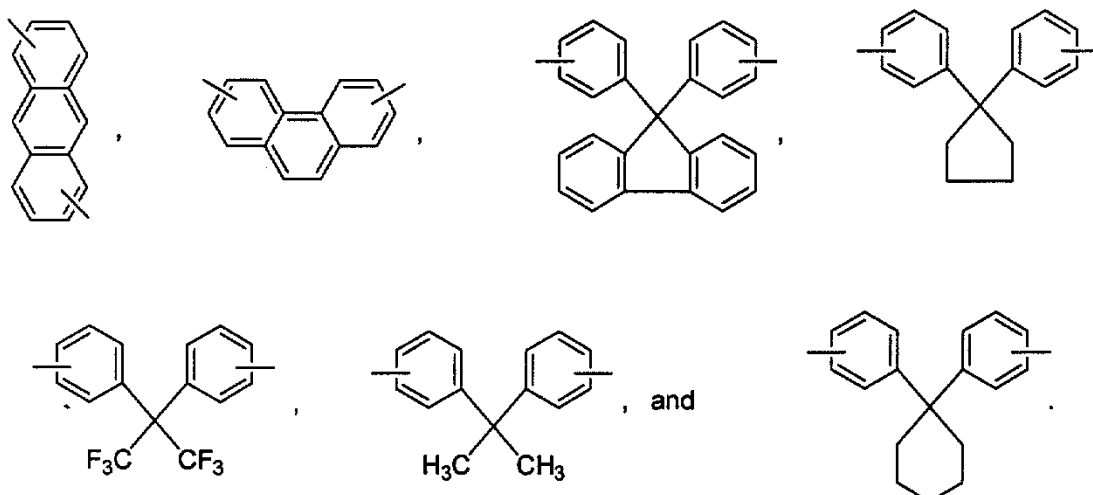
10 22. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer comprises at least one unsaturated group comprising at least one member selected from the group consisting of:



23. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer contain the aryl radicals that are independently selected from the group

5 consisting of:

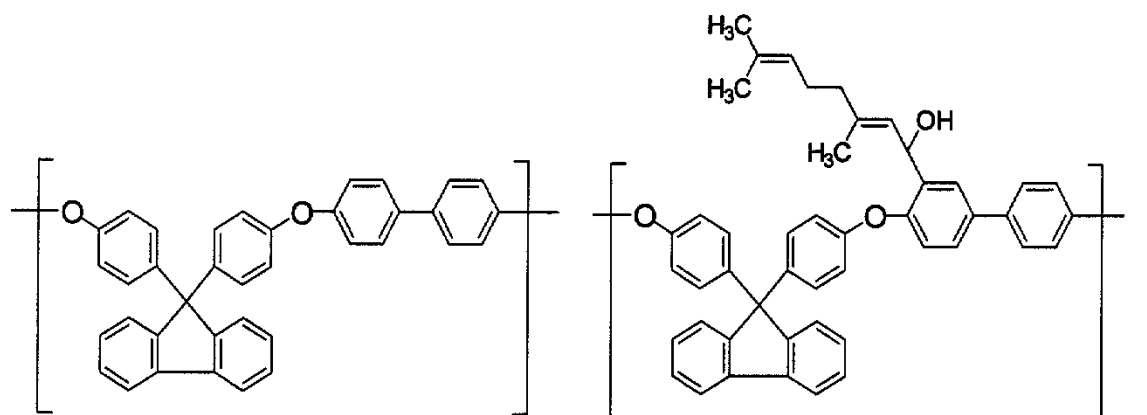




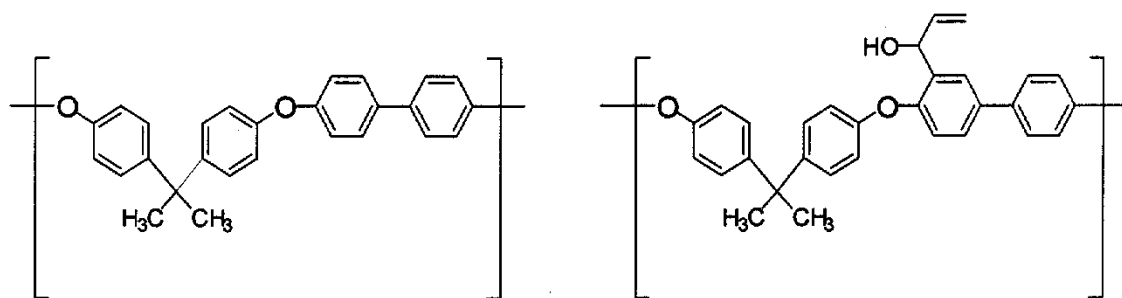
24. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer comprises at least one of the aryl radical that is selected from the group consisting of 9,9-bis(4-hydroxyphenyl)-fluorene, 2,2-diphenylhexafluoropropene and 2,2-diphenylpropene.

25. The thin film transistor according to claim 11, wherein the poly(arylene ether) polymer contain the average number of unsaturated groups per polymer unit is more than 0.1 and not more than 1, and the poly(arylene ether) polymer comprises one of the following polymer repeat units:

a)

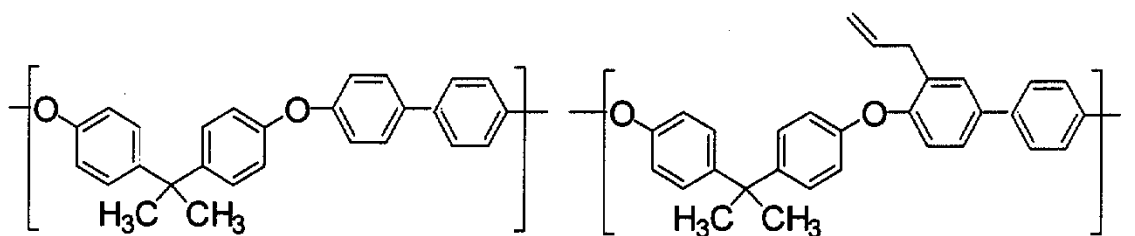


b)

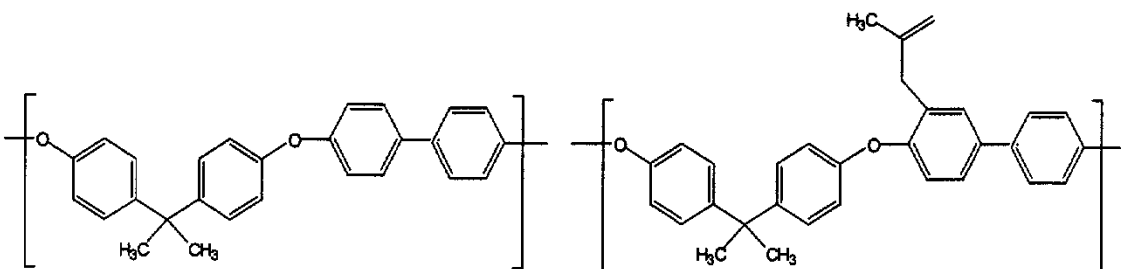


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c)

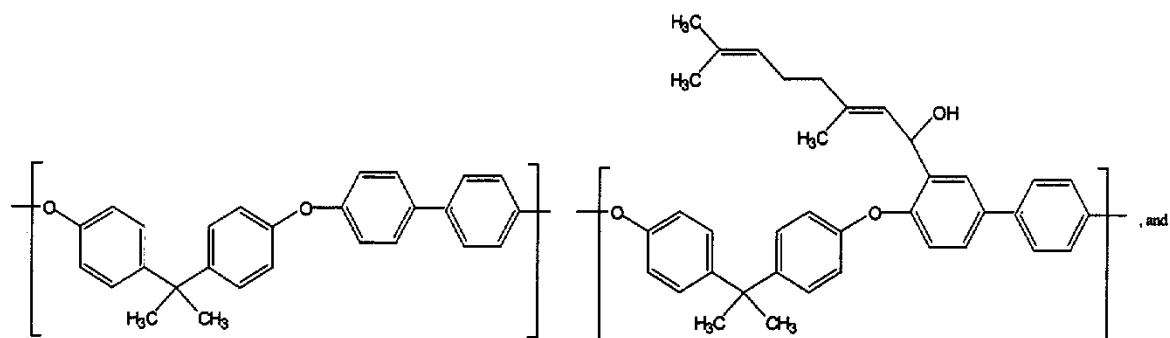


d)



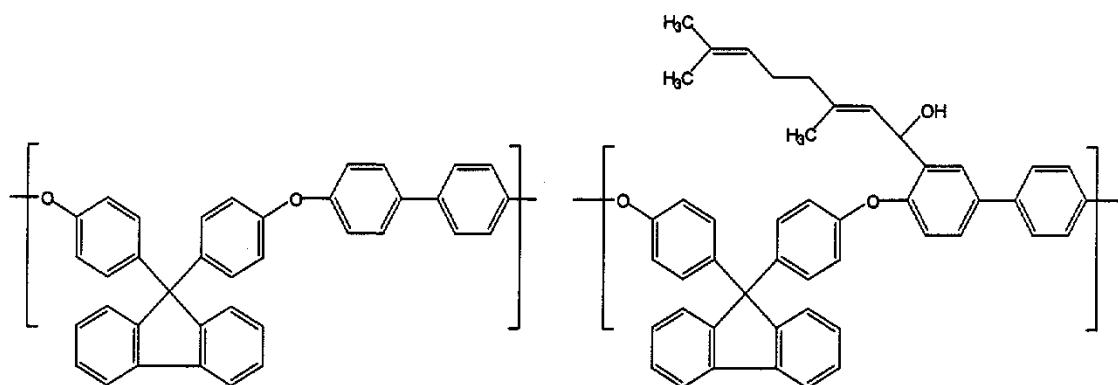
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e)



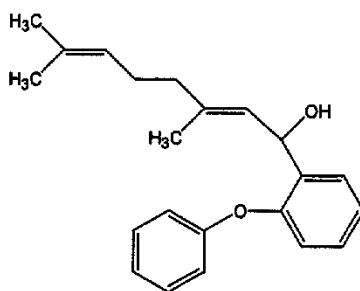
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f)



26. The thin film transistor of claim 11, wherein the poly(arylene ether) polymer contains at least one of the aryl radicals:

10



27. The thin film transistor of claim 11, wherein the gate dielectric layer has a capacitance of greater than about 5 nF/cm².

28. The thin film transistor of claim 11, wherein the poly(arylene ether) polymer is present in cured form, said cured form of the polymer having a curing temperature from about 130 to about 180°C, a dielectric constant below about 3.0, and a maximum
5 moisture absorption of less than about 0.2 wt%.

29. A thin film transistor comprising:
a substrate;
At least one gate electrode;
10 At least one gate dielectric layer comprising at least one poly(arylene ether);
At least one source electrode;
At least one drain electrode;
15 At least one semiconductor layer in contact with the source and drain electrodes, wherein the gate dielectric layer has a dielectric constant of greater than about 2.7 and a capacitance of greater than about 5 nF/cm².

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