

DESCRIPTION

TITLE: PROCESS FOR MANUFACTURING A MULTILAYER STRUCTURE COMPRISING A POROUS SILICON LAYER

TECHNICAL FIELD OF THE INVENTION

5 [0001] The technical field of the invention is that of semiconductor materials for microelectronic components. The invention more particularly relates to a multi-layer structure adapted to high-performance radio frequency applications and comprising a buried porous silicon layer.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

10 [0002] Radio frequency (RF) integrated circuits are widely used in telecommunications (cellular telephony, Wi-Fi, Bluetooth, etc.). These circuits are fabricated on substrates (also referred to as wafers) which mainly serve as a support for their manufacture. As the level of integration and performance of RF circuits increases, there is an ever-increasing coupling between their performance and
15 characteristics of the substrate on which they are formed.

[0003] By way of example of circuit-substrate coupling, electromagnetic fields from high-frequency signals propagating in RF circuits penetrate deep into the substrate and interact with charge carriers located therein. This leads to problems of non-linear distortion (harmonics) of the signal, unnecessary consumption of part of the signal
20 energy through insertion loss and possible influences between circuits.

[0004] Radio frequency (RF) circuits, such as RF signal transceiver modules (so-called "front-end" modules), antenna switches and adapters, and power amplifiers, can be fabricated on different types of substrate.

[0005] Fig. 1 shows a multi-layer structure 10 derived from the Silicon On Insulator (SOI) multi-layer structure and commonly usable in the manufacture of RF integrated
25 circuits.

[0006] This multi-layer structure 10, referred to as "TR-SOI", successively comprises a support layer 11 of high-resistivity silicon ($> 1 \text{ k}\Omega\cdot\text{cm}$), a charge-trapping layer 12 (also referred to as a trap-rich layer), a buried oxide layer 13 and an active
30 layer 14 of single crystal silicon. The trapping layer 12 prevents the parasitic conduction phenomenon at the interface between the support layer 11 and the buried oxide layer

13, which phenomenon is usually caused by free electrons accumulating at the interface under the effect of fixed positive charges contained in the buried oxide layer 13. By virtue of the trapping layer 12, electrons are trapped and can no longer circulate. Effective resistivity of the support layer 11 is thus increased relative to a multi-layer structure free of a trapping layer (a structure referred to as "HR-SOI"). The trapping layer 12 can consist of polycrystalline silicon. The traps are located at the grain boundaries of polycrystalline silicon.

[0007] The combination of a high-resistivity support layer 11 and a trapping layer 12 reduces the circuit-substrate coupling mentioned as an example and therefore greatly improves the RF performance of integrated circuits manufactured from the multi-layer structure 10, especially in terms of linearity and crosstalk. Passive elements (inductors, capacitors, etc.) formed over the active layer 14 in turn benefit from a better quality factor.

[0008] However, a substrate provided with a polycrystalline silicon trapping layer has RF performance that degrades as the temperature of use increases. Indeed, polycrystalline silicon has the drawback of undergoing partial recrystallisation during heat treatment steps at high temperatures, which contributes to reducing density of traps in the layer.

[0009] Fig. 2 schematically represents another multi-layer structure 20 adapted to radio frequency applications and described in document WO2021/001066A1.

[0010] The multi-layer structure 20 comprises a support layer 21 of silicon (resistivity between $0.5\Omega\cdot\text{cm}$ - $4\Omega\cdot\text{cm}$), a porous silicon layer 22 disposed on the support layer 21, a dielectric layer 23 (for example of silicon oxide) disposed on the porous silicon layer 22 and an active layer 24 (for example of silicon), also referred to as the surface layer and disposed on the dielectric layer 23.

[0011] The method for manufacturing this multi-layer structure 20 especially comprises:

- a step of providing a support substrate of silicon;
- a step of porosifying part of the support substrate to form the porous silicon layer 22;
- a step of depositing the dielectric layer 23 onto the porous silicon layer 22;

- a step of providing a donor substrate comprising a buried brittle plane delimiting the surface layer 24;
- a step of assembling the donor substrate on the dielectric layer, by disposing the surface layer 24 in contact with the dielectric layer 23;
- 5 - a separation step along the buried brittle plane to transfer the surface layer 24 onto the dielectric layer 23; and
- one or more heat treatment steps aiming at improving crystal quality of the surface layer 24 or its surface state (roughness, defectivity).

[0012] However, it happens that the surface layer 24 cracks during the separation
 10 step and/or the substrate finally obtained, formed by the multi-layer structure 20, curve
 excessively after the separation step, especially during the heat treatment steps. Such
 defects render the substrate unusable for the manufacture of RF circuits.

SUMMARY OF THE INVENTION

[0013] The purpose of the invention is to reduce the risk of cracks upon transferring
 15 a surface layer from a donor substrate onto a support substrate comprising a porous
 silicon layer and to limit the curvature phenomenon of the multi-layer structure thus
 obtained.

[0014] According to the invention, this purpose tends to be achieved by providing
 a method for manufacturing a multi-layer structure, comprising the following steps of:

- 20 - providing a support substrate comprising a support layer and a porous
 silicon layer disposed on the support layer;
- providing a donor substrate comprising a first face, a buried brittle plane and
 a surface layer delimited by the first face and the buried brittle plane;
- assembling the support substrate and the donor substrate by bonding, the
 25 surface layer of the donor substrate being disposed in contact with the
 support substrate; and
- separating the surface layer from the donor substrate by fracturing along
 the buried brittle plane.

This manufacturing method is remarkable in that at least one of the support and donor
 30 substrates, called a degraded substrate, comprises a degraded portion so as to

prevent it from being bonded to the other of the support and donor substrates during the assembly step, the degraded portion having an annular or substantially annular shape and being located less than 25 mm from the flank of said degraded substrate, preferably less than 5 mm from the flank of said degraded substrate.

5 [0015] In some modes of implementation of the manufacturing method, the support substrate further comprises a non-porous silicon peripheral portion disposed around the porous silicon layer and the degraded portion is located, in assembling the support substrate and the donor substrate, in vertical alignment with an interface between the non-porous silicon peripheral portion and the porous silicon layer.

10 [0016] In another mode of implementation, the porous silicon layer comprises a central portion having a substantially constant first thickness and a peripheral portion having a second thickness increasing towards the flank of the support substrate and the degraded portion is located, in assembling the support substrate and the donor substrate, in vertical alignment with a transition between the central portion and the
15 peripheral portion of the porous silicon layer.

[0017] In another mode of implementation, the support substrate further comprises a peripheral portion of non-porous silicon disposed around the porous silicon layer and the degraded portion consists of a cavity extending into the porous silicon layer and located at a distance of less than 2 mm from an interface between the peripheral
20 portion of non-porous silicon and the porous silicon layer. The cavity is advantageously filled with a material having a Young's modulus lower than that of porous silicon.

[0018] Further to the characteristics just discussed in the preceding paragraphs, the manufacturing method according to the invention may have one or more additional characteristics from among the following, considered individually or according to any
25 technically possible combination:

- the degraded portion further extends to the flank of said degraded substrate;
- the degraded portion is spaced from the flank of said degraded substrate and has a width between 10 μm and 4 mm;
- the degraded portion consists of a recessed portion;
- 30 - the recessed portion belongs to the donor substrate;

- the step of providing the donor substrate comprises a step of implanting light ions into a first substrate at an implantation depth to form the buried brittle plane, the recessed portion being obtained by forming a cavity with a depth greater than the implantation depth;
- 5 - the recessed portion belongs to the support substrate;
- the degraded portion consists of a textured portion with a surface roughness greater than or equal to 1 nm;
- the degraded portion consists of a chamfered portion;
- the support substrate further comprises a dielectric layer disposed on the porous silicon layer; and
- 10 - the degraded portion is substantially annular and the degraded substrate comprises a so-called non-degraded portion located as an extension of the degraded portion, said non-degraded portion being bonded to the other of the support and donor substrates during the assembly step.

15 **BRIEF DESCRIPTION OF THE FIGURES**

[0019] Further characteristics and advantages of the invention will clearly become apparent from the description thereof given below, by way of indicating and in no way limiting purposes, with reference to the appended figures, in which:

- Fig. 1, previously described, represents a multi-layer structure according to prior art, which can be used as a starting substrate for the manufacture of radio-frequency integrated circuits;
- 20 - Fig. 2, previously described, represents another multi-layer structure according to prior art, also adapted to the manufacture of radio frequency circuits;
- 25 - Fig. 3A to 3C represent a first mode of implementation of the multi-layer structure manufacturing method according to the invention;
- Figs. 4A to 4C represent a second mode of implementation of the multi-layer structure manufacturing method;
- Figs. 5A to 5C represent a third mode of implementation of the multi-layer structure manufacturing method;
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- Figs. 6A to 6C represent a fourth mode of implementation of the multi-layer structure manufacturing method;
- Figs. 7A to 7C represent a fifth mode of implementation of the multi-layer structure manufacturing method;
- 5 - Figs. 8A to 8C represent a sixth mode of implementation of the multi-layer structure manufacturing method;
- Figs. 9A to 9C represent a seventh mode of implementation of the multi-layer structure manufacturing method;
- Figs. 10A to 10C represent a mode of implementation for the step of
10 providing the support substrate comprising the porous silicon layer; and
- Fig. 11 represents a main face of a substrate comprising a substantially annular degraded zone.

[0020] For greater clarity, identical or similar elements are identified by identical reference signs throughout the figures.

15 **DETAILED DESCRIPTION**

[0021] Figs. 3A-3C, 4A-4C, 5A-5C, 6A-6C, 7A-7C, 8A-8C and 9A-9C illustrate different modes of implementation of a method for manufacturing a multi-layer structure 30. The multi-layer structure 30 is intended to serve as a support for the manufacture of microelectronic components, in particular radio frequency (RF)
20 integrated circuits. It thus forms a wafer.

[0022] These figures represent a cross-section view of only part of the multi-layer structure 30 and the substrates 40, 50 required to manufacture it. The multi-layer structure 30 and the substrates 40, 50 each comprise two main faces (commonly referred to as front face and rear face), for example disc-shaped, which extend
25 perpendicularly to the cross-sectional plane of the figures. Furthermore, the multi-layer structure 30 and the substrates 40, 50 advantageously have a plane of symmetry, depicted as a chain-dotted line (and passing through the centre of the two main faces).

[0023] In a manner common to all the modes of implementation, the method for manufacturing the multi-layer structure 30 comprises the following steps S1 to S4:

- S1: providing a support substrate 40 comprising a support layer 41 and a porous silicon layer 42 disposed on the support layer 41 (see [Fig. 3A], [Fig. 4A], [Fig. 5A], [Fig. 6A], [Fig. 7A], [Fig. 8A] and [Fig. 9A]);
- S2: providing a donor substrate 50 comprising a first face 50A, a buried brittle plane 50B and a surface layer 51 delimited by the first face 50A and the buried brittle plane 50B (cf. [Fig. 3A], [Fig. 4A], [Fig. 5A], [Fig. 6A], [Fig. 7A], [Fig. 8A] and [Fig. 9A]);
- S3: assembling the support substrate 40 and the donor substrate 50 by bonding, the surface layer 51 of the donor substrate 50 being disposed in contact with the support substrate 40 (cf. [Fig. 3B], [Fig. 4B], [Fig. 5B], [Fig. 6B], [Fig. 7B], [Fig. 8B] and [Fig. 9B]); and
- S4: separating the surface layer 51 from the donor substrate 50 by fracturing along the buried brittle plane 50B (see [Fig. 3C], [Fig. 4C], [Fig. 5C], [Fig. 6C], [Fig. 7C], [Fig. 8C] and [Fig. 9C]).

[0024] The multi-layer structure 30 comprising the porous silicon layer 42 is adapted to radio frequency applications targeting:

- low insertion losses (low signal attenuation) and good linearity (low signal distortion leading to harmonics);
- temperature stability, in particular in the range of use for RF integrated circuits [-40°C to 150°C], and even up to 225°C;
- low capacitive coupling between the RF integrated circuits and the support layer 41, typically by virtue of a dielectric permittivity lower than that of silicon.

[0025] The support layer 41 of the support substrate 40 is for ensuring mechanical strength of the multi-layer structure 30, especially so that it can be handled during the microelectronic component manufacturing steps. Its thickness may be between 500 μm and 1 mm. The support layer 41 preferably consists of silicon. Advantageously, the silicon of the support layer 41 has an electrical resistivity between 5 m $\Omega\cdot\text{cm}$ and 20 $\Omega\cdot\text{cm}$, preferably between 0.5 $\Omega\cdot\text{cm}$ and 4 $\Omega\cdot\text{cm}$.

[0026] The porous silicon layer 42 comprises hollow pores, the diameter of which is preferably between 2 nm and 50 nm. By hollow pores, it is meant pores that are not

completely filled with a solid material. The inner walls of the pores are advantageously lined with oxide, for example silicon dioxide (SiO_2). The fact that the inner walls of the pores are lined with oxide reflects a stabilised state of the porous silicon layer 42, in which dangling bonds of the Si-Hx type have predominantly been replaced with much more stable Si-O-Si bonds. This improves the mechanical stability of the porous silicon layer 42.

[0027] Advantageously, the porosity of the porous silicon layer 42 is between 40% and 70%. This level of porosity ensures good balance between mechanical properties and electrical properties of the porous silicon layer 42.

10 [0028] The porous silicon layer 42 advantageously has a resistivity greater than 20 $\text{k}\Omega\cdot\text{cm}$.

[0029] The thickness of the porous silicon layer 42 is preferably between 5 μm and 50 μm . The thickness of the porous silicon layer 42, combined with its morphology (pore diameter, porosity rate), defines the mechanical strength of the porous silicon layer 42.

[0030] With reference to Figs. 3A, 4A, 5A, 6A, 7A, 8A and 9A, the step S1 of providing the support substrate 40 may comprise a sub-step of porosifying a surface portion of a first silicon substrate. By surface portion (or layer), it is meant a portion (layer) which extends from a (main) face of the first substrate. The porosified portion of the first substrate constitutes the porous silicon layer 42, while the remaining, non-porosified portion of the first substrate constitutes the support layer 41.

[0031] The porosification step is generally carried out electrochemically or photoelectrochemically. It is based on an anodic dissolution phenomenon in an acidic medium, from silicon of the first substrate. For example, the first substrate is soaked in a hydrofluoric acid (HF) based solution. The first substrate is in contact with an anode and a cathode is placed opposite the face to be porosified on the first substrate.

[0032] There are different configurations of porosification equipment. The most common configurations are referred to as "single cell" and "double cell". In the first case, only one face of the first substrate is in contact with the acidic medium. In the second case, both faces of the first substrate are in contact with the acidic medium, this acidic medium comprising either the same solution for both faces, or two different solutions.

[0033] In one alternative implementation, only the surface portion (to be porosified) of the first substrate is of silicon. The remaining portion of the first substrate, intended to form the support layer 41, may consist of another material (semiconductor or not).

[0034] After the porosification sub-step, step S1 of providing the support substrate 40 advantageously comprises a sub-step of annealing the porous silicon layer 42 under an oxidising atmosphere at a temperature between 300°C and 400°C, so as to stabilise the porous silicon layer 42. Preferably, the duration of the annealing under an oxidising atmosphere is between 5 min and 200 min.

[0035] This annealing makes it possible to replace predominantly dangling bonds of the Si-Hx type, in particular present on the inner walls of the pores, with much more stable Si-O-Si bonds.

[0036] Advantageously, annealing under an oxidising atmosphere is followed by annealing in a neutral atmosphere, for example nitrogen, at a temperature between 400°C and 450°C, for example 420°C. Annealing in a neutral atmosphere typically lasts between 2 and 16 hours, for example 10 hours.

[0037] Annealing in a neutral atmosphere especially avoids degassing during heat treatments subsequently applied to the multi-layer structure 30, this degassing being likely to degrade quality of said structure. Furthermore, annealing in a neutral atmosphere tends to stabilise curvature of the support substrate 40 provided with the porous silicon layer 42, limiting the curvature phenomenon of the multi-layer structure 30 after these heat treatments.

[0038] Finally, step S1 of providing the support substrate 40 may include a sub-step of forming a dielectric layer 43 on the porous silicon layer 42. The dielectric layer 43 is an electrically insulating layer. It may consist of a nitride, for example silicon nitride (Si_3N_4), or an oxide such as silicon dioxide (SiO_2) or aluminium oxide (Al_2O_3). Its thickness can be between 200 nm and 2 μm .

[0039] The dielectric layer 43 can be formed by a chemical vapour deposition technique, for example Low Pressure Chemical Vapour Deposition (LPCVD), Plasma Enhanced Chemical Vapour Deposition (PECVD) or even High Density Plasma-Chemical Vapour Deposition (HDP-CVD).

[0040] Still with reference to Figs. 3A, 4A, 5A, 6A, 7A, 8A and 9A, at least one so-called "active" part of the surface layer 51 of the donor substrate 50 is formed of a

material selected from silicon, germanium, silicon carbide, piezoelectric materials (for example LiNbO_3 , LiTaO_3 ...) and binary, ternary or quaternary alloys of type IV-IV (e.g. SiGe), III-V or II-VI semiconductor materials. The surface layer 51 is intended to be transferred onto the support substrate 40 and its active part is intended to receive
 5 active components, such as transistors, upon manufacturing microelectronic components from the multi-layer structure 30. The thickness of the active part is preferably between 50 nm and 1.5 μm .

[0041] The surface layer 51 can be formed by a thin film (50 nm - 1.5 μm) of piezoelectric material or semiconductor material (silicon, germanium, silicon carbide,
 10 type IV-IV, III-V or II-VI alloys, etc.), intrinsic or doped (see Figs. 3A, 4A, 5A, 6A and 9A). It is then entirely intended to receive the active components. This is also known as the active layer.

[0042] Alternatively, the surface layer 51 may be formed of a stack of several sublayers (see Figs. 7A and 8A), for example a stack comprising an active sublayer
 15 511 of a piezoelectric or semiconductor material (whose thickness may be between 50 nm and 1.5 μm) and a dielectric sublayer 512 disposed on the active sublayer 511 (and whose thickness may be between 50 nm and 500 nm).

[0043] The step S2 of providing the donor substrate 50 preferably comprises a sub-step of forming the buried brittle plane 50B in a second substrate. Preferably, the
 20 second substrate consists of a material selected from silicon, germanium, silicon carbide, piezoelectric materials (for example LiNbO_3 , LiTaO_3 ...) and binary, ternary or quaternary alloys of type IV-IV (e.g. SiGe), III-V or II-VI semiconductor materials.

[0044] The buried brittle plane 50B is advantageously formed by implanting light ions through a first face of the second substrate. Ions are implanted into the second
 25 substrate at a given implantation depth, measured from the first face of the second substrate. The implantation depth can be between 50 nm and 1.5 μm , for example 400 nm. Light ions herein designate ions of chemical species with an atomic number less than or equal to 5. Light ions are preferably hydrogen or helium ions, as these ions are conducive to the formation of microcavities around the implantation depth, giving rise
 30 to the buried brittle plane 50B, as described in the method for manufacturing SOI substrates known as Smart Cut™ (registered trademark).

[0045] Before or after the implantation sub-step, the step S2 of providing the donor substrate 50 may also comprise depositing a dielectric sublayer 512 (see Figs. 7A and 8A) onto the first face of the second substrate (this dielectric sublayer 512 forming part of the surface layer 51).

5 [0046] Steps S3 and S4 described hereafter relate to the transfer of the surface layer 51 from the donor substrate 50 to the support substrate 40.

[0047] The step S3 of assembling the support substrate 40 and the donor substrate 50 consists in bonding the donor substrate 50 on the side of its first face 50A to the support substrate 40. This assembly step S3 is also referred to as the step of
10 transferring the donor substrate 50 onto the support substrate 40.

[0048] In a preferred mode of implementation of the assembly step S3 illustrated by Figs. 3B, 4B, 5B, 6B and 9B, the surface layer 51 of the donor substrate 50 is brought into contact with the dielectric layer 43 of the support substrate 40.

[0049] In one alternative implementation illustrated by Fig. 7B, the surface layer 51
15 comprises on the surface a dielectric sublayer 512 which is brought into contact with the dielectric layer 43 of the support substrate 40. The dielectric sublayer 512 of the donor substrate 50 and the dielectric layer 43 of the support substrate 40 are advantageously formed of the same dielectric material, preferably an oxide (e.g. SiO₂).

[0050] Finally, in one alternative implementation represented by Fig. 8B, the
20 support substrate 40 is free of a dielectric layer 43 and the surface layer 51 comprises on the surface a dielectric sublayer 512 which is brought into contact with the porous silicon layer 42 of the support substrate 40.

[0051] Assembling the support and donor substrates 40, 50 can be achieved by any known bonding technique, preferably by molecular adhesion direct bonding. This
25 technique will not be described in detail herein. It should nevertheless be noted that, prior to bonding, the support substrate 40 and the donor substrate 50 have preferably undergone cleaning and/or surface activation sequences, in order to guarantee quality of the bonding interface in terms of defectivity and bonding energy. Furthermore, the support substrate 40 and the donor substrate 50 have preferably undergone a
30 polishing step (for example by Chemical Mechanical Planarisation or CMP) of their bonding surface so as to obtain a surface roughness of strictly lower than 0.7 nm. This roughness value, as well as all those given hereafter, are expressed as a root mean

square value. The root-mean-square roughness (noted Rq) is determined by statistical analysis of an atomic force microscope image, taking a surface area of $1 \times 1 \mu\text{m}^2$ as the sample.

[0052] The step S4 of separating the surface layer 51 by fracturing along the buried brittle plane 50B makes it possible to detach the surface layer 51 from the donor substrate 50 and thus obtain the multi-layer structure 30 on the one hand, and the remainder of the donor substrate 50 on the other hand. The remainder of the donor substrate 50 can be reused to transfer other surface layers during new iterations of the manufacturing method.

[0053] Preferably, step S4 of separating the surface layer 51 comprises a heat treatment. For a silicon surface layer 51 (or active sublayer 511), this heat treatment is carried out at a temperature between 200°C and 500°C , preferably between 350°C and 450°C . Such a heat treatment is able to increase the embrittlement level of the buried brittle plane 50B, which phenomenon underlies the Smart Cut™ method.

[0054] A temperature in the order of 400°C is advantageous in that the assembly is subject to fewer mechanical stresses due to the different coefficients of expansion of the materials making up the support substrate 40 and the donor substrate 50. Indeed, excessively high stresses are likely to affect integrity of the porous silicon layer 42.

[0055] After the separation step S4, the method for manufacturing the multi-layer structure 30 may include one or more heat treatment steps to improve crystal quality and/or the surface state (roughness, defectivity) of the surface layer 51 (so-called finish annealing of the surface layer 51) or to consolidate the bonding interface (so-called consolidation annealing of the interface).

[0056] In the modes of implementation of Figs. 3A-3C, 4A-4C, 5A-5C, 6A-6C, 7A-7C and 8A-8C, the support substrate 40 further comprises a non-porous silicon (or bulk silicon) peripheral portion 44 disposed around the porous silicon layer 42. In other words, the porous silicon layer 42 does not extend to the flank of the support substrate 40. This is especially the case when "double cell" type porosification equipment has been used to form the porous silicon layer 42 (a peripheral seal rests on the face of the first substrate in contact with the acidic medium). The non-porous silicon peripheral portion 44 has a width L1 which ranges from 1 mm to 5 mm (depending on the

equipment used, for example). The width of a portion of a substrate herein designates the dimension of this portion measured along a radius of said substrate. The thickness of the peripheral portion 44 is equal to the thickness of the porous silicon layer 42.

[0057] The peripheral portion of non-porous silicon 44 tends to decrease the curvature of the multi-layer structure 30 during subsequent heat treatment steps (steps of finishing the surface layer 51 or manufacturing the components). On the other hand, it is responsible for circular arc cracks which may appear in the surface layer 51 during the separation step S4.

[0058] The separation of the surface layer 51 is the result of the propagation of at least one fracture wave in the buried brittle plane 50B. The fracture wave originates at one point in the buried brittle plane 50B, typically at the edge (typically circular), and propagates in all directions of the buried brittle plane 50B, in the case set forth herein at different speeds due to the heterogeneous composition of the underlying support substrate 40. More particularly, the fracture wave propagates much faster over non-porous silicon than over porous silicon, which further absorbs the fracture energy. This is the cause of the cracks observed.

[0059] In order to drastically reduce the risk of cracks in the surface layer 51 during the separation step S4, at least one of the support and donor substrates 40, 50 comprises a degraded portion 60, configured so as not to be bonded to the other of the support and donor substrates 40, 50 during the assembly step S3. Thus, the bonding of the support and donor substrates 40, 50 is only partial (i.e. it occurs outside the degraded portion or portions 60). The substrate comprising the degraded portion 60 is referred to hereinafter as the degraded substrate.

[0060] This local absence of bonding between the support substrate 40 and the donor substrate 50 results in that cracking cannot be achieved (in the buried brittle plane 50B) facing the degraded portion 60 due to the lack of a stiffener. Consequently, the surface layer 51 of the donor substrate 50 is not transferred to the support substrate 40 facing the degraded portion 60.

[0061] The degraded portion 60 has an annular or substantially annular shape. The expression "substantially annular" refers to a segment of a ring, this segment having a circumference (or external perimeter) greater than or equal to 90% of the circumference of the ring (as a whole). It can also refer to several segments of the

same ring whose total circumference is greater than or equal to 90% of the circumference of the ring.

[0062] In the first mode of implementation represented by Figs. 3A-3C, the degraded substrate is the donor substrate 50. In other words, the degraded portion 60 belongs to the donor substrate 50. It is located, in the assembly of substrates 40 and 50, in vertical alignment with the interface between the porous silicon layer 42 and the peripheral non-porous silicon portion 44 (in other words, the vertical projection of the interface passes through the degraded portion 60). Furthermore, it extends to the flank of the degraded substrate (herein the donor substrate 50).

[0063] The degraded portion 60 of Figs. 3A-3C is formed by a recessed portion relative to the first face 50A of the donor substrate 50. This recessed portion, also referred to as a setback portion, can be obtained by forming a cavity (annular or substantially annular) in the donor substrate 50 from the first face 50A (see Fig. 3A). The depth P of this cavity, measured from the first face 50A, is greater than the topology of the edge of the support substrate 40 (so as not to risk bonding to the support substrate). Furthermore, it is advantageously greater than the depth of implantation of the light ions to form the buried brittle plane 50B. It is preferably between 200 nm and 10 μm , for example 6 μm . The cavity can be obtained by etching or micro-milling.

[0064] One advantage of this first mode of implementation is that the surface layer 51 transferred onto the support substrate 40 then has a clean contour (see Fig. 3C). Additionally, when the depth P of the cavity is greater than or equal to twice the implantation depth, the donor substrate 50 can be reused without the need to form the cavity again.

[0065] In the second mode of implementation represented by Figs. 4A-4C, the degraded substrate is instead the support substrate 40. Stated differently, the degraded portion 60 belongs to the support substrate 40. As previously, it extends from the flank of the degraded substrate (herein the support substrate 40) until it reaches or projects from the vertical projection of the interface between the porous silicon layer 42 and the peripheral portion 44.

[0066] The degraded portion 60 of Figs. 4A-4C consists of a textured portion of the dielectric layer 43, this portion being textured so as to have a surface roughness

greater than or equal to 1 nm. Indeed, too high a roughness prevents the support substrate 40 and the donor substrate 50 from bonding. Apart from the degraded portion 60, the surface roughness of the support and donor substrates 40, 50 is therefore strictly lower than 1 nm.

5 [0067] The textured portion can be obtained by etching the dielectric layer 43, by chemical treatment, by plasma treatment, by ion beam bombardment, by nanosecond laser annealing or by applying (punching) a textured ring to create defects.

[0068] In a first alternative implementation (not represented by the figures), the degraded portion 60 is a textured portion ($R_q \geq 1$ nm) belonging to the donor substrate
10 50, and more particularly to the surface layer 51.

[0069] In a second alternative implementation (also not represented by the figures), the degraded portion 60 is a recessed portion belonging to the support substrate 40, and more particularly to the dielectric layer 43. The depth of the corresponding cavity is preferably strictly lower than the thickness of the dielectric layer 43.

15 [0070] Thus, in these first two modes of implementation and their alternatives, the degraded portion 60 is arranged so as to obtain a fracture wave which propagates above a homogeneous medium comprising the porous silicon layer 42. Hence, there are no cracks. The width L2 of the degraded portion 60 is strictly greater than the width L1 of the peripheral portion 44, and preferably between 2 mm and 6 mm.

20 [0071] In the third mode of implementation represented by Figs. 5A-5C, the degraded portion 60 belongs to the support substrate 40. It is also located (in the assembly of substrates 40 and 50) in vertical alignment with the interface between the porous silicon layer 42 and the peripheral portion 44. On the other hand, and in contrast to the second mode of implementation (Figs. 4A-4C), it does not extend to the flank of
25 the support substrate 40. Stated differently, it is spaced from the flank of the support substrate 40. It is located at a distance d of less than 5 mm from the flank of the support substrate 40.

[0072] The degraded portion 60 may be formed by a recessed portion of the dielectric layer 43, as is represented in Figs. 5A-5C (and as in the second alternative
30 implementation), or by a textured portion of high roughness of the dielectric layer 43 (as in the mode of implementation in Figs. 4A-4C).

[0073] In the fourth mode of implementation represented by Figs. 6A-6C, the degraded portion 60 belongs to the donor substrate 50. It is also located in vertical alignment with the interface between the porous silicon layer 42 and the peripheral portion 44. However, unlike the first mode of implementation (Figs. 3A-3C), it does not extend to the flank of the donor substrate 50. It is nevertheless located at a distance d of less than 5 mm from the flank of the donor substrate 50. The degraded portion 60 may be formed by a portion set back relative to the first face 50A of the donor substrate 50, as is represented in Figs. 6A-6C (and as in the mode of implementation in Figs. 3A-3C), or by a textured portion of high roughness of the surface layer 51 (as in the first alternative mode of implementation).

[0074] In these third and fourth modes of implementation, the degraded portion 60 is arranged so as to obtain two fracture waves each propagating in a specific region (peripheral or central) of the buried brittle plane 50B, above a homogeneous medium (comprising either the porous silicon layer 42 or the peripheral portion 44). There are therefore only two fracture fronts which have not the possibility to meet, given that the fracture waves do not propagate facing the degraded portion 60 (absence of bonding of the surface layer 51). The width $L3$ of the degraded portion 60 is preferably between 10 μm and 4 mm.

[0075] The third and fourth modes of implementation of the manufacturing method further make it possible to obtain an (annular) portion of active layer at the periphery of the multi-layer structure 30 (unlike the preceding modes of implementation), which may prove useful for the integration of microelectronic components.

[0076] In the fifth mode of implementation represented by Figs. 7A-7C, the degraded portion 60 consists of a cavity (annular or substantially annular) which extends (from the bonding face of the support substrate 40) into the porous silicon layer 42, at a distance d of less than 7 mm from the flank of the support substrate 40 and at a distance d' of less than 2 mm from the interface between the porous silicon layer 42 and the peripheral portion 44. Cavity 60 can be formed by etching, micro-milling or nanosecond laser annealing. Its width $L4$ is preferably between 10 μm and 1 mm.

[0077] Advantageously, the cavity 60 extends through the entire thickness of the porous silicon layer 42.

[0078] This cavity 60 allows the porous silicon layer 42 to deform (or rearrange) at least in part along the flank rather than vertically, as well as avoiding protrusions or inhomogeneities which can impair bonding quality (and therefore create non-transferred zones).

5 [0079] A dielectric material, typically that forming the dielectric layer 43, may cover the bottom and side walls of the cavity 60, without however filling it completely. Additionally, cavity 60 can be (with or without a dielectric coating on the bottom and side walls) partially or completely filled with a material that absorbs the fracture wave, thus forming a box of absorbing material. The absorbing material has a Young's
10 modulus lower than that of porous silicon (i.e. less than 20 GPa).

[0080] Once again, the cavity 60 or the absorbing box makes it possible to distinguish two distinct zones for the propagation of fracture waves, above a homogeneous or practically homogeneous medium, which prevents the appearance of cracks.

15 [0081] In the sixth mode of implementation represented by Figs. 8A-8C, the degraded portion 60 is made on either of the substrates 40-50 (on both in the example of Figs. 8A-8C) by optimising the wafer edge chamfers. This optimisation is made, for example, by edge-grinding so that the chamfered part of the wafer edge (constituting the degraded portion 60) extends up to the porous silicon layer 42 (before assembly
20 when it belongs to the support substrate 40 and after assembly when it belongs to the donor substrate 50) so that there can be no bonding beyond the porous silicon layer 42.

[0082] In the seventh mode of implementation represented by Figs. 9A-9C, the porous silicon layer 42 comprises a central portion 421 having a substantially constant
25 thickness e_1 and a peripheral portion 422 of increasing thickness e_2 towards the flank of the support substrate 40. By substantially constant, it is meant that the thickness e_1 of the central portion 421 does not vary by more than 5%. On the other hand, the thickness e_2 of the peripheral portion 422 may vary by more than 30% between the interface with the central portion 421 and the flank of the support substrate 40.

30 [0083] Such a porous silicon layer 42 is especially obtained when "single cell" type porosification equipment is used (for the record, one entire face of the first substrate is

exposed to the acidic medium). The peripheral portion 422 of increasing thickness has a width $L1'$ which can vary between 2 mm and 25 mm.

[0084] In this case, the multi-layer structure 30 is practically unaffected by the cracking phenomenon, as the fracture wave propagates above an overall homogeneous (composition) medium. On the other hand, the inhomogeneity of the thickness of the porous silicon at the edge of the wafer is responsible for an increase in the curvature of the multi-layer structure 30 during annealing, especially during consolidation annealing of the bonding interface, which can reach 1000°C (the multi-layer structure 30 can have a deflection of 600 μm after annealing).

[0085] In order to limit or cancel the effect of the thickness gradient, and thus reduce the curvature of the multi-layer structure 30, a degraded portion 60 is arranged in at least one of the support and donor substrates 40, 50. The degraded portion 60 is located, in assembling the support substrate 40 and the donor substrate 50, in vertical alignment with the transition between the central portion 421 and the peripheral portion 422 of the porous silicon layer 42.

[0086] The degraded portion 60 may be a recessed portion, a textured portion (with a roughness greater than or equal to 1 nm; see Figs. 9A-9C), a cavity (filled or not with absorbent material), or a chamfered portion of wafer edge, as described previously. It can extend to the flank of the degraded substrate ($L2 > L1'$). Its width $L2$ is then advantageously between 3 mm and 26 mm.

[0087] The recessed portion in the dielectric layer 43 is the most favourable solution, as the dielectric layer 43 also plays a role in the curvature of the multi-layer structure 30.

[0088] More generally, the degraded portion 60 is located less than 25 mm from the flank of the degraded substrate, and preferably less than 7 mm in the mode of implementation of Figs. 7A-7C and less than 5 mm in the modes of implementation of Figs. 3A-3C, 4A-4C, 5A-5C, 6A-6C and 8A-8C. Thus, the risks of cracks in the surface layer 51 and/or excessive curvature of the multi-layer structure 30 caused by inhomogeneities at the edge of the assembly can be reduced.

[0089] Figs. 10A-10C represent a mode of implementation for the step of providing the support substrate 40, making it possible to recreate the structure comprising a peripheral portion of non-porous silicon 44 (cf. Figs. 3A-3C, 4A-4C, 5A-5C, 6A-6C, 7A-

7C, 8A-8C), even though "single cell" type porosification equipment is employed to form the porous silicon layer 42.

[0090] In a first sub-step S11 illustrated in Fig. 10A, a first silicon substrate 90 is recessed (for example by etching) so as to form a central cavity 91 laterally delimited by a ring 92 (of silicon). The ring 92 constitutes a peripheral portion of the first substrate 90.

[0091] The thickness e_3 of this ring 92 (equal to the etching depth) is greater than or equal to the maximum thickness (e_2) of the porous silicon layer to be formed (i.e. the thickness at the flank). Thus, during the second porosification sub-step S12 by means of "single cell" type porosification equipment (see Fig. 10B), the porous silicon layer 42' formed does not extend to the entire ring 92. A buried portion 921 of the ring 92 is left intact. Preferably, the width L_5 of the ring 92 is such that the peripheral portion of increasing thickness of the porous silicon layer 42' lies entirely within the ring 92.

[0092] Finally, in a third sub-step S23 (see Fig. 10C), the ring 92 is removed entirely so as to obtain a planar surface with the central portion (of substantially constant thickness e_1) of the porous silicon layer 42'.

[0093] The delimitation of a ring 92 at the periphery of the first substrate 90 during the first sub-step S11 therefore makes it possible to protect an underlying silicon portion of the porosification method (forming said peripheral portion 44 of the support substrate 40), this silicon portion being disposed around the porous silicon portion finally retained (forming said porous silicon layer 42 of the support substrate 40).

[0094] This particular mode of implementation of step S1 of providing the support substrate 40 also avoids the porous silicon extending over the flank of the multi-layer structure 30, which may be a source of brittleness or contamination (e.g. infiltration of etching or cleaning solutions, etc. employed during component manufacture).

[0095] As previously indicated, the degraded portion 60 of the support substrate 40 or donor substrate 50 may have a shape that is not completely annular ("substantially annular"). In other words, a portion of the support substrate 40 or donor substrate 50 may be left intact for the purpose of creating a fracture initiation zone at the edge.

[0096] Fig. 11 represents, by way of example, the bonding face of the support substrate 40 of Fig. 4A. The dotted circle represents the interface between the porous

silicon layer 42, in the centre of the substrate, and the peripheral non-porous silicon portion 44. A non-degraded portion 70 (herein of the dielectric layer 43) is located as an extension of the degraded portion 60 as a ring segment, so that it completes the ring. By "non-degraded portion", it is meant a portion which is bonded to the other of the substrates during assembly step S3.

[0097] The non-degraded portion 70 is advantageously arranged so as to encompass a notch 80 in the support substrate 40 (or donor substrate 50), as is represented in Fig. 11.

[0098] With reference to Figs. 3C, 4C, 5C, 6C, 7C, 8C and 9C, the multi-layer structure 30 thus comprises the support layer 41, the porous silicon layer 42 disposed on the support layer 41, a dielectric layer 43, 512 (dielectric layer 43 and/or dielectric sublayer 512) disposed on the porous silicon layer 42 and an active layer 51, 511 (surface/active layer 51 or active sublayer 511) disposed on the dielectric layer 43, 512.

[0099] In the case of an oxide, the dielectric layer 43, 512 may also be referred to as a buried oxide layer or BOX.

[00100] A feature of the multi-layer structure 30 is that the active layer 51, 511 comprises an annular or substantially annular recess 510. The recess 510 extends up to the dielectric layer 43, stated differently over the entire thickness of the active layer 51, 511. As such, the active layer 51, 511 does not completely cover the support layer 41.

[00101] Such a recess in the active layer 51, 511 near the flank of the multi-layer structure 30 is much less damaging than excessive curvature or cracks for microelectronic component manufacturing (these cracks generally extending much further towards the centre of the wafer).

CLAIMS

[Claim 1] A method for manufacturing a multi-layer structure (30), comprising the following steps of:

- 5 – providing (S1) a support substrate (40) comprising a support layer (41) and a porous silicon layer (42) disposed on the support layer;
- providing (S2) a donor substrate (50) comprising a first face (50A), a buried brittle plane (50B) and a surface layer (51) delimited by the first face and the buried brittle plane;
- 10 – assembling (S3) the support substrate (40) and the donor substrate (50) by bonding, the surface layer (51) of the donor substrate being disposed in contact with the support substrate;
- separating (S4) the surface layer (51) from the donor substrate (50) by fracturing along the buried brittle plane (50B);

15 which method is characterised in that at least one of the support and donor substrates (40, 50), called a degraded substrate, comprises a degraded portion (60) so as to prevent it from being bonded to the other of the support and donor substrates (50, 40) during the assembly step, the degraded portion (60) having an annular or substantially annular shape and being located less than 25 mm from the flank of said degraded substrate.

20 [Claim 2] The method according to claim 1, wherein the support substrate (40) further comprises a non-porous silicon peripheral portion (44) disposed around the porous silicon layer (42) and in which the degraded portion (60) is located, in assembling the support substrate (40) and the donor substrate (50), in vertical alignment with an interface between the non-porous silicon peripheral portion (44) and
25 the porous silicon layer (42).

 [Claim 3] The method according to claim 1, wherein the porous silicon layer (42) comprises a central portion (421) having a substantially constant first thickness (e1) and a peripheral portion (422) having a second thickness (e2) increasing towards the flank of the support substrate (40) and in which the degraded portion (60) is located,
30 in assembling the support substrate (40) and the donor substrate (50), in vertical

alignment with a transition between the central portion (421) and the peripheral portion (422) of the porous silicon layer (42).

[Claim 4] The method according to any of claims 1 to 3, wherein the degraded portion (60) further extends to the flank of said degraded substrate.

5 [Claim 5] The method according to any of claims 1 to 3, wherein the degraded portion (60) is spaced from the flank of said degraded substrate and has a width (L3) between 10 μm and 4 mm.

[Claim 6] The method according to any of claims 1 to 5, wherein the degraded portion (60) consists of a recessed portion.

10 [Claim 7] The method according to claim 6, wherein the recessed portion belongs to the donor substrate (50).

[Claim 8] The method according to claim 7, wherein the step (S2) of providing the donor substrate (50) comprises a sub-step of implanting light ions into a first substrate at an implantation depth to form the buried brittle plane (50B), the recessed portion
15 being obtained by forming a cavity with a depth (P) greater than the implantation depth.

[Claim 9] The method according to any of claims 1 to 5, wherein the degraded portion (60) consists of a textured portion having a surface roughness greater than or equal to 1 nm.

[Claim 10] The method according to claim 1, wherein the support substrate (40)
20 further comprises a non-porous silicon peripheral portion (44) disposed around the porous silicon layer (42) and in which the degraded portion (60) consists of a cavity extending into the porous silicon layer (42) and located at a distance (d') of less than 2 mm from an interface between the non-porous silicon peripheral portion (44) and the porous silicon layer (42).

25 [Claim 11] The method according to claim 10, wherein the cavity is filled with a material having a Young's modulus lower than that of porous silicon.

[Claim 12] The method according to any of claims 1 to 11, wherein the support substrate (40) further comprises a dielectric layer (43) disposed on the porous silicon layer (42).

30 [Claim 13] The method according to any of claims 1 to 12, wherein the degraded portion (60) is substantially annular and wherein said degraded substrate comprises a

so-called non-degraded portion (70) located as an extension of the degraded portion (60), said non-degraded portion (70) being bonded to the other of the support and donor substrates (50, 40) during the assembly step (S3).