CLAIMS

1. A semiconductor device comprising:

a stacked vertical transistor memory cell including:

a bottom tier including a plurality of bottom vertical transistors having a merged top source/drain epitaxial region (epi), including at least one non-floating transistor and at least one floating transistor, the at least one floating transistor having at least one terminal being electrically disconnected from other transistors of the stacked vertical transistor memory cell;

a top tier including a plurality of top vertical transistors having a merged bottom source/drain epi; and

a cross-coupling including epi connections and gate to epi connections between the top tier and the bottom tier.

2. The device of claim 1, wherein:

the plurality of bottom vertical transistors including first non-floating and floating transistors, and second non-floating and floating transistors; and

the plurality of top vertical transistors includes first, second, third and fourth top vertical transistors.

3. The device of claim 2, wherein the cross-coupling includes:

epi connections by the merged top source/drain epi between the first non-floating and floating transistors, and the second non-floating and floating transistors;

epi connections by the merged bottom source/drain epi between the first and third top vertical transistors, and the second and fourth top vertical transistors;

gate to epi connections by metal between the first non-floating transistor and the second floating transistor, and the second non-floating transistor and the first floating transistor; and

gate to epi connections by metal between the first and second top vertical transistors, and the third and fourth top vertical transistors.

4. The device of claim 2, wherein the plurality of bottom vertical transistors include n-type field-effect transistors (nFETs) and the plurality of top vertical transistors include p-type field-effect transistors (pFETs).

5. The device of claim 2, wherein the plurality of bottom vertical transistors further includes respective bottom source/drain epis and the plurality of top vertical transistors further includes respective top source/drain epis.

6. The device of claim 5, further comprising dielectric layers separating the bottom source/drain epis and the top source/drain epis, and isolation layers separating the bottom tier and the top tier.

7. The device of claim 1, further comprising wordline, bitline, supply voltage and ground contacts.

8. The device of claim 1, wherein the cross-coupling further contacts gate structures of the bottom and top tiers.

9. A semiconductor device comprising:

a stacked vertical transistor memory cell including:

a bottom tier including a plurality of bottom vertical transistors including n-type field-effect transistors (nFETs) having a merged top source/drain epitaxial region (epi), and gate structures, the plurality of bottom vertical transistors including first and second non-floating transistors and first and second floating transistors, wherein the first and second floating transistors have at least one terminal being electrically disconnected from other transistors of the stacked vertical transistor memory cell;

a top tier including a plurality of top vertical transistors including p-type field-effect transistors (pFETs) having a merged bottom source/drain epi, and gate structures, the plurality of top vertical transistors including first, second, third and fourth top vertical transistors; and

a cross-coupling contacting the gate structures of the bottom and top tiers, including:

epi connections by the merged top source/drain epi between the first non-floating and floating transistors, and the second non-floating and floating transistors;

epi connections by the merged bottom source/drain epi between the first and third top vertical transistors, and the second and fourth top vertical transistors;

gate to epi connections by metal between the first non-floating and second floating transistors, and the second non-floating and first floating transistors; and

gate to epi connections by metal between the first and second top vertical transistors, and the third and fourth top vertical transistors.

10. The device of claim 9, wherein the plurality of bottom vertical transistors further includes respective bottom source/drain epis and the plurality of top vertical transistors further includes respective top source/drain epis.

11. The device of claim 10, further comprising dielectric layers separating the bottom source/drain epis and the top source/drain epis, and isolation layers separating the bottom tier and the top tier.

12. The device of claim 9, further comprising wordline, bitline, supply voltage and ground contacts.

13. A method for fabricating a semiconductor device, comprising:

forming a stacked vertical transistor memory cell including:

a bottom tier having a plurality of bottom vertical transistors having a merged top source/drain epitaxial region (epi), the plurality of bottom vertical transistors including at least one non-floating transistor and at least one floating transistor; and a top tier having a plurality of top vertical transistors having a merged bottom source/drain epi; wherein the at least one floating transistor have at least one terminal being electrically disconnected from other transistors of the stacked vertical transistor memory cell, wherein forming the stacked transistor memory cell includes:

forming a cross-coupling including epi connections and gate to epi connections between the top tier and the bottom tier.

14. The method of claim 13, wherein:

the plurality of bottom vertical transistors including first non-floating and floating transistors, and second non-floating and floating transistors; and

the plurality of top vertical transistors includes first, second, third and fourth top vertical transistors.

15. The method of claim 14, wherein forming the cross-coupling further includes:

forming epi connections by the merged top source/drain epi between the first non-floating and floating transistors, and the second non-floating and floating transistors;

forming epi connections by the merged bottom source/drain epi between the first and third top vertical transistors, and the second and fourth top vertical transistors;

forming gate to epi connections by metal between the first non-floating and second floating transistors, and the second non-floating and first floating transistors; and

forming gate to epi connections by metal between the first and second top vertical transistors, and the third and fourth top vertical transistors.

16. The method of claim 14, wherein the plurality of bottom vertical transistors include n-type field-effect transistors (nFETs) and the plurality of top vertical transistors include p-type field-effect transistors (pFETs).

17. The method of claim 14, wherein the plurality of bottom vertical transistors further includes respective bottom source/drain epis and the plurality of top vertical transistors further includes respective top source/drain epis.

18. The method of claim 17, wherein the bottom source/drain epis and the top source/drain epis are separated by dielectric layer, and wherein the bottom tier and the top tier are separated by isolation layers.

19. The method of claim 13, wherein the semiconductor device includes wordline, bitline, supply voltage and ground contacts.

20. The method of claim 13, wherein forming the cross-coupling further includes contacting gate structures of the bottom and top tiers.