CLAIMS

What is claimed is:

1. An integrated circuit package, comprising:

an electronic interposer, wherein the electronic interposer comprises:

an upper section having between two and four layers, wherein each layer comprises an organic material layer and at least one conductive route comprising at least one conductive trace and at least one conductive via;

a lower section having between two and four layers, wherein each layer comprises an organic material layer and at least one conductive route comprising at least one conductive trace and at least one conductive via; and

a middle section between the upper section and the lower section, wherein the middle section comprises up to eight layers, wherein each layer comprises an organic material and at least one conductive route comprising at least one conductive trace and at least one conductive via, and wherein a thickness of each layer of the middle section is thinner than a thickness of any of the layers of the upper section and thinner than a thickness of any of the layers of the lower section;

at least one die side integrated circuit device having an active surface electrically attached to the electronic interposer, wherein the at least one die side integrated circuit device is at least partially encased in a mold material layer and wherein a back surface of the at least one die side integrated circuit device is in the same plane as an outer surface of the mold material layer; and

at least one stacked integrated circuit device electrically attached to the back surface of the at least one die side integrated circuit device through an interconnection structure formed

between the at least one die side integrated circuit device and the at least one stacked integrated circuit device.

2. The integrated circuit package of claim 1, wherein the interconnection structure abuts the back surface of the at least one die side integrated circuit device and abuts the outer surface of the mold material layer.

3. The integrated circuit package of claim 1, wherein the interconnection structure and the at least one stacked integrated circuit device are within a package module, wherein the package module comprises a support structure having a first surface and a second surface, wherein the interconnection structure is formed on the first surface of the support structure, wherein a plurality of module-to-device interconnects are formed on the second surface of the support structure and are electrically connected to the interconnection structure, and wherein the at least one stacked integrated circuit device is electrically attached to the interconnection structure.

4. The integrated circuit package of claim 3, further comprising a package mold material at least partially encasing the at least one stacked integrated circuit device.

5. The integrated circuit package of claim 1, wherein the thickness of each layer of the upper section is between 13 and 40 microns, wherein the thickness of each layer of the lower section is between 13 and 40 microns, and wherein the thickness of each layer of the middle section is between 1.5 and 9 microns.

6. The integrated circuit package of claim 1, wherein the at least one conductive trace of the upper section comprises a plurality of conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; wherein the at least one conductive trace of the lower section comprises a plurality of conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; and wherein the at least one conductive trace of the middle section comprises a plurality of conductive traces having a width between 0.75 microns and 3 microns, a spacing between 0.75 microns and 3 microns, and a thickness of between 0.5 microns and 4 microns, and wherein the at least one conductive via has a thickness of between 1 and 6 microns.

7. The integrated circuit package of claim 1, further comprising at least one high-density device-to-device conductive route within the middle section.

8. The integrated circuit package of claim 1, wherein at least one conductive trace of the middle section has a larger thickness in comparison with a thickness of another conductive trace of the middle section.

9. An electronic system comprising:

a board; and

an integrated circuit package electrically attached to the board, wherein the integrated circuit package comprises:

an electronic interposer, wherein the electronic interposer comprises;

an upper section having between two and four layers, wherein each layer comprises an organic material layer and at least one conductive route comprising at least one conductive trace and at least one conductive via;

a lower section having between two and four layers, wherein each layer comprises an organic material layer and at least one conductive route comprising at least one conductive trace and at least one conductive via; and

a middle section between the upper section and the lower section, wherein the middle section comprises up to eight layers, wherein each layer comprises an organic material and at least one conductive route comprising at least one conductive trace and at least one conductive via, and wherein a thickness of each layer of the middle section is thinner than a thickness of any of the layers of the upper section and thinner than a thickness of any of the layers of the lower section;

at least one die side integrated circuit device having an active surface electrically attached to the electronic interposer, wherein the at least one die side integrated circuit device is at least partially encased in a mold material layer and wherein a back surface of the at least one die side integrated circuit device is in the same plane as an outer surface of the mold material layer; and

at least one stacked integrated circuit device electrically attached to the back surface of the at least one die side integrated circuit device through an interconnection structure formed between the at least one die side integrated circuit device and the at least one stacked integrated circuit device.

10. The electronic system of claim 9, wherein the interconnection structure abuts the back surface of the at least one die side integrated circuit device and abuts the outer surface of the mold material layer.

11. The electronic system of claim 9, wherein the interconnection structure and the at least one stacked integrated circuit device are within a package module, wherein the package module comprises a support structure having a first surface and a second surface, wherein the interconnection structure is formed on the first surface of the support structure, wherein a plurality of module-to-device interconnects are formed on the second surface of the support structure and are electrically connected to the interconnection structure, and wherein the at least one stacked integrated circuit device is electrically attached to the interconnection structure.

12. The electronic system of claim 11, further comprising a package mold material at least partially encasing the at least one stacked integrated circuit device.

13. The electronic system of claim 9, wherein the thickness of each layer of the upper section is between 13 and 40 microns, wherein the thickness of each layer of the lower section is between 13 and 40 microns, and wherein the thickness of each layer of the middle section is between 1.5 and 9 microns.

14. The electronic system of claim 9, wherein the at least one conductive trace of the upper section comprises a plurality of conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; wherein the at

least one conductive trace of the lower section comprises a plurality of conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; and wherein the at least one conductive trace of the middle section comprises a plurality of conductive traces having a width between 0.75 microns and 3 microns, a spacing between 0.75 microns and 3 microns, and a thickness of between 0.5 microns and 4 microns, and wherein the at least one conductive via has a thickness of between 1 and 6 microns.

15. The electronic system of claim 9, further comprising at least one high-density device-to-device conductive route within the middle section.

16. The electronic system of claim 9, wherein at least one conductive trace of the middle section has a larger thickness in comparison with a thickness of another conductive trace of the middle section.

17. A method of fabricating an integrated circuit package, comprising:

forming an electronic interposer, wherein forming the electronic interposer comprises;

forming an upper section having between two and four layers, wherein each layer comprises an organic material layer and at least one conductive route comprising at least one conductive trace and at least one conductive via;

forming a lower section having between two and four layers, wherein each layer comprises an organic material layer and at least one conductive route comprising at least one conductive trace and at least one conductive via; and

forming a middle section between the upper section and the lower section, wherein the middle section comprises up to eight layers, wherein each layer comprises an organic material and at least one conductive route comprising at least one conductive trace and at least one conductive via, and wherein a thickness of each layer of the middle section is thinner than a thickness of any of the layers of the upper section and thinner than a thickness of any of the layers of the lower section;

forming at least one die side integrated circuit device;

electrically attaching an active surface of the at least one die side integrated circuit device to the electronic interposer;

at least partially encasing the at least one die side integrated circuit device in a mold material layer, wherein a back surface of the at least one die side integrated circuit device is in the same plane as an outer surface of the mold material layer; and

electrically attaching at least one stacked integrated circuit device to the back surface of the at least one die side integrated circuit device through an interconnection structure formed between the at least one die side integrated circuit device and the at least one stacked integrated circuit device.

18. The method of claim 17, wherein forming the interconnection structure comprises forming the interconnection structure to abut the back surface of the at least one die side integrated circuit device and to abut the outer surface of the mold material layer.

19. The method of claim 17, wherein the interconnection structure and the at least one stacked integrated circuit device are formed within a package module, wherein the package module comprises:

forming a support structure having a first surface and a second surface;

forming the interconnection structure on the first surface of the support structure;

forming a plurality of module-to-device interconnects on the second surface of the support structure, wherein the plurality of module-to-device interconnects are electrically connected to the interconnection structure; and

electrically attaching the at least one stacked integrated circuit device to the interconnection structure.

20. The method of claim 19, further comprising at least partially encasing the at least one stacked integrated circuit device in a package mold material.

21. The method of claim 17, further comprising forming at least one high-density device-to-device conductive route within the middle section.

22. The method of claim 17, wherein at least one conductive trace of the middle section has a larger thickness in comparison with a thickness of another conductive trace of the middle section.