

DESCRIPTION

TITLE: Substrate and the manufacturing method thereof for producing a wide bandgap bi-directional switch

TECHNICAL FIELD

5 The field of the invention is that of bi-directional switches made of wide bandgap materials, such as gallium nitride (GaN) and silicon carbide (SiC). The invention more specifically relates to a substrate and the manufacturing method thereof for producing a bi-directional switch with transistors connected vertically back-to-back.

PRIOR ART

10 In power electronics applications, such as electric vehicles, renewable energy generation, vehicle-to-vehicle communication and energy storage, bi-directional switches are particularly useful. These switches allow the flow of energy to be effectively controlled in both directions, which ensures reliable and safe operation under various operating conditions.

15 In the power device market, which is currently dominated by silicon devices, devices based on wide bandgap materials, such as GaN and SiC, are gradually increasing their market share. Indeed, the latter can operate at much higher temperatures and voltages, while offering higher power levels and lower losses.

20 GaN-based bi-directional switches typically have a lateral structure as shown, for example, in figure 15(a) of article [1] referenced at the end of the description. The separation between the drain and gate electrodes determines the breakdown voltage of these switches. The greater the separation, the higher the voltage that the switch can block. However, this then results in a significant chip footprint.

25 SiC-based bi-directional switches as shown, for example, in figure 15(b) in the same article [1], typically comprise two transistors with a common drain. These switches have two drift regions, one for each polarity of the blocking voltage. This also results in a significant chip footprint.

One solution for addressing this footprint problem is to vertically connect two MOS transistor cells back-to-back, as shown in figure 15(d) in the same article [1], so that they share a common drift region. This connection can be made in a common source or common drain configuration. The common source configuration allows bi-directional blocking and conduction to be controlled with a single gate control. The common drain configuration requires two separate gate controls.

As described in article [2] referenced at the end of the description, implementing this vertical back-to-back connection involves implementing double-sided lithography processes on a monocrystalline SiC substrate forming the shared drift region. The shared drift region made of monocrystalline SiC is 250 μm thick and has high resistivity: a differential on-state resistance of 140 $\text{m}\Omega\cdot\text{cm}^2$ is thus observed.

In addition, the polar nature of the SiC shared drift layer means that one face has a surface that is mainly formed by silicon atoms (known as the Si-type surface) and the other face has a surface that is mainly formed by carbon atoms (known as the C-type surface). The MOS transistor cell manufactured on the Si-type surface therefore has properties that differ from the MOS transistor cell manufactured on the C-type surface.

Indeed, the state of the surface of a layer formed by epitaxial growth differs depending on whether the layer is formed on the Si-type surface or on the C-type surface. On the one hand, on the C-type surface, the surface after epitaxy is rather flat with no macroscopic steps. On the other hand, on the Si-type surface, the surface after epitaxy exhibits 200-600 nm terraces with 2-8 nm steps.

Furthermore, the oxidation of the SiC occurs at a rate that is 8 to 15 times faster on the C-type surface than on the Si-type surface. After oxidation, the bandgap height is higher on the Si-type surface (2.7-2.8 eV) than on the C-type surface (2.4-2.5 eV).

As described in article [2], one consequence of the different properties is a very different threshold voltage between the two surfaces. Indeed, at room temperature this threshold voltage is 13.7 V on the C-type surface and 7.3 V on the Si-type surface. Furthermore, the difference in trap density at the interface makes the transistor channel prepared on the MOS transistor cell manufactured on the C-type surface much more

sensitive to temperature variations than the MOS transistor cell manufactured on the Si-type surface.

DISCLOSURE OF THE INVENTION

The aim of the invention is to propose a solution for designing a bi-directional switch with MOS transistors, connected vertically back-to-back, that exhibit similar properties.

To this end, the invention proposes a method for manufacturing a substrate for producing a bi-directional switch with transistors connected vertically back-to-back, comprising:

- providing a carrier substrate having a front face and a rear face;
- transferring a first seed layer made of a wide bandgap polar semiconductor material onto the front face of the carrier substrate, said first seed layer having a first type of surface and a second type of surface;
- transferring a second seed layer made of said wide bandgap polar semiconductor material onto the rear face of the carrier substrate, said second monocrystalline layer having a first type of surface and a second type of surface.

The transfers are carried out so as to expose the first type of surface of the first seed layer and the first type of surface of the second seed layer, with the second type of surface of the first seed layer and the second type of surface of the second seed layer being at the interface with the front face and the rear face of the carrier substrate, respectively.

Some preferred but non-limiting aspects of this method are as follows:

- transferring each of the first and second seed layers onto the front face and the rear face of the carrier substrate, respectively, comprises:
 - bonding a second type of surface of a donor substrate made of said wide bandgap polar semiconductor material onto the front face and the rear face of the carrier substrate, respectively, with the donor substrate having been previously implanted with ion species through its second type of surface in order to form a weakened plane therein;
 - delivering thermal and/or mechanical energy in order to separate the donor substrate in the vicinity of the weakened plane.

- it further comprises growing, on each of the first and second seed layers transferred onto the front face and the rear face of the carrier substrate, respectively, a drift layer made of a wide bandgap semiconductor material.
- the thickness of the drift layer deposited onto each of the first and second seed layers ranges between 5 and 100 μm .
- the drift layer deposited onto each of the first and second seed layers is doped.
- it further comprises implanting N-type or P-type impurities in the migration layer deposited onto each of the first and second seed layers.
- it further comprises depositing a gate oxide layer onto the migration layer deposited onto each of the first and second seed layers and forming a gate electrode on the gate oxide layer.
- the carrier substrate is made of a material with electrical resistivity of less than 20 $\text{m}\Omega\cdot\text{cm}$.
- the carrier substrate is a silicon carbide, aluminium nitride, diamond or gallium oxide substrate.
- the thickness of the carrier substrate ranges between 100 and 500 μm , and preferably ranges between 300 and 400 μm .
- the thickness of the first and second seed layers is less than or equal to 10 μm .
- the first type and the second type of surfaces of each one from among the first seed layer and the second seed layer are perpendicular faces, to within 15° , in opposite crystalline directions.
- each one from among the first and the second seed layers is a layer of SiC whose first type of surface is an Si-type surface.
- each one from among the first and the second seed layers is a layer of GaN whose first type of surface is a Ga-type surface.

The invention also relates to a substrate for producing a bi-directional switch with transistors connected vertically back-to-back, comprising:

- a carrier substrate having a front face and a rear face;
- a first seed layer transferred onto the front face of the carrier substrate, with the first seed layer being made of a wide bandgap polar semiconductor material and

having a first type of surface and a second type of surface, with the second type of surface of the first seed layer being at the interface with the front face of the carrier substrate;

- a second seed layer transferred onto the rear face of the carrier substrate, with the second seed layer being made of a wide bandgap polar semiconductor material and having a first type of surface and a second type of surface, with the second type of surface of the second seed layer being at the interface with the rear face of the carrier substrate.

A further aim of the invention is a bi-directional switch with transistors connected vertically back-to-back, integrating a substrate as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

Further aspects, aims, advantages and features of the invention will become more apparent from reading the following detailed description of preferred embodiments thereof, which are provided by way of a non-limiting example, and with reference to the accompanying drawings, in which:

- figure 1 illustrates various steps for manufacturing a substrate according to the invention;
- figure 2 is a schematic view of a substrate according to the invention;
- figure 3 is another schematic view of a substrate according to the invention after implementing a step of forming drift layers;
- figure 4 is a schematic view of a substrate according to the invention following the formation of MOS cells in the drift layers.

DETAILED DISCLOSURE OF SPECIFIC EMBODIMENTS

The invention relates to a substrate and the manufacturing method thereof for producing a bi-directional wide bandgap switch with transistors that are connected vertically back-to-back.

With reference to figure 1(A), such a method comprises providing a carrier substrate 1 with a front face and a rear face. This carrier substrate 1 can be made of a wide bandgap material, for example, of silicon carbide (for example, of the β -SiC type), of aluminium

nitride, of diamond or of gallium oxide. Wide bandgap is typically understood to mean a bandgap that is wider than that of silicon, that is, a bandgap typically ranging between 1.5 and 7 eV. The carrier substrate 1 is preferably a substrate with very low electrical resistivity, i.e., a substrate with electrical resistivity that is less than or equal to 20 mΩ.cm. The carrier substrate is, for example, polycrystalline, notably if it is made of silicon, diamond or aluminium nitride.

The thickness of the carrier substrate 1 can range between 100 and 500 μm, preferably between 300 and 400 μm. For a substrate with a diameter of 150 mm (for example, made of polycrystalline SiC), this thickness corresponds to the SEMI industry standard. For a 200 mm substrate (for example, made of polycrystalline SiC), this thickness may need to be adjusted relative to the current standard of 500 μm. In any case, beyond the thickness that needs to be adjusted prior to bonding, it may be worthwhile preparing a surface suitable for bonding, for both the front and rear faces of the substrate 1.

As illustrated in figure 2, the method further comprises transferring a first seed layer 21 onto the front face of the carrier substrate 1 and transferring a second seed layer 22 onto the rear face of the carrier substrate 1. "Seed layer" is understood to mean a monocrystalline growth seed layer. The thickness of each one from among the first and the second seed layers 21, 22 can be less than or equal to 10 μm, for example, the thickness can range between 400 and 800 nm.

The seed layers 21, 22 are made of a wide bandgap polar material. This material can be SiC (for example, 4H-SiC or 6H-SiC) or GaN. It should be noted that SiC or GaN seed layers can be transferred onto a polycrystalline SiC carrier substrate.

Due to their polar nature, a feature of the seed layers 21, 22 is to have a first type of surface F1 on one face and a second type of surface F2 on the other face.

The first type F1 and the second type F2 of surfaces correspond to faces that are perpendicular, to within 15°, in opposite crystalline directions. For example, these crystalline directions correspond to the positive direction along the c-axis (+c, (0001) plane) and the negative direction along the c-axis (-c, (000-1) plane). Thus, the first type of surface F1 can be defined as a surface whose crystalline off-cut relative to the (0001) axis of the crystal is less than 15°. Similarly, the second type of surface F2 can be defined as a surface

whose crystalline off-cut relative to the (000-1) axis of a crystal is less than 15°. It should be noted that this off-cut is based on the need for step-edge growth to promote the growth of a polytype or to minimise antiphase boundaries.

In the case of SiC, the Si face is the face oriented in the (0001) direction, while the C face is the face oriented in the (000-1) direction. The first type of surface F1 is then an Si-type surface mainly made up of silicon atoms, while the second type of surface F2 is then a C-type surface mainly made up of carbon atoms.

In the case of GaN, the Ga face is the face oriented in the (0001) direction, while the N face is the face oriented in the (000-1) direction. The first type of surface F1 is then a Ga-type surface mainly made up of gallium atoms, while the second type of surface F2 is then an N-type surface mainly made up of nitrogen atoms.

The respective transfers of the first seed layer 21 onto the front face of the carrier substrate and of the second seed layer 22 onto the rear face of the carrier substrate are carried out so as to expose the first type of surface F1 of the first seed layer 21 and the first type of surface F1 of the second seed layer 22. Thus, the second type of surface F2 of the first seed layer 21 and the second type of surface F2 of the second seed layer 22 are at the interface with the front face and the rear face of the carrier substrate, respectively. The first type of surface F1 is preferably the Si-type surface in the case of SiC and the Ga-type surface in the case of GaN. In this way, epitaxial growth of SiC or of GaN, respectively, on the first type of surfaces F1 of the seed layers 21, 22 is promoted. It should be noted in this respect that the first type of surface F1 of each of the seed layers 21, 22 preferably has an off-cut that is suitable for crystal growth thereon, for example, an off-cut ranging between 4° and 8° in the case of SiC.

In a preferred embodiment, each of the first and second seed layers 21, 22 is transferred onto the front face and the rear face of the carrier substrate, respectively, in accordance with the Smart Cut™ method. These transfers then involve bonding (see figure 1(B)) a second type of surface of a donor substrate 2 made of said wide bandgap polar semiconductor material onto the front face and the rear face of the carrier substrate 1, respectively, with the donor substrate having previously been implanted with ion species through its second type of surface in order to form a weakened plane 3 therein and having

previously received thermal and/or mechanical energy in order to separate the donor substrate in the vicinity of the weakened plane (see figure 1(C)), thereby transferring the seed layer from the donor substrate to the carrier substrate (figure 1(D)). Figures 1(B)-1(D) show the transfer of the first seed layer 21 onto the front face of the carrier substrate 1. It is understood that identical steps are implemented in order to transfer the second seed layer 22 onto the rear face of the carrier substrate 1.

The bonding can be carried out in accordance with the techniques disclosed in patents FR 3117666 B1 and FR 3112240 B1. It is also possible to carry out direct Surface Activated Bonding (SAB) or bonding using a conductive or semi-conductive bonding layer (for example, Si or W).

Optionally, after the seed layers 21 and 22 have been transferred, "finishing" annealing can be provided in order to reinforce the bonding and/or to reactivate the dopants in the seed layers 21 and 22 (since ion species implantation is likely to damage the crystalline lattice of these layers and therefore reduce the level of active dopants).

In one possible embodiment, the successive transfer of seed layers 21 and 22 is preceded by the successive implementation of surface preparation and transfer methods on both faces of the carrier substrate 1. To this end, two approaches can be considered.

The first approach involves preparing, by transferring the seed layer 21 of an intermediate substrate combining the carrier substrate 1 and the seed layer 21, followed, after depositing a protective layer onto the surface of the seed layer 21, by a second sequence of transferring the seed layer 22. Optionally, a drift layer 31 (described hereafter) is deposited onto the seed layer 21 before transferring the seed layer 22, in which case it is the surface of the drift layer 31 that is covered with a protective layer before and during the transfer of the seed layer 22.

This first approach amounts to successively linking two sequences of the Smart Cut™ method, addressing one face of the carrier substrate 1 each time. It has the advantage of re-using the existing prior art. It also allows a new sequence to be implemented of preparing the surface of the carrier substrate 1 before transferring the seed layer 22, with it being understood that the rear face of a carrier substrate is impacted, during the operations associated with the Smart Cut™ method and with the growth of the drift layer

31, by: roughening under the effect of the heat treatments, creation of scratches during handling operations and installing/removing on equipment of the chuck type, the addition of particles related to each manufacturing step. This new sequence of preparing the carrier substrate 1 before transferring the seed layer 22 can also include a step of thinning the carrier substrate 1 if necessary.

Protecting the surface of the drift layer 31 before initiating surface preparation and transferring the seed layer 22 can involve, for example, depositing a layer (or “capping”) of carbon.

The second approach involves combined preparation by successively bonding the donor substrates of the seed layers 21 and 22, before applying a single debonding annealing process, resulting in the separation of three substrates, one forming the negative that provided the seed layer 21 (in other words, the portion of the donor substrate remaining after transferring the seed layer 21), the second being the substrate formed by the seed layer 21, the carrier substrate 1 and the seed layer 22, the third forming the negative that provided the layer 22 (in other words, the portion of the donor substrate remaining after transferring the seed layer 22).

This second approach limits the thermal budget required to produce and finish the substrates illustrated in figure 3, since the debonding and/or finishing annealing processes do not need to be repeated.

However, this second approach has two disadvantages. Firstly, it requires successively handling the substrates with their rear face. It therefore can be advisable to apply/remove protective layers (for example, by depositing a carbon resin, potentially annealed) onto the rear face to be handled, before applying a treatment (for example, polishing or epitaxy) on the opposite face of the substrate. Secondly, without a protective layer, this second approach requires successively impacting each surface when treating an opposite face. This disadvantage, which is particularly noticeable during the growth or heat treatment steps, can be limited by carefully aligning the substrates during each step, impacting as few chips as possible.

With reference to figure 3, the method can continue with the growth, on each of the first and second seed layers 21, 22 transferred onto the front face and the rear face of the

carrier substrate, respectively, of a drift layer 31, 32 made of a wide bandgap semiconductor material (which may or may not be identical to that of the underlying seed layers). This thus can involve monocrystalline drift layers, for example, SiC layers deposited onto SiC seed layers, or even GaN layers deposited onto GaN or SiC seed layers.

5 Each of the drift layers 31, 32 can be grown by epitaxy, for example, by chemical vapour deposition (CVD).

The thickness of the drift layer 31, 32 deposited onto each of the first and second seed layers 21, 22 can range between 5 and 100 μm depending on the desired blocking voltage.

10 The drift layer 31, 32 deposited onto each of the first and second seed layers 21, 22 is preferably doped, for example, n-type doped, notably so as to lower its resistivity. In the case of an SiC drift layer, this can have a doping level ranging between 10^{13} and 10^{17} atoms/ cm^3 .

15 In a preferred application, the carrier substrate 1 is made of a material with lower resistivity than that of the material of the drift layers, preferably resistivity of less than 20 $\text{m}\Omega\cdot\text{cm}$. Using the example of a polycrystalline SiC carrier substrate, this exhibits resistivity ranging between 1 and 10 $\text{m}\Omega\cdot\text{cm}$. Such low resistivity is so low that the two drift layers 31, 32 can be considered to be connected by a conducting wire. As a result, the equivalent electrical thickness of the carrier substrate is divided up to 20 times. Considering an optimal
20 configuration for a polycrystalline SiC carrier substrate (carrier substrate thickness of 100 μm and resistivity of 1 $\text{m}\Omega\cdot\text{cm}$), a differential on-state resistance as low as 0.01 $\text{m}\Omega\cdot\text{cm}^2$ is found, equivalent to that of a 5 μm thick monocrystalline SiC substrate and significantly lower than that (140 $\text{m}\Omega\cdot\text{cm}^2$) found in article [2] with a shared drift region in the form of a 250 μm thick monocrystalline SiC substrate.

25 The method can continue by producing all or some of the electronic components on each side of the substrate, i.e., in each of the drift regions 31, 32, notably by means of double-sided lithography steps. In particular, the method can include carrying out steps conventionally implemented in the field in order to form an MOS transistor from each of the drift layers 31, 32.

The method thus can include implanting N-type or P-type impurities in the drift layer 31, 32 deposited onto each of the first and second seed layers. In the embodiment shown in figure 4, this implantation allows P-doped wells 33 to be formed and allows N+ doped bands 34 and P+ doped bands 35 to be formed within them. The implantation also allows a region to be formed that forms a Junction Field Effect Transistor (JFET) channel 36 or a charge storage layer (CSEL).

The method can also include depositing a gate oxide layer 37 onto the drift layer 31, 32 deposited onto each of the first and second seed layers and forming a gate electrode 28 on the gate oxide layer 37.

The invention is not limited to the method described above but also extends to the substrate thus manufactured (at any stage of the manufacturing process) and to a bi-directional switch made from such a substrate, for example, in a common source or common drain configuration.

References

[1] J. Huber and J. W. Kolar, "Monolithic Bidirectional Power Transistors", in *IEEE Power Electronics Magazine*, Vol. 10, No. 1, pp. 28-38, March 2023, doi: 10.1109/MPEL.2023.3234747.

[2] S. Chowdhury, C. Hitchcock, Z. Stum, R. P. Dahal, I. B. Bhat and T. P. Chow, "Experimental Demonstration of High-Voltage 4H-SiC Bi-Directional IGBTs", in *IEEE Electron Device Letters*, Vol. 37, No. 8, pp. 1033-1036, Aug. 2016, doi: 10.1109/LED.2016.2581419

CLAIMS

1. Method for manufacturing a substrate for producing a bi-directional switch with transistors connected vertically back-to-back, comprising:

- providing a carrier substrate (1) having a front face and a rear face;
- 5 - transferring a first seed layer (21) made of a wide bandgap polar semiconductor material onto the front face of the carrier substrate, said first seed layer having a first type of surface (F1) and a second type of surface (F2);
- transferring a second seed layer (22) made of said wide bandgap polar semiconductor material onto the rear face of the carrier substrate, said second
- 10 monocrystalline layer having a first type of surface (F1) and a second type of surface (F2);

said transfers being carried out so as to expose the first type of surface (F1) of the first seed layer (21) and the first type of surface (F1) of the second seed layer (22), with the second type of surface (F2) of the first seed layer (21) and the second type of surface (F2) of the

15 second seed layer (22) being at the interface with the front face and the rear face of the carrier substrate, respectively.

2. Method according to Claim 1, wherein transferring each of the first and second seed layers (21, 22) onto the front face and the rear face of the carrier substrate,

20 respectively, comprises:

- bonding a second type of surface of a donor substrate (2) made of said wide bandgap polar semiconductor material onto the front face and the rear face of the carrier substrate (1), respectively, with the donor substrate having been previously implanted with ion species through its second type of surface in order to form a
- 25 weakened plane (3) therein:
- delivering thermal and/or mechanical energy in order to separate the donor substrate in the vicinity of the weakened plane.

3. Method according to any of Claims 1 and 2, further comprising growing, on each

30 of the first and second seed layers (21, 22) transferred onto the front face and the rear face

of the carrier substrate, respectively, a drift layer (31; 32) made of a wide bandgap semiconductor material.

4. Method according to Claim 3, wherein the thickness of the drift layer (31, 32) deposited onto each of the first and second seed layers (21, 22) ranges between 5 and 100 μm .

5. Method according to any of Claims 3 and 4, wherein the drift layer (31, 32) deposited onto each of the first and second seed layers (21, 22) is doped.

6. Method according to any of Claims 3 to 5, further comprising implanting N-type or P-type impurities in the drift layer (31, 32) deposited onto each of the first and second seed layers.

7. Method according to Claim 6, further comprising depositing a gate oxide layer (37) onto the drift layer (31, 32) deposited onto each of the first and second seed layers and forming a gate electrode (38) on the gate oxide layer.

8. Method according to any of Claims 3 to 7, wherein the carrier substrate (1) is made of a material with electrical resistivity of less than 20 $\text{m}\Omega\cdot\text{cm}$.

9. Method according to any of Claims 1 to 8, wherein the carrier substrate (1) is a substrate of silicon carbide, aluminium nitride, diamond or gallium oxide.

10. Method according to any of Claims 1 to 9, wherein the thickness of the carrier substrate (1) ranges between 100 μm and 500 μm , and preferably ranges between 300 and 400 μm .

11. Method according to any of Claims 1 to 10, wherein the thickness of each of the first and second seed layers (21, 22) is less than or equal to 10 μm .

12. Method according to any of Claims 1 to 11, wherein the first type (F1) and the second type (F2) of surfaces of each one from among the first seed layer (21) and the

second seed layer (22) are perpendicular faces, to within 15°, in opposite crystalline directions.

13. Method according to Claim 12, wherein each one from among the first and the second seed layers (21, 22) is a layer of SiC whose first type of surface (F1) is an Si-type surface.

14. Method according to Claim 12, wherein each one from among the first and the second seed layers (21, 22) is a layer of GaN whose first type of surface (F1) is a Ga-type surface.

15. Substrate for producing a bi-directional switch with transistors connected vertically back-to-back, comprising:

- a carrier substrate (1) having a front face and a rear face;
- a first seed layer (21) transferred onto the front face of the carrier substrate, with the first seed layer being made of a wide bandgap polar semiconductor material and having a first type of surface (F1) and a second type of surface (F2), with the second type of surface (F2) of the first seed layer being at the interface with the front face of the carrier substrate;
- a second seed layer (22) transferred onto the rear face of the carrier substrate, with the second seed layer being made of a wide bandgap polar semiconductor material and having a first type of surface (F1) and a second type of surface (F2), with the second type of surface (F2) of the second seed layer being at the interface with the rear face of the carrier substrate.

16. Bi-directional switch with transistors connected vertically back-to-back, integrating a substrate according to Claim 15.