

PRECODERS FOR PARTIAL RESPONSE CHANNELS

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates generally to methods and apparatuses used either for storing data on magnetic storage media, or for communication through channels, when equalization at the receiver side is performed according to a partial response target. More particularly, it relates to PR channels with concatenated coding for error detection and correction.

Description of the Related Art

10 As can be noted from R. Karabed, P. Siegel, E. Soljanin, "Constrained Coding for Binary Channels with High Intersymbol Interference," IEEE Transaction on Information Theory, vol. IT-45, No. 6, Sept. 1999, pp 1777-1797, imposing certain constraints on modulation codes for partial response (PR) channels increases the minimum free Euclidean distance of the decoding trellis, which consequently improves the Bit-Error-Rate (BER)
15 characteristics. However, this improvement is achieved at the cost of increased complexity in encoding/decoding circuits. For example, the Maximum-Transition-Run (MTR) code constraint increases the minimum squared Euclidean distance from 6 to 10 in an *EPR4* channel, producing about 2.2 dB in coding gain. The gain can be further improved (by up to 3.5 dB) by using a modified target and the 16/17 quasi-MTR code.
20 The 16/17 quasi-MTR code allows three (but not four) consecutive transitions, and thus results in 65,546 code words of length 17 that meet the code constraint. Since 65,536

different 16-bit input patterns are to be encoded out of the available 17-bit patterns for this code, the complexity of the encoder/decoder circuits is relatively large.

As a general rule, using nontrivial distance enhancing constraints leads to relatively complicated decoding trellises, and as a consequence, to "bulky" time variant decoding circuits. U.S. Patent No. 5,497,384 discusses a read/write channel with a time variant decoding trellis. Such a decoding method employs a detector trellis structure, which consists of connected trellises with periodically repeated patterns of nodes and subtrellises, that is, it is a periodic permutation of states. The ending states of one subtrellis must mate with the beginning states of an adjacent subtrellis to generate a detector trellis structure for arbitrarily long sequences. Therefore, the survivor metric and survivor sequence for an ending of a subtrellis will be assigned to the beginning state of the subsequent subtrellis with which it is mated. The mating of the ending states and beginning states ensures that the resulting trellis will contain no distance 2 events, and it is therefore used to increase minimum distance properties and reduce error event length.

Alternative solutions are based on a coded modulation technique using so-called Structured Set Partitions (SSP) of the PR channel. See A. Kuznetsov and M. Umemoto, "Structured Set Partitions and Multilevel Concatenated Coding for Partial Response Channels", IEEE Transactions on Communications, vol. COM-47, No. 6, June 1999, pp. 856-861. The first proposed scheme of this type combines the List Trellis Detector (LTD), which can be considered as a modified Viterbi Algorithm (VA) that searches for the two best paths in the trellis, and an efficient concatenated coding scheme that uses conventional block codes with different error correction capabilities. The structure is quite flexible and can be applied to different types of PR channels, to set different code lengths and error correction capabilities, and to use well-known algebraic and probabilistic decoders for component codes. This significantly improves the overall signal-to-noise ratio (SNR) performance of the read channel compared to the uncoded PR solutions. For

the *EPR4* channel using the Lorentzian model with user densities of 2.5 and 3.0, the expected SNR gain is between 1.9 and 2.0 dB compared to the uncoded *EPR4* channel, and between 2.7 and 2.8 dB compared to the rate 16/17 ($d=0$, 6/6) coded *EPR4* channel.

U.S. Patent No. 5,881,071 discusses one read/write channel of this type that may consist of the following three steps: 1) An incoming data sequence is de-multiplexed into two or more subsequences. 2) Each of these subsequences is encoded using a conventional encoder designed for error detection or correction purposes. 3) Finally, the parallel sub-strings in the output of the encoders are converted into the channel media code according to the unique SSP table that partitions output words of the *EPR4* channel into special subsets. These subsets are characterized by the spectrum of squared minimal Euclidean distances $\{d_0^2 = 4, d_1^2 = 8, d_2^2 = 16\}$. The SSP table is a key element in the approach in U.S. Patent 5,881,071, since in the *EPR4* channel the minimal squared Euclidean distance d^2 of the 3-level concatenated code satisfies

$$d^2 \geq \min\{d_0^2 D_0, d_1^2 D_1, d_2^2 D_2\},$$
 where D_0 , D_1 , and D_2 are the minimum Hamming distances of the conventional codes used at stage 2 of the encoding process. For example, if $D_0 = 8$ (as in the extended binary Golay code), $D_1 = 4$ (as in the Hamming code), and $D_2 = 2$ (as in the trivial parity check), then $d^2 \geq 32$. The drawback of this SSP based approach is the lack of SSP tables for different types of PR channels, and the complexity of the precoders using Read Only Memory (ROM) to store the SSP table. U.S Patent 5,881,071 teaches the provision of only one SSP table for an *EPR4* channel.

The Soft-Output Viterbi Algorithm (SOVA) is another modified VA that gives the most likely path sequence in the trellis as well as the *a posteriori* probability for each transmitted bit. Similar *a posteriori* probabilities (soft outputs) are also given by the BCJR algorithm. Since the SOVA and BCJR operate on a trellis, they can be used for a PR channel. These algorithms can also be combined with a soft decoding scheme for block or

convolutional modulation codes. A problem with the above mentioned decoding schemes is that, although the BER of such schemes approaches record high levels, the complexity of the decoding schemes implementation and the time delays involved, raise serious problems and have drawbacks.

Summary of Invention

The problems and drawbacks of the above mentioned techniques are overcome by utilizing simple, efficient SSP precoders, along with exemplary embodiments of the present invention so that the complexity and time delay of a decoder scheme is minimized or reduced for many types of PR channels. The main task of an exemplary embodiment of this invention is to produce precoders and their corresponding logic schemes, together with a method of using these precoders and their schemes, to generate a media code sequence of symbols for data storage channels, with partial response equalization and a multilevel encoding/modulation scheme. Partial responses are defined by the classical and modified target polynomials, while multilevel encoding/modulation schemes include 1) Structured Set Partitions (SSP), 2) a set of conventional block codes with different error correcting capabilities, and 3) a variety of iterative decoding methods such as the List Trellis Decoder (LTD), the BCJR algorithm, and soft decoding of low-density parity check codes. Precoders are derived from the SSP's, and combined with ECC encoders that are designed for error detection, or error correction, or both. A cascade of parallel ECC encoders followed by an SSP precoder, increases the minimum Euclidean distance between different media code sequences of symbols, and as a result gives lower bit error rates after decoding.

Brief Description of the Drawings

The present invention may be better understood by consulting the following Detailed Description in conjunction with the accompanying Drawings wherein:

FIGURE 1 is a block diagram of a read/write channel.

FIGURE 2 is a diagram showing the general structure of an outer code matrix.

FIGURE 3 shows a 3-level concatenated encoder combined with an SSP-precoder.

FIGURE 4 shows an example of an outer code matrix using 2 block codes for burst error correction and a parity check code.

FIGURE 5 shows an SSP precoder and an encoder generating the outer code matrix shown in FIGURE 4.

FIGURE 6 shows an example of an outer code matrix using block code with a low density parity check matrix (LDPC code) in the first two rows.

FIGURE 7 shows an SSP precoder and an encoder generating the outer code matrix shown in FIGURE 6.

FIGURE 8 shows an example of an outer code matrix using LDPC code in the first row.

FIGURE 9 shows an SSP precoder and an encoder generating the outer code matrix shown in FIGURE 8.

FIGURE 10 is the SSP precoder which maps the given stage $s = (s_2, s_1)$ and three new code bits a , b , and c to the next state $s = (s_0, s_1, s_2)$ for the *EPR4* channel with the target $[1, 1, -1, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 8, d_2^2 = 16\}.$$

FIGURE 11 is the SSP precoder which maps the given state $s = (s_2, s_1)$ and three new code bits a , b , and c to the next state $s = (s_0, s_1, s_2)$ for the *EPR4* channel with the target $[1, 1, -1, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 4, d_2^2 = 16, d_3^2 = 8\}.$$

FIGURE 12 is the SSP precoder which maps the given state $s = (s_{-2}, s_{-1})$ and three new code bits a , b , and c to the next state $s = (s_0, s_1, s_2)$ for the *EPR4* channel with the target $[1, 1, -1, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 4, d_2^2 = 16, d_3^2 = 8\}.$$

FIGURE 13 is the SSP precoder which maps the given state $s = (s_{-3}, s_{-2}, s_{-1})$ and three new code bits a , b , and c to the next state $s = (s_0, s_1, s_2)$ for the *EPR4* channel with the target $[1, 2, -2, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 12, d_2^2 = 24\}.$$

FIGURE 14 is the SSP precoder which maps the given state $s = (s_{-1})$ and three new code bits a , b , and c to the next state $s = (s_0, s_1, s_2)$ for the *MEPR4* channel with the target $[1, 2, -2, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 16, d_2^2 = 16\}.$$

FIGURE 15 is the SSP precoder which maps the given state $s = (s_{-2}, s_{-1})$ and three new code bits a , b , and c to the next state $s = (s_0, s_1, s_2)$ for the *MEPR4* channel with the target $[2, 3, -3, -2]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 12, d_1^2 = 36, d_2^2 = 64\}.$$

FIGURE 16 is the SSP precoder which maps the given state $s = (s_{-3}, s_{-2})$ and three new code bits a , b , and c to the state extension $s = (s_0, s_1, s_2)$ for the *E²PR4* channel with the target $[1, 2, 0, -2, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 8, d_2^2 = 16\}.$$

FIGURE 17 is the SSP precoder which maps the given state $s = (s_{-2}, s_{-1})$ and three new code bits a , b , and c to the state extension $s = (s_0, s_1, s_2)$ for the ME^2PR4 channel with the target $[1, 3, 0, -3, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 16, d_2^2 = 44\}$$

FIGURE 18 is the SSP precoder which maps the given state $s = (s_{-2}, s_{-1})$ and three new code bits a , b , and c to the state extension $s = (s_0, s_1, s_2)$ for the ME^2PR4 channel with the target $[1, 3, 0, -3, -1]$. It gives the spectrum of minimal Euclidean distances

$$\{d_0^2 = 4, d_1^2 = 20, d_2^2 = 24\}.$$

FIGURE 19 is the SSP precoder which maps the given state $s = (s_{-4}, s_{-2}, s_{-1})$ and three new code bits a , b , and c to the state extension $s = (s_0, s_1, s_2)$ for the ME^2PR4 channel with the target $[5, 4, -3, -4, -2]$. It gives the spectrum of minimal Euclidean distances $\{d_0^2 = 16, d_1^2 = 36, d_2^2 = 116\}$.

Detailed Description of the Preferred Exemplary Embodiments

To aid the understanding of the exemplary embodiments of the present invention, the unpublished document, A.V. Kuznetsov, "Coded Modulation Schemes with Turbo and List Detection For Higher-Order PR Channels", is hereby incorporated by reference and attached hereto. Referring now to the drawings, and in particular to FIGURE 1, there is shown the structure of a read/write channel 100 with an L-level concatenated encoder 102 followed by an SSP precoder 104, and the functions of its main blocks. Encoding part of the channel 100 consists of a set of algebraic encoders 102 and a precoder 104. The combination of the encoder 102 and precoder 104 provide an encoder/precoder complex 106. Algebraic encoders generate an *outer code matrix* U of size $L \times n$, $L \leq l$, such that its i -th row is a code word of the code C_i with alphabet size $q_i = 2^{l(i)}$, and minimum Hamming

distance, D_i , $i = 0, 1, \dots, L-1$. In the general case, the parameters $l(i)$ are arbitrary positive integers, such that $l(0) + l(1) + \dots + l(L-1) = l$, but in our examples below $l = L = 3$, i.e., $l(0) = l(1) = l(2) = 1$. Coded modulation schemes are usually set up so that $D_0 > D_1 > \dots > D_{L-1}$. The general structure of an outer code matrix 200 for $L = 3$, is shown in FIGURE 2.

An outer code matrix, U , is generated by a set of parallel conventional ECC encoders 302, as shown in FIGURE 3 in the encoder/precoder complex 300 for the case when each row of an outer code matrix U is generated by its own encoder.

The columns $\mathbf{u}_0, \mathbf{u}_1, \dots, \mathbf{u}_{n-1}$ of an outer code matrix U are sequentially sent to a precoder 104. At the time instant j , for $j = 0, 1, \dots, n-1$, using $\mathbf{u}_j$ and the current state of the channel, $\mathbf{s}^- = (s_{i-m}, \dots, s_{i-2}, s_{i-1})$, the precoder generates a state sequence extension, $\mathbf{s} = \varphi(\mathbf{s}^-, \mathbf{u}_j)$, of length l , and sends it to its output 304. At the same time, it also updates its internal register containing $\mathbf{s}^-$ 306: If $l = m$, then $\mathbf{s}^-$ is simply replaced by $\mathbf{s}$. If $l < m$, then the new state $\mathbf{s}^-$ is a concatenation of the last $m - l$ bits of $\mathbf{s}^-$ and $\mathbf{s}$. If $l > m$, then the new state $\mathbf{s}^-$ 306 consists of the last m bits of $\mathbf{s}$.

An input of the PR channel is a bipolar sequence $(\dots, x_{i-1}, x_i, x_{i+1}, x_{i+2}, \dots)$ with components $x_i = 2s_i - 1 = \pm 1$, where $s_i = 0, 1$ is a binary output of the precoder. Given a target $\mathbf{f} = [f_0, f_1, \dots, f_m]$ with integer (real or complex in general case) components, an output symbol y_i of the PR channel at the time instant i is defined by the equality

$$y_i = (f_m x_{i-m} + \dots + f_2 x_{i-2} + f_1 x_{i-1}) + f_0 x_i \quad (1)$$

The bipolar word $\mathbf{x}^- = (x_{i-m}, \dots, x_{i-2}, x_{i-1})$ and its binary version $\mathbf{s}^- = (s_{i-m}, \dots, s_{i-2}, s_{i-1})$ are both called *states* of the channel at the time instant i . The current state $\mathbf{s}^-$ 306 and a sequence of subsequent state bits $\mathbf{s} = (s_i, s_{i+1}, s_{i+2}, \dots)$ define an output word 304 of the PR channel, $\mathbf{y} = (y_i, y_{i+1}, y_{i+2}, \dots)$, by application of (1), component-by-component. Therefore, the word $\mathbf{y}$ is a function $f(\mathbf{s}^- \circ \mathbf{s})$ of the concatenation $\mathbf{s}^- \circ \mathbf{s} = (s_{i-m}, \dots, s_{i-2}, s_{i-1}, s_i, s_{i+1}, s_{i+2}, \dots)$

of $\mathbf{s}^-$ and $\mathbf{s}$. This function is time invariant, and the length of $\mathbf{y}$ is equal to the length of $\mathbf{s}$. In matrix notation, we have $\mathbf{y} = f(\mathbf{s}^- \circ \mathbf{s}) = \mathbf{x}^* F$, where the matrix

$$F = \begin{pmatrix} f_m & 0 & \dots & 0 \\ f_{m-1} & f_m & \dots & 0 \\ \dots & \dots & \dots & \dots \\ f_0 & f_1 & \dots & f_m \\ 0 & f_0 & \dots & f_{m-1} \\ \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & f_0 \end{pmatrix} \quad (2)$$

has size $(m+1) \times l$, and $\mathbf{x}$ is the bipolar representation of the compound state $\mathbf{s}^- \circ \mathbf{s}$.

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The method of Structured Set Partitions (SSP) has proved to be a useful tool in constructing precoder functions $\varphi(\mathbf{s}^-, \mathbf{u}_j)$ with good spectra of minimal squared Euclidean distances $\{d_0^2, d_1^2, \dots, d_{L-1}^2\}$.

An output L -level concatenated modulation code C of length $N = nl$ is the set of all sequences $F(\mathbf{s}_0, U) = (f(\mathbf{s}_0 \circ \varphi(\mathbf{s}_0, \mathbf{u}_0)) \circ f(\mathbf{s}_1 \circ \varphi(\mathbf{s}_1, \mathbf{u}_1)) \circ \dots \circ f(\mathbf{s}_{n-1} \circ \varphi(\mathbf{s}_{n-1}, \mathbf{u}_{n-1})))$, where $\mathbf{s}_0$ is the initial state of the channel, and $\mathbf{s}_j$ is the next state after $\mathbf{s}_{j-1}$, for $j = 1, 2, \dots, n$. The rate R of the code C is equal to $(l(0)k_0 + l(1)k_1 + \dots + l(L-1)k_{L-1})/N$, where k_i is the number of q_i -ary information symbols of the code C_i , $i = 0, 1, \dots, L-1$.

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If the SSP has a spectrum of minimal squared Euclidean distances

$\{d_0^2 < d_1^2 < \dots < d_{L-1}^2\}$, then the minimal squared Euclidean distance $d^2(C)$ of the L -level

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concatenated code C satisfies the inequality:

$$d^2(C) \geq \min\{d_0^2 D_0, d_1^2 D_1, \dots, d_{L-1}^2 D_{L-1}\} \quad (3)$$

where D_i is the minimum Hamming distance of C_i , $i = 0, 1, \dots, L-1$.

Although the lower bound in (3) is based only on the minimum distances, the detection scheme and its error statistic usually require component codes that correct or at least detect some specific types of errors. In particular, simulations of an exemplary embodiment of the present invention with List Trellis Decoding (LTD), have shown that for a given BER, higher user densities can be achieved using burst error correcting codes C_i instead of block codes, to correct the same number of independent bit errors.

FIGURE 4 is an example of an outer code matrix 400 with 3 rows and 256 columns. Its first two rows are code words of two different cyclic codes, correcting single bursts of errors of length 5 and 3, and having 14 and 10 redundant bits, respectively. The last row consists of 254 data bits and a single parity bit in the last position. The code rate equals $740/765 \approx .967$. The corresponding encoder/precoder complex 500 is shown as a cascade of encoders 502 and precoder 504 in FIGURE 5.

FIGURE 6 depicts an outer code matrix 600 with 3 rows of length 620, the first two of which contain a code word of the so called LDPC code, with a low density parity check matrix of size 120×1240 . This code has 3 orthogonal parity check equations for each of 1240 code bits, and is suitable for "turbo" type coding algorithms. The third row of this outer code matrix consists of uncoded data bits. The code rate equals $1742/1860 \approx$

.936. The corresponding encoder/precoder complex 700 is shown as a cascade of an encoder 702 and a precoder 704 in FIGURE 7.

FIGURE 8 shows an outer code matrix 800 with 3 rows of length 1240. The first row is a code word of the above mentioned LDPC code, and the last two rows are filled by uncoded data bits. The code rate equals $3602/3720 \approx .968$. The corresponding encoder/precoder complex 900 is shown as a cascade of an encoder 902 and a precoder 904 in FIGURE 9.

FIGURES 10 through 19 depict a number of different precoder functions, and the corresponding logic schemes for their implementation.

Although the foregoing description of concatenated encoding followed by SSP precoding is of prime importance here, other types of conventional ECC codes and parameter values, such as code lengths and minimum Hamming distances, can be applied to the system in accordance with the teachings of the invention.

The previous description is of a preferred embodiment for implementing the invention, and the scope of the invention should not necessarily be limited by this description. The scope of the present invention is instead defined by the following claims.

What is claimed is:

1. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:
 - an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and
 - a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals, wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's previous output bits (s_{-2} and s_{-1}) and 3 code data bits (a , b and c), into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = (\bar{a} \& s_{-2}) \oplus c$, $s_1 = (a \& s_{-2}) \oplus s_{-1} \oplus b \oplus c$, and $s_2 = s_{-2} \oplus a$, where $\oplus$ is the exclusive OR operator.

2. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:
 - an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and
 - a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,
 wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's previous output bits (s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = (\overline{a \oplus b} \& s_{-2}) \oplus c$, $s_1 = ((a \oplus b) \& s_{-2}) \oplus s_{-1} \oplus c \oplus b$, and $s_2 = a \oplus b \oplus s_{-2}$.

3. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:
 - an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and

a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,

wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's

previous output bits (s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = (\overline{a \oplus b} \& s_{-2}) \oplus b \oplus c$,

$s_1 = ((a \oplus b) \& s_{-2}) \oplus s_{-1} \oplus c$, and $s_2 = s_{-2} \oplus a \oplus b$.

4. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:

an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and

a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,

wherein said series of multi-bit-length sequences are composed of 6-bit-length sequences and wherein said precoder encodes said 6-bit-length sequences comprising 3 said precoder's previous output bits (s_{-3} , s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits

(s_0 , s_1 and s_2) which are generated according to $s_0 = (s_{-2} \& a) \oplus (s_{-1} \& \bar{a}) \oplus c$,

$s_1 = (s_{-2} \& \bar{a}) \oplus (s_{-1} \& a) \oplus b \oplus c$, and $s_2 = s_{-3} \oplus a$.

5. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:

an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and

a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,

wherein said series of multi-bit-length sequences are composed of 4-bit-length sequences and wherein said precoder encodes said 4-bit-length sequences comprising 1 said precoder's

previous output bit s_{-1} and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2)

which are generated according to $s_0 = (s_{-1} \& \bar{a}) \oplus c$, $s_1 = s_{-1} \oplus b$, and $s_2 = s_{-1} \oplus a$.

6. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:
 - an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and
 - a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,
 wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's previous output bits (s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = (s_{-2} \& \bar{a}) \oplus c$, $s_1 = (s_{-2} \& a) \oplus s_{-1} \oplus b \oplus c$, and $s_2 = s_{-2} \oplus a$.

7. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:
 - an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and
 - a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,
 wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's previous output bits (s_{-3} and s_{-2}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = (s_{-3} \& a \& \bar{b}) \oplus s_{-2} \oplus c$, $s_1 = s_{-3} \oplus b$, and $s_2 = s_{-2} \oplus a \oplus b$.

8. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:
 - an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and
 - a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,

wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's previous output bits (s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = s_{-2} \oplus c$, $s_1 = (s_{-2} \& a) \oplus s_{-1} \oplus b \oplus c$, and $s_2 = s_{-2} \oplus a$.

9. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:

an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and

a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,

wherein said series of multi-bit-length sequences are composed of 5-bit-length sequences and wherein said precoder encodes said 5-bit-length sequences comprising 2 said precoder's previous output bits (s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = s_{-2} \oplus b \oplus c$, $s_1 = s_{-1} \oplus b$, and $s_2 = s_{-2} \oplus a \oplus c$.

10. A partial response channel utilizing concatenated coding for error detection and correction, said partial response channel comprising:

an encoder for error checking and correcting, said encoder receiving a stream of data and producing an outer code matrix; and

a precoder for receiving said outer code matrix and for encoding a series of multi-bit-length sequences of digital electrical signals,

wherein said series of multi-bit-length sequences are composed of 6-bit-length sequences and wherein said precoder encodes said 6-bit-length sequences comprising 3 said precoder's previous output bits (s_{-4} , s_{-2} and s_{-1}) and 3 coded data bits (a , b and c) into 3 output media bits (s_0 , s_1 and s_2) which are generated according to $s_0 = c \oplus s_{-4} \oplus (s_{-2} \& (a \oplus b))$, $s_1 = b \oplus c \oplus s_{-1} \oplus (s_{-2} \& (a \oplus b))$, and $s_2 = a \oplus b \oplus s_{-2}$.

11. A method to generate a media code sequence of symbols for data storage channels, comprising the steps:
 - (a) de-multiplexing an input data stream into three parallel substreams;
 - (b) encoding at least one of said parallel substreams into at least one encoded parallel substream by a separate block or a convolutional encoder having at least one of error detection and/or correction capabilities; and
 - (c) converting at least one said encoded parallel substream and any remaining parallel substreams into said media code sequence of symbols via a precoder, said precoder operating according to three predetermined equations.
12. The method according to claim 11, wherein said predetermined equations are $s_0 = (\bar{a} \& s_{-2}) \oplus c$, $s_1 = (a \& s_{-2}) \oplus s_{-1} \oplus b \oplus c$, and $s_2 = s_{-2} \oplus a$.
13. The method according to claim 11, wherein said predetermined equations are $s_0 = (\overline{a \oplus b} \& s_{-2}) \oplus c$, $s_1 = ((a \oplus b) \& s_{-2}) \oplus s_{-1} \oplus c \oplus b$, and $s_2 = a \oplus b \oplus s_{-2}$.
14. The method according to claim 11, wherein said predetermined equations are $s_0 = (\overline{a \oplus b} \& s_{-2}) \oplus b \oplus c$, $s_1 = ((a \oplus b) \& s_{-2}) \oplus s_{-1} \oplus c$, and $s_2 = s_{-2} \oplus a \oplus b$.
15. The method according to claim 11, wherein said predetermined equations are $s_0 = (s_{-2} \& a) \oplus (s_{-1} \& \bar{a}) \oplus c$, $s_1 = (s_{-2} \& \bar{a}) \oplus (s_{-1} \& a) \oplus b \oplus c$, and $s_2 = s_{-3} \oplus a$.
16. The method according to claim 11, wherein said predetermined equations are $s_0 = (s_{-1} \& \bar{a}) \oplus c$, $s_1 = s_{-1} \oplus b$, and $s_2 = s_{-1} \oplus a$.
17. The method according to claim 11, wherein said predetermined equations are $s_0 = (s_{-2} \& \bar{a}) \oplus c$, $s_1 = (s_{-2} \& a) \oplus s_{-1} \oplus b \oplus c$, and $s_2 = s_{-2} \oplus a$.
18. The method according to claim 11, wherein said predetermined equations are $s_0 = (s_{-3} \& a \& \bar{b}) \oplus s_{-2} \oplus c$, $s_1 = s_{-3} \oplus b$, and $s_2 = s_{-2} \oplus a \oplus b$.

19. The method according to claim 11, wherein said predetermined equations are $s_0 = s_{-2} \oplus c$, $s_1 = (s_{-2} \& a) \oplus s_{-1} \oplus b \oplus c$, and $s_2 = s_{-2} \oplus a$.
20. The method according to claim 11, wherein said predetermined equations are $s_0 = s_{-2} \oplus b \oplus c$, $s_1 = s_{-1} \oplus b$, and $s_2 = s_{-2} \oplus a \oplus c$.
21. The method according to claim 11, wherein said predetermined equations are $s_0 = c \oplus s_{-4} \oplus (s_{-2} \& (a \oplus b))$, $s_1 = b \oplus c \oplus s_{-1} \oplus (s_{-2} \& (a \oplus b))$, and $s_2 = a \oplus b \oplus s_{-2}$.