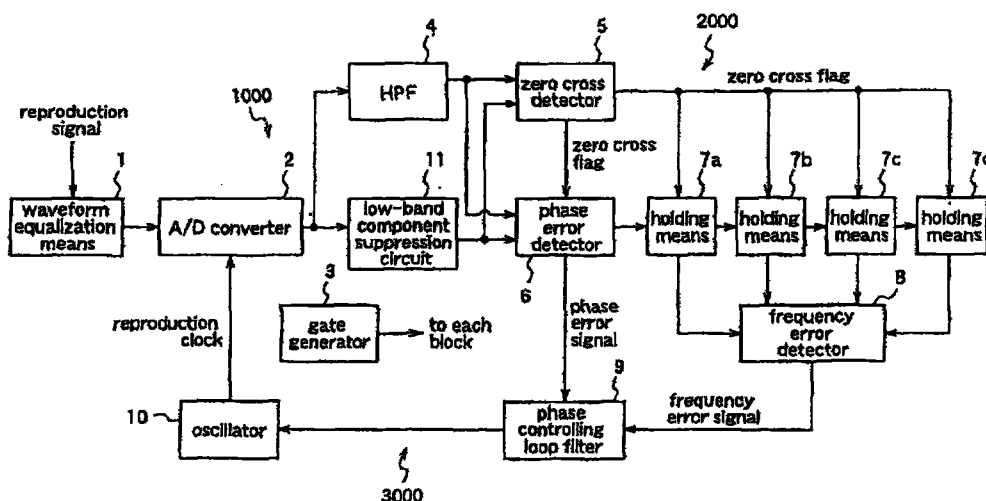




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(54) Title: PHASE-LOCKED LOOP APPARATUS



(57) Abstract

The present invention provides a phase-locked loop apparatus which extends a capture range in clock reproduction when digital data is reproduced and performs a high-speed and stable phase locking. A phase error is detected by a phase error detector (6) from a signal obtained by the sampling. Further, a frequency error is detected by a frequency error detector (8) on the basis of an inclination of a phase curve obtained by phase error information. A phase-locked loop circuit is controlled on the basis of these obtained phase error and frequency error.