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METHOD TO FORM SELF-ALIGNED/DRAIN CMOS DEVICE ON INSULATED STAIRCASE OXIDE

Abstract

A method to form elevated source / drain (S/D) over staircase shaped openings in insulating layers. A gate structure is formed over a substrate The gate structure is preferably comprised of a gate dielectric layer, gate electrode, first spacers, and hard mask A first insulating layer is formed over the substrate and the gate structure A resist layer is formed having an opening over the gate structure and over a lateral area adjacent to the gate structure We etch the insulating layer through the opening in the resist layer. The etching removes a first thickness of the insulating layer to form a source / drain (S/D) opening. We remove the first spacers and hardmask to form a source / drain (S/D) contact opening. We implant ions into the substrate through the source / drain (S/D) contact opening to form lightly doped drain regions. We form second spacers on the sidewalls of the gate electrode and the gate dielectric and on the sidewalls of the insulating layer in the source / drain (S/D) contact opening and the source / drain (S/D) opening. A conductive layer is deposited over the gate electrode, the insulating layer. The conductive layer is planarized to exposed the insulating layer to form elevated source / drain (S/D) blocks on a staircase shape insulating layer.

Figure 8

FILED ON 3/4/02