

# **VERTICAL MEMORY DEVICES AND METHODS OF MANUFACTURING THE SAME**

## **CROSS-REFERENCE TO RELATED APPLICATIONS**

**[0001]** This patent application claims priority to Korean Patent Application No. 10-2019-0092525, filed on 30 July 2019 in the Korean Intellectual Property Office (KIPO), the contents of which are herein incorporated by reference in their entirety.

## **TECHNICAL FIELD**

**[0002]** Inventive concepts relate to a vertical memory device and/or a method of manufacturing the same.

## **BACKGROUND**

**[0003]** In a VNAND flash memory device, a charge trapping layer on an outer sidewall of a vertical channel may extend in a vertical direction, and thus charges trapped in the charge trapping layer may be moved in the vertical direction by a plurality of gate electrodes at a plurality of levels, respectively. As a result, a retention characteristic of the VNAND flash memory device may deteriorate, which may cause reliability problems.

## **SUMMARY**

**[0004]** Some example embodiments provide a vertical memory device having improved characteristics.

**[0005]** Some example embodiments provide a method of manufacturing a vertical memory device having improved characteristics.

**[0006]** According to some example embodiments, there is provided a vertical memory device including a channel on a substrate, the channel extending in a vertical direction that is perpendicular to an upper surface of the substrate, a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern, and a first blocking pattern that are sequentially stacked in a horizontal direction, the horizontal direction parallel to the upper surface of the substrate, and gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure. The charge storage structure includes charge trapping patterns spaced apart from each other in the vertical direction, each of the charge trapping patterns facing one of the gate electrodes in the horizontal direction. A first length in the vertical direction of an inner sidewall of at least one of the charge trapping patterns facing the tunnel insulation pattern is less than a second length in the vertical direction of an outer sidewall of a respective at least one of the charge trapping patterns facing the first blocking pattern.

**[0007]** According to some example embodiments, there is provided a vertical memory device including a channel on a substrate, the channel extending in a vertical direction that is perpendicular to an upper surface of the substrate, a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern structure, and a blocking pattern that are sequentially stacked in a horizontal direction parallel to the upper surface of the substrate, and gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure. The charge storage structure includes charge trapping pattern structures spaced apart from each other in the vertical direction, each of the charge trapping pattern structures facing a corresponding one of the gate electrodes in the horizontal direction. Each of the charge trapping pattern structures includes first and second charge

trapping patterns that are sequentially stacked in the horizontal direction on an outer sidewall of the tunnel insulation pattern, the first and second trapping patterns including different materials from each other.

**[0008]** According to some example embodiments, there is provided a vertical memory device including a channel on a substrate, the channel extending in a vertical direction perpendicular to an upper surface of the substrate, a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern, and a blocking pattern that are sequentially stacked in a horizontal direction parallel to the upper surface of the substrate, a dummy charge storage structure spaced apart from the charge storage structure in the vertical direction on the substrate, the dummy charge storage structure including a dummy tunnel insulation pattern, a dummy charge trapping pattern, and a dummy blocking pattern that are sequentially stacked, and gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure. The charge storage structure includes charge trapping patterns spaced apart from each other in the vertical direction, each of the charge trapping patterns facing a corresponding one of the gate electrodes in the horizontal direction. The dummy tunnel insulation pattern and the dummy blocking pattern include materials substantially the same as those of the tunnel insulation pattern and the blocking pattern, respectively, and the dummy charge trapping pattern includes a material different from that of the charge trapping patterns.

**[0009]** According to some example embodiments, there is provided a vertical memory device including channels on a substrate, each of the channels extending in a first direction perpendicular to an upper surface of the substrate, a channel connection pattern on the substrate, the channel connection pattern contacting the channels, a charge storage structure on outer sidewalls of the channels on the channel connection pattern, the charge storage

structure including a tunnel insulation pattern, a charge trapping pattern, a blocking pattern and a division pattern, the tunnel insulation pattern, the charge trapping pattern, and the blocking pattern sequentially stacked in a horizontal direction parallel to the upper surface of the substrate, gate electrodes spaced apart from each other in the first direction, each of the gate electrodes surrounding the charge storage structure, division structures on the substrate, each of the division structures extending through the gate electrodes in a second direction parallel to the upper surface of the substrate, the division structures dividing each of the gate electrodes in a third direction, the third direction parallel to the upper surface of the substrate and crossing the second direction, and bit lines on the channels, each of the bit lines extending in the third direction to electrically connect to the channels. The charge storage structure includes charge trapping patterns spaced apart from each other in the first direction, each of the charge trapping patterns facing one of the gate electrodes in the horizontal direction. A first length in the first direction of an inner sidewall of each of the charge trapping patterns facing the tunnel insulation pattern is less than a second length in the first direction of an outer sidewall of each of the charge trapping patterns facing the blocking pattern. The division pattern is between ones of the charge trapping patterns that neighbor in the first direction, the division pattern contacting the tunnel insulation pattern and the blocking pattern, the division pattern including an insulating material.

**[0010]** According to some example embodiments, there is provided a method of fabricating a vertical memory device including forming a mold on a substrate, the mold including an insulation layer and a first sacrificial layer that are alternately and repeatedly stacked, forming a channel and a preliminary charge storage structure on the substrate, the channel extending through the mold, and the preliminary charge storage structure covering an outer sidewall of the channel and including a tunnel insulation pattern, a preliminary charge trapping pattern, and a first blocking pattern that are sequentially stacked, forming an

opening through the mold to expose an upper surface of the substrate, removing the first sacrificial layer through the opening to form a first gap exposing an outer sidewall of the preliminary charge storage structure, performing a first nitridation process on the preliminary charge trapping pattern through the first gap to form charge trapping patterns spaced apart from each other in a vertical direction that is perpendicular to the upper surface of the substrate, performing a first oxidation process on the preliminary charge trapping pattern through the first gap to form a division pattern between the charge trapping patterns, and forming a gate electrode in the first gap.

**[0011]** According to some example embodiments, there is provided a method of fabricating a vertical memory device including forming a mold on a substrate, the mold including an insulation layer and a sacrificial layer that are alternately and repeatedly stacked, forming a channel and a preliminary charge storage structure on the substrate, the channel extending through the mold, and the preliminary charge storage structure covering an outer sidewall of the channel and including a tunnel insulation pattern, a preliminary charge trapping pattern, and a first blocking pattern that are sequentially stacked, forming an opening through the mold to expose an upper surface of the substrate, removing the sacrificial layer through the opening to form a gap exposing an outer sidewall of the preliminary charge storage structure, performing a first nitridation process on the preliminary charge trapping pattern through the gap to form oxidation reduction patterns spaced apart from each other in a vertical direction that is perpendicular to the upper surface of the substrate, performing a first oxidation process on the preliminary charge trapping pattern through the gap to form a preliminary division pattern between the oxidation reduction patterns, performing a second oxidation process on the oxidation reduction patterns and the preliminary charge trapping pattern through the gap to divide the preliminary charge trapping pattern into a plurality of pieces spaced apart from each other in the vertical direction, performing a second nitridation

process on each of the preliminary charge trapping patterns through the gap to form a charge trapping pattern at lower and upper ends and an outer sidewall of each of the preliminary charge trapping patterns, and forming a gate electrode in the gap.

**[0012]** In the method of manufacturing the vertical memory device in accordance with some example embodiments, a nitridation process and/or an oxidation process may be performed on the preliminary charge trapping pattern extending in the vertical direction, to more easily form a plurality of charge trapping patterns spaced apart from each other in the vertical direction. Thus, charges trapped in the charge trapping patterns may not move in the vertical direction, or may move a reduced amount in the vertical direction, by gate electrodes at other levels, so that the retention characteristics may be enhanced. Accordingly, the vertical memory device including the charge trapping patterns may have enhanced reliability and/or enhanced retention characteristics.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0013]** FIGS. 1 and 2 are cross-sectional views illustrating a vertical memory device in accordance with some example embodiments.

**[0014]** FIGS. 3 to 11 are cross-sectional views illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments.

**[0015]** FIG. 12 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments, and an enlarged cross-sectional view of the region X of FIG. 1.

**[0016]** FIGS. 13 to 16 are cross-sectional views, particularly, enlarged cross-sectional views of the region X of FIG. 1 illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments.

**[0017]** FIG. 17 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments, and an enlarged cross-sectional view of the region X of FIG. 1.

**[0018]** FIGS. 18 to 22 are cross-sectional views, particularly, enlarged cross-sectional views of the region X of FIG. 1 illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments.

**[0019]** FIG. 23 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments, and an enlarged cross-sectional view of the region X of FIG. 1.

**[0020]** FIGS. 24 to 26 are cross-sectional views, particularly, enlarged cross-sectional views of the region X of FIG. 1 illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments.

**[0021]** FIG. 27 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments.

**[0022]** FIGS. 28 to 30 are cross-sectional views illustrating a vertical memory device in accordance with some example embodiments.

#### DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0023]** The above and other aspects and features of the vertical memory devices and/or the methods of manufacturing the same in accordance with some example embodiments will become readily understood from detail descriptions that follow, with reference to the accompanying drawings. Hereinafter in the specifications (not necessarily in the claims), a direction substantially perpendicular to an upper surface of a substrate may be defined as a first direction, and two directions substantially parallel to the upper surface of the substrate and crossing each other may be defined as second and third directions, respectively. In some

example embodiments, the second and third directions may be substantially perpendicular to each other.

**[0024]** FIGS. 1 and 2 are cross-sectional views illustrating a vertical memory device in accordance with some example embodiments. FIG. 2 is an enlarged cross-sectional view of a region X of FIG. 1.

**[0025]** Referring to FIGS. 1 and 2, the vertical memory device may include a channel 260, a first charge storage structure 252, and a gate electrode structure on a substrate 100. The vertical memory device may further include a dummy charge storage structure 250, a channel connection pattern 330, an insulation pattern 175, a second blocking pattern 360, a common source pattern (CSP) 390, a second spacer 380, a support layer 160, a support pattern 165, a filling pattern 270, a pad 280, first to third insulating interlayers 190, 290 and 400, a contact plug 410, and a bit line 430.

**[0026]** The substrate 100 may be or include a wafer, and may include silicon, germanium, silicon-germanium or a III-V compound such as GaP, GaAs, GaSb, etc. In some example embodiments, the substrate 100 may be or include a silicon-on-insulator (SOI) substrate or a germanium-on-insulator (GOI) substrate. For example, n-type impurities may be doped into the substrate 100.

**[0027]** The channel 260 may extend in the first direction on the substrate 100, and may have, e.g., a cup-like shape. The channel 260 may include polysilicon, e.g., undoped polysilicon.

**[0028]** In some example embodiments, the channel 260 may be formed in each of the second and third directions to form a channel array. The CSP 390 and the second spacer 380 on each of opposite sidewalls of the CSP 390 in the third direction may form a division structure, and the channels 260 surrounded by the gate electrode structure between ones of the division structures that neighbor each other in the third direction may form a channel

block. The channel array may include a plurality of channel blocks arranged in the third direction. The channels 260 included in each of the channel blocks may be connected with each other by the channel connection pattern 330.

**[0029]** The channel connection pattern 330 may extend in the second direction between neighboring ones of the division structures in the third direction to contact a lower outer sidewall of each of the channels 260, and a plurality of channel connection patterns 330 may be formed in the third direction. The channel connection pattern 330 may include, e.g., undoped polysilicon or polysilicon doped with impurities such as p-type and/or n-type impurities. An air gap 340 may be formed in the channel connection pattern 330.

**[0030]** The first charge storage structure 252 may be formed on the channel connection pattern 330 to cover an outer sidewall of a portion of the channel 260 extending through the gate electrode structure, and the dummy charge storage structure 250 may be formed between an upper surface of the substrate 100 and the channel connection pattern 330 to cover a bottom surface and an outer sidewall of a lower end of the channel 260. For example, the first charge storage structure 252 and the dummy charge storage structure 250 may be spaced apart from each other in the first direction by the channel connection pattern 330 contacting a lower sidewall of the channel 260. A lower surface of the first charge storage structure 252 and an upper surface of the dummy charge storage structure 250 may contact the channel connection pattern 330.

**[0031]** The first charge storage structure 252 may include a tunnel insulation pattern 240, a charge trapping pattern 232, and a first blocking pattern 220 that are sequentially stacked in a horizontal direction. The horizontal direction may be substantially parallel to the upper surface of the substrate 100. The tunnel insulation pattern 240, the charge trapping pattern 232, and the first blocking pattern 220 may be sequentially stacked from an outer sidewall of the channel 260. The first charge storage structure 252 may further include a division

pattern 234. Each of the tunnel insulation pattern 240 and the first blocking pattern 220 may include an oxide, e.g., silicon oxide, and the charge trapping pattern 232 may include a nitride, e.g., silicon nitride. The charge trapping pattern 232 may not include an oxide, and either or both of the tunnel insulation pattern 240 and the first blocking pattern 220 may not include a nitride.

**[0032]** The gate electrode structure may include the gate electrodes 372, 374, and 376 stacked at a plurality of levels, respectively, spaced apart from each other in the first direction, and the insulation pattern 175 may be formed between neighboring ones of the gate electrodes 372, 374, and 376. The insulation pattern 175 may include an oxide, e.g., silicon oxide. Each of the gate electrodes 372, 374 and 376 may surround the channels 260 and the first charge storage structures 252 covering the outer sidewall of the channels 260, respectively, between neighboring ones of the division structures in the third direction.

**[0033]** In some example embodiments, the gate electrode structure may include at least one first gate electrode 372, a plurality of second gate electrodes 374, or at least one third gate electrode 376 sequentially stacked in the first direction. The first gate electrode may serve as a ground selection line (GSL), each of the second gate electrodes 374 may serve as a word line, and the third gate electrode 376 may serve as a string selection line (SSL).

**[0034]** In the third direction, a plurality of gate electrode structures may be formed to be spaced apart from each other by the division structures. In some example embodiments, the gate electrode structure may form a staircase structure of which a length in the second direction may decrease from a lowermost level toward an uppermost level in the first direction.

**[0035]** Each of the first to third gate electrodes 372, 374, and 376 may include a gate conductive pattern and a gate barrier pattern covering a surface of the gate conductive pattern. The gate conductive pattern may include a low resistance metal, e.g., at least one of tungsten,

titanium, tantalum, platinum, etc., and the gate barrier pattern may include a metal nitride, e.g., at least one of titanium nitride, tantalum nitride, etc.

**[0036]** Upper and lower surfaces and a sidewall facing the first charge storage structure 252 of each of the first to third gate electrodes 372, 374, and 376 may be covered by the second blocking pattern 360, and the second blocking pattern 360 may extend in the first direction to cover a sidewall of the insulation pattern 175 between the first to third gate electrodes 372, 374 and 376. The second blocking pattern 360 may include a metal oxide, e.g., aluminum oxide.

**[0037]** In some example embodiments, each of the tunnel insulation pattern 240 and the first blocking pattern 220 included in the first charge storage structure 252 may extend in the first direction through the gate electrode structure, and a plurality of charge trapping patterns 232 may be spaced apart from each other in the first direction to face the gate electrodes 372, 374 and 376, respectively, in the horizontal direction.

**[0038]** However, a minimum length L1 in the first direction of each of the charge trapping patterns 232 may be greater than that of a third length L3 in the first direction of each of second gaps 350 for forming the gate electrodes 372, 374, and 376, respectively, between the insulation patterns 175. One of the gate electrodes 372, 374, and 376 and the second blocking pattern 360 may be formed in each of the second gaps 350, and thus the first length L1 may be greater than a fourth length L4 in the first direction of each of the gate electrodes 372, 374 and 376.

**[0039]** In some example embodiments, a length in the first direction of each of the charge trapping patterns 232 may gradually increase from the tunnel insulation pattern 240 to the first blocking pattern 220. Thus, in each of the charge trapping patterns 232, the first length L1 of an inner sidewall contacting the tunnel insulation pattern 240 may be less than a second length L2 of an outer sidewall contacting the first blocking pattern 220. In some example

embodiments, an absolute value of a slope of an upper surface or a lower surface of each of the charge trapping patterns 232 with respect to the upper surface of the substrate 100 may gradually decrease from the tunnel insulation pattern 240 to the first blocking pattern 220. The charge trapping patterns 232 may be concave, e.g. may be concave in the third direction from the tunnel insulation pattern 240 to the first blocking pattern 220.

**[0040]** The division pattern 234 may be formed between neighboring ones of the charge trapping patterns 232 in the first direction, and thus the charge trapping patterns 232 may be spaced apart from each other. The division pattern 234 may face the insulation pattern 175 in the horizontal direction, more particularly, may face a central portion in the first direction of the insulation pattern 175, e.g. with the first blocking pattern 220 therebetween. The division pattern 234 may include an oxide, e.g., silicon oxide.

**[0041]** A length in the first direction of the division pattern 234 may be less than a length in the first direction of a corresponding one of the insulation patterns 175, and may gradually decrease from the tunnel insulation pattern 240 to the first blocking pattern 220. In some example embodiments, an absolute value of a slope of an upper surface or a lower surface of each of the division pattern 234 with respect to the upper surface of the substrate 100 may gradually decrease from the tunnel insulation pattern 240 to the first blocking pattern 220. The division pattern 234 may be convex, e.g. may be convex in the third direction from the tunnel insulation pattern 240 to the first blocking pattern 220.

**[0042]** In some example embodiments, bottom surfaces of the tunnel insulation pattern 240 and the charge trapping pattern 232 of the first charge storage structure 252 may be higher than a bottom surface of the first blocking pattern 220 of the first charge storage structure 252.

**[0043]** The dummy charge storage structure 250 may include the tunnel insulation pattern 240, a dummy charge trapping pattern 230, and the first blocking pattern 220 that are

sequentially stacked from the channel 260. Hereinafter, the tunnel insulation pattern 240 and the first blocking pattern 220 of the dummy charge storage structure 250 may be referred to as a dummy tunnel insulation pattern and a dummy first blocking pattern, respectively, so as to be distinguished from those of the first charge storage structure 252. Thus, the dummy charge storage structure 250 may include the dummy tunnel insulation pattern 240, the dummy charge trapping pattern 230, and the dummy first blocking pattern 220 sequentially stacked. Each of the dummy tunnel insulation pattern 240 and the dummy first blocking pattern 220 may include an oxide, e.g., silicon oxide as that of the first charge storage structure 252.

**[0044]** The dummy charge trapping pattern 230 may include at least one of silicon, or silicon compounds, e.g., at least one of silicon carbonitride, silicon boronitride, silicon doped with carbon, silicon doped with nitrogen, etc.

**[0045]** Each of the dummy tunnel insulation pattern 240, the dummy charge trapping pattern 230, and the dummy first blocking pattern 220 included in the dummy charge storage structure 250 may have a single layered structure covering the bottom surface and the outer sidewall of the lower end of the channel 260.

**[0046]** In some example embodiments, an upper surface of the dummy charge storage structure 250 may have a shape corresponding to the lower surface of the first charge storage structure 252. Thus, upper surfaces of the dummy tunnel insulation pattern 240 and the dummy charge trapping pattern 230 of the dummy charge storage structure 250 may be lower than the upper surface of the first blocking pattern 220 of the dummy charge storage structure 250.

**[0047]** An inner space formed by the cup-like channel 260 may be filled with the filling pattern 270. The filling pattern 270 may include an oxide, e.g., silicon oxide.

**[0048]** The pad 280 may be formed on the channel 260, the first charge storage structure 252, and the filling pattern 270, and thus may be connected to the channel 260. The pad 280 may include polysilicon, e.g., undoped or doped polysilicon.

**[0049]** The CSP 390 may extend in the second direction, and may form the division structure together with the second spacer 380 on each of opposite sidewalls of the CSP 390 in the third direction to divide each of the gate electrodes 372, 374 and 376 in the third direction. A plurality of CSPs 390 may be spaced apart from each other in the third direction. The CSP 390 may include a metal, e.g., at least one of tungsten, copper, aluminum, etc.

**[0050]** As the second spacer 380 covers the sidewalls of the CSP 390, the CSP 390 may be electrically insulated from neighboring gate electrodes 372, 374 and 376. The second spacer 380 may include an oxide, e.g., silicon oxide.

**[0051]** An impurity region 105 may be formed at an upper portion of the substrate 100 contacting a bottom surface of the CSP 390. The impurity region 105 may include silicon, e.g., single crystalline silicon doped with n-type impurities such as phosphorus and/or arsenic. As the impurity region 105 is formed, the contact resistance between the CSP 390 and the substrate 100 may be reduced.

**[0052]** The support layer 160 may be formed on the channel connection pattern 330, and the support pattern 165 may be connected to the support layer 160 on the substrate 100. The support layer 160 may extend in the second direction between neighboring ones of the division structures in the third direction, and a plurality of support patterns 165 may be formed in each of the second and third directions. The support layer 160 and the support pattern 165 may include substantially the same material, e.g., doped or undoped polysilicon, and may be integrally formed with each other, e.g. may be formed at the same time.

**[0053]** The first to third insulating interlayers 190, 290, and 400 may include an oxide, e.g., silicon oxide, and thus may be merged with each other, e.g. may be homogenized with each

other, e.g. may be homogenized with each other through a thermal process and/or other processing steps.

**[0054]** The contact plug 410 may extend through the second and third insulating interlayers 290 and 400 to contact an upper surface of the pad 280, and the bit line 430 may extend in the third direction to electrically connect to the contact plugs 410 arranged in the third direction. Thus, a current generated from a voltage applied by the bit line 430 may flow through the contact plug 410 and the pad 280 to the channel 260. In some example embodiments, a plurality of bit lines 430 may be formed to be spaced apart from each other in the second direction.

**[0055]** The contact plug 410 and the bit line 430 may include at least one of a metal, a metal nitride, a metal silicide, doped polysilicon, etc.

**[0056]** The vertical memory device may include the first charge storage structure 252 covering the outer sidewall of the portion of the channel 260 extending through the gate electrode structure, and the first charge storage structure 252 may include the charge trapping patterns 232 spaced apart from each other in the first direction by the division pattern 234 and facing one of the gate electrodes 372, 374, and 376 in the horizontal direction. Thus, charges trapped in each of the charge trapping patterns 232 may not move/be moved in the first direction by the gate electrodes 372, 374, and 376 at other levels, and the retention characteristic may be enhanced and/or improved. Accordingly, the vertical memory device including the first charge storage structure 252 may have improved reliability.

**[0057]** FIGS. 3 to 11 are cross-sectional views illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments. FIGS. 9 and 10 are enlarged cross-sectional views of a region X of FIG. 8.

**[0058]** Referring to FIG. 3, a sacrificial layer structure 140 may be formed on a substrate 100, and may be partially removed to form a first opening 150 exposing an upper surface of

the substrate 100. The sacrificial layer structure 140 may be formed with a chemical vapor deposition (CVD) process, such as an atomic layer deposition (ALD) and/or a plasma enhanced chemical vapor deposition (PECVD) process. A photolithography process may be used to form the first opening 150. A support layer 160 may be formed on the substrate 100 and the sacrificial layer structure 140 to at least partially fill the first opening 150. The support layer 160 may be formed with a suitable process such as a PECVD process.

**[0059]** The sacrificial layer structure 140 may include first to third sacrificial layers 110, 120 and 130 sequentially stacked in the first direction on the substrate 100. Each of the first and third sacrificial layers 110 and 130 may include an oxide, e.g., silicon oxide, and the second sacrificial layer 120 may include a nitride, e.g., silicon nitride. Each of the first through third sacrificial layers 110, 120, and 130 may be formed at the same time.

**[0060]** The support layer 160 may include a material having an etching selectivity with respect to the first to third sacrificial layers 110, 120 and 130. For example, the support layer 160 may be formed of or include doped or undoped polysilicon. In some example embodiments, the support layer 160 may be formed by depositing doped or undoped amorphous silicon, and by performing a heat treatment or by being crystallized through heat generated during the deposition process for other structures to include doped or undoped polysilicon. The support layer 160 may be deposited with a CVD process.

**[0061]** The support layer 160 may be conformally deposited. The support layer 160 may have a uniform thickness, and thus a first recess may be formed on a portion of the support layer 160 in the first opening 150. Hereinafter, the portion of the support layer 160 in the first opening 150 may be referred to as a support pattern 165.

**[0062]** An insulation layer 170 may be formed on the support layer 160 to fill the first recess, and an upper portion of the insulation layer 170 may be planarized. The planarization process may include a chemical mechanical polishing (CMP) process and/or an etch back

process.

**[0063]** A fourth sacrificial layer 180 and the insulation layer 170 may be alternately and repeatedly formed on the insulation layer 170, and thus a mold layer may be formed on the substrate 100. Each layer of the fourth sacrificial layer 180 and the insulation layer 170 may be formed simultaneously; however, inventive concepts are not limited thereto. Furthermore, although eight layers of the fourth sacrificial layer 180 and the insulation layer 170 are illustrated in FIG. 3, inventive concepts are not limited thereto, and the number of layers of the fourth sacrificial layer 180 and the insulation layer 170 that are alternately stacked may be an integer more than 8 or less than 8. The fourth sacrificial layer 180 may include a material having an etching selectivity with respect to the insulation layer 170, e.g., a nitride such as silicon nitride.

**[0064]** A patterning process using a photoresist pattern (not shown) as an etching mask may be performed on the insulation layer 170 and the fourth sacrificial layer 180, and a trimming process for reducing an area of the photoresist pattern may be also performed. The patterning process and the trimming process may be alternately and repeatedly performed to form a mold having a plurality of step layers each including the fourth sacrificial layer 180 and the insulation layer 170 sequentially stacked on the substrate 100.

**[0065]** Referring to FIG. 4, a first insulating interlayer 190 may be formed on an uppermost one of the insulation layers 170, and a channel hole 200 may be formed through the first insulating interlayer 190 and the mold to expose an upper surface of the substrate 100 by a dry etching process, e.g. by a dry etching process, such as a reactive ion etching (RIE) process, capable of etching a high aspect ratio hole.

**[0066]** In some example embodiments, the dry etching process may be performed until the upper surface of the substrate 100 may be exposed, and an upper portion of the substrate 100 may be further removed in the dry etching process. In some example embodiments, a

plurality of channel holes 200 may be formed in each of the second and third directions, and thus a channel hole array may be defined.

**[0067]** A preliminary charge storage structure 250, a channel 260, a filling pattern 270, and a pad 280 may be formed in the channel hole 200. The preliminary charge storage structure 350, the channel 260, and the filling pattern 270 may be formed in-situ, at the same time, with an ALD process; however, inventive concepts are not limited thereto. For example, the preliminary charge storage structure 350 may be formed at a different time than either or both of the channel 260 and the filling pattern 270.

**[0068]** Particularly, a preliminary charge storage structure layer and a channel layer may be sequentially formed on a sidewall of the channel hole 200, the exposed upper surface of the substrate 100 and an upper surface of the first insulating interlayer 190, a filling layer may be formed on the channel layer to fill a remaining portion of the channel hole 200, and the filling layer, the channel layer, and the preliminary charge storage structure layer may be planarized, e.g. planarized with a CMP and/or an etchback process, until the upper surface of the first insulating interlayer 190 may be exposed.

**[0069]** By the planarization process, the preliminary charge storage structure 250 and the channel 260 may be formed, each of which may have a cup-like shape and are sequentially stacked on the sidewall of the channel hole 200 and the upper surface of the substrate 100, and the filling pattern 270 may fill an inner space formed by the channel 260.

**[0070]** As the channel hole 200 in which the channel 260 is formed may define the channel hole array, the channel 260 in the channel hole 200 may also define a channel array.

**[0071]** In some example embodiments, the preliminary charge storage structure 250 may include a first blocking pattern 220, a preliminary charge trapping pattern 230, and a tunnel insulation pattern 240 that are sequentially stacked. For example, the first blocking pattern 220 and the tunnel insulation pattern 240 may include an oxide, e.g., silicon oxide. The

preliminary charge trapping pattern 230 may include silicon, or silicon compound, e.g., at least one of silicon carbonitride, silicon boronitride, or silicon doped with nitrogen and/or carbon.

**[0072]** Upper portions of the filling pattern 270, the channel 260 and the preliminary charge storage structure 250 may be removed to form a second recess, a pad layer may be formed on the first insulating interlayer 190 to fill the recess, and the pad layer may be planarized with, e.g. a CMP and/or an etchback process, until the upper surface of the first insulating interlayer 190 may be exposed to form the pad 280.

**[0073]** Referring to FIG. 5, a second insulating interlayer 290 may be formed on the first insulating interlayer 190 and the pad 280, and a second opening 300 may be formed through the first and second insulating interlayers 190 and 290 and the mold by a dry etching process such as a RIE process capable of etching a high aspect-ratio hole.

**[0074]** In some example embodiments, the dry etching process may be performed until an upper surface of the support layer 160 and/or an upper surface of the support pattern 165 is exposed, and an upper portion of the support layer 160 and/or an upper portion of the support pattern 165 may be also removed during the dry etching process. As the second opening 300 is formed, the insulation layers 170 and the fourth sacrificial layers 180 of the mold may be exposed.

**[0075]** In some example embodiments, the second opening 300 may extend in the second direction, and a plurality of second openings 300 may be formed in the third direction. As the second opening 300 is formed, the insulation layer 170 may be transformed into an insulation pattern 175 extending in the second direction, and the fourth sacrificial layer 180 may be transformed into a fourth sacrificial pattern 185 extending in the second direction.

**[0076]** A first spacer layer may be formed, e.g. formed with a PECVD process, on a sidewall of the second opening 300, the exposed upper surfaces of the second opening 300,

an upper surface of the second insulating interlayer 290, and may be etched, e.g. anisotropically etched with, e.g., a dry etching process, to remove portions of the first spacer layer on the upper surfaces of the support layer 160 and the support pattern 165, so that a first spacer 310 is formed and that the upper surfaces of the support layer 160 and the support pattern 165 may be exposed again.

**[0077]** In some example embodiments, the first spacer 310 may include, e.g., undoped amorphous silicon and/or undoped polysilicon. When the first spacer 310 includes undoped amorphous silicon, the undoped amorphous silicon may be crystallized during subsequent deposition and/or thermal processes.

**[0078]** Portions of the support layer 160 and the support pattern 165 not covered by the first spacer 310 and a portion of the sacrificial layer structure 140 thereunder may be removed to enlarge the second opening in a downward direction. Thus, the second opening 300 may expose an upper surface of the substrate 100, and further extend through (e.g. into) an upper portion of the substrate 100.

**[0079]** When the sacrificial layer structure 140 is partially removed, the sidewall of the second opening 300 may be covered by the first spacer 310, and the first spacer 310 includes a material different from that of the sacrificial layer structure 140 so that the insulation patterns 175 and the fourth sacrificial patterns 185 included in the mold may not be removed.

**[0080]** Referring to FIG. 6, the sacrificial layer structure 140 exposed by the second opening 300 may be removed to form a first gap 320 exposing a lower outer sidewall of the preliminary charge storage structure 250, and a portion of the preliminary charge storage structure 250 exposed by the first gap 320 may be further removed to expose a lower outer sidewall of the channel 260.

**[0081]** The sacrificial layer structure 140 and the preliminary charge storage structure 250 may be removed by a wet etching process using, e.g., (buffered) hydrofluoric acid, and/or

by a dry etching process using, e.g., hydrogen fluoride. When the first gap 320 is formed, the support layer 160 and the support pattern 165 may not be removed so that the mold may not collapse.

**[0082]** As the first gap 320 is formed, the preliminary charge storage structure 250 may be divided into an upper portion extending through the mold to cover almost an entire outer sidewall of the channel 260, and a lower portion covering a bottom surface of the channel 260 on the substrate 100.

**[0083]** Hereinafter, the upper portion of the preliminary charge storage structure 250 covering almost the entire outer sidewall of the channel 260 may be referred to as the preliminary charge structure 250, and the lower portion of the preliminary charge storage structure 250 covering the bottom surface of the channel 260 on the substrate 100 may be referred to as a dummy charge storage structure. The tunnel insulation pattern 240, the preliminary charge trapping pattern 230, and the first blocking pattern 220 that are included in the dummy charge storage structure 250 may be referred to as a dummy tunnel insulation pattern, a dummy charge trapping pattern, and a dummy first blocking pattern, respectively.

**[0084]** Referring to FIG. 7, after removing the first spacer 310, a channel connection pattern 330 may be formed to fill the first gap 320.

**[0085]** The channel connection pattern 330 may be formed, e.g. formed with a PECVD process and/or with a low pressure chemical vapor deposition (LPCVD) process, by forming a channel connection layer on the substrate 100 and the second insulating interlayer 290 to fill the second opening 300 and the first gap 320, and performing an etch back process on the channel connection layer. The channel connection layer may include, e.g., amorphous silicon doped with n-type impurities such as phosphorus, and may be crystallized by heat generated during subsequent deposition/thermal processes so as to include polysilicon doped with n-type impurities. As the channel connection pattern 330 is formed, the channels 260

between neighboring ones of the second openings 300 in the third direction may be connected with each other to form a channel block.

**[0086]** An air gap 340 may be formed in the channel connection pattern 330; however, inventive concepts are not limited thereto.

**[0087]** Referring to FIG. 8, for example, impurities such as n-type impurities including at least one of phosphorus or arsenic, and/or p-type impurities including boron, may be implanted, e.g. with a beamline implantation process, into an upper portion of the substrate 100 exposed by the second opening 300 to form an impurity region 105.

**[0088]** The fourth sacrificial patterns 185 may be removed to form a second gap 350 exposing an outer sidewall of the preliminary charge storage structure 250. The fourth sacrificial patterns 185 may be removed by a wet etching process using e.g., phosphoric acid and/or (buffered) hydrofluoric acid and/or by a dry etching process.

**[0089]** Referring to FIG. 9, a first nitridation process may be performed on the preliminary charge storage structure 250 through the second gap 350.

**[0090]** In some example embodiments, the first nitridation process may include a decoupled plasma nitride (DPN) process and/or a rapid thermal nitridation (RTN) process using at least one of nitrogen (N), nitric oxide (NO), ammonia (NH<sub>3</sub>), etc., and/or an annealing process. By the first nitridation process, the preliminary charge trapping pattern 230 of the preliminary charge storage structure 250 may be partially nitridated to form a charge trapping pattern 232.

**[0091]** The first nitridation process may be performed on the preliminary charge trapping pattern 230 through a portion of the first blocking pattern 220 exposed by the second gap 350. Thus, nitrogen may be implanted into a portion of the preliminary charge trapping pattern 230 overlapping the second gap 350 in a horizontal direction substantially parallel to the upper surface of the substrate 100 and a portion of the preliminary charge trapping

pattern 230 adjacent thereto in the first direction so that the portions of the preliminary charge trapping pattern 230 including silicon (e.g. silicon without nitrogen) may be transformed into the charge trapping pattern 232 including silicon nitride (SiN).

**[0092]** In some example embodiments, a plurality of charge trapping patterns 232 may be formed to be spaced apart from each other in the first direction, and a first length L1 in the first direction of an inner sidewall of each of the charge trapping patterns 232 contacting the tunnel insulation pattern 240 may be less than a second length L2 in the first direction of an outer sidewall of each of the charge trapping patterns 232 contacting the first blocking pattern 220. However, the first length L1 of each of the charge trapping patterns 232 may be greater than a third length L3 in the first direction of a corresponding one of the second gaps 350.

**[0093]** In some example embodiments, a length in the first direction of each of the charge trapping patterns 232 may gradually increase from the tunnel insulation pattern 240 to the first blocking pattern 220, and an absolute value of a slope of an upper surface or a lower surface of each of the charge trapping patterns 232 with respect to the upper surface of the substrate 100 may decrease from the tunnel insulation pattern 240 to the first blocking pattern 220. In some example embodiments, the charge trapping patterns 232 may be concave, e.g. concave in the third direction from the tunnel insulation pattern 240 to the first blocking pattern 220.

**[0094]** Referring to FIG. 10, a first oxidation process may be performed on the preliminary charge storage structure 250 through the second gap 350.

**[0095]** In some example embodiments, the first oxidation process may include at least one of a rapid thermal oxidation (RTO) process, an annealing process, a dry oxidation process, a wet oxidation process, etc. The first oxidation process may be or include a selective oxidation process in which the charge trapping pattern 232 including silicon nitride may not

be oxidized or may only be partially oxidized, for example may not be oxidized because of the inclusion of nitride. For example, the charge trapping pattern 232 may serve as an oxidation prevention pattern (or an oxidation reduction pattern) during the first oxidation process. By the first oxidation process, a remaining portion of the preliminary charge trapping pattern 230 in the preliminary charge storage structure 250 may be oxidized, and may form a division pattern 234.

**[0096]** However, a lower portion of the preliminary charge trapping pattern 230 may not be affected by the first nitridation process or the first oxidation process, so as not to be converted into the charge trapping pattern 232 or the division pattern 234 but to remain, e.g. to remain as the preliminary charge trapping pattern 230.

**[0097]** By the first oxidation process, a portion of the preliminary charge trapping pattern 230 between neighboring ones of the charge trapping patterns 232 in the first direction may be oxidized to form the division pattern 234 including silicon oxide ( $\text{SiO}_2$ ). In some example embodiments, an absolute value of a slope of an upper surface or a lower surface of the division pattern 234 with respect to the upper surface of the substrate 100 may gradually decrease from the tunnel insulation pattern 240 to the first blocking pattern 220.

**[0098]** Hereinafter, the tunnel insulation pattern 240, the charge trapping patterns 232, the division patterns 234, and the first blocking pattern 220 may be referred to as a first charge storage structure 252. For example, the first charge storage structure 252 may be formed on an outer sidewall of the channel 260 on the channel connection pattern 330, and the dummy charge storage structure 250 may be formed on an outer sidewall and a bottom surface of the channel 260 under the channel connection pattern 330.

**[0099]** Referring to FIG. 11, a second blocking layer may be formed on the exposed outer sidewall of the first charge storage structure 252, inner walls of the second gaps 350, surfaces of the insulation patterns 175, sidewalls of the support layer 160 and the support pattern 165,

a sidewall of the channel connection pattern 330, the upper surface of the substrate 100, and an upper surface of the second insulating interlayer 290, and a gate electrode layer may be formed on the second blocking layer. The gate electrode layer may include a gate barrier layer and a gate conductive layer that are sequentially stacked.

**[0100]** The gate electrode layer may be partially removed to form a gate electrode in each of the second gaps 350. In some example embodiments, the gate electrode layer may be partially removed by a wet etching process.

**[0101]** In some example embodiments, the gate electrode may extend in the second direction, and a plurality of gate electrodes may be formed in the first direction. Additionally or alternatively, a plurality of gate electrodes may be formed in the third direction. For example, the gate electrodes each of which may extend in the second direction may be spaced apart from each other by the second opening 300.

**[0102]** The gate electrode may include first, second, and third gate electrodes 372, 374, and 376.

**[0103]** A second spacer layer may be formed on the second blocking layer (e.g. within the second opening 300), and anisotropically etched to form a second spacer 380 on the sidewall of the second opening 300. Thus an upper surface of the second blocking layer on the substrate 100 may be partially exposed.

**[0104]** A portion of the second blocking layer not covered by the second spacer 380 may be etched to form a second blocking pattern 360, and a portion of the second blocking layer on the upper surface of the second insulating interlayer 290 may be also removed. Additionally, an upper portion of the impurity region 105 may be partially removed.

**[0105]** A conductive layer may be formed, e.g. formed with a PECVD process or with a PECVD process and a sputter process, on the upper surface of the impurity region 105, the second spacer 380, and the second insulating interlayer 290 to fill a remaining portion of the

second opening 300. The conductive layer may be planarized, e.g. may be planarized with a CMP process and/or with an etchback process until the upper surface of the second insulating interlayer 290 may be exposed to form a CSP 390. The CSP 390 may include a metal, such as tungsten, and/or may include a (doped) polysilicon layer; however, inventive concepts are not limited thereto.

**[0106]** Referring to FIGS. 1 and 2 again, after forming a third insulating interlayer 400 on the second insulating interlayer 290, the CSP 390, the second spacer 380, and the second blocking pattern 360, a contact plug 410 may be formed through the second and third insulating interlayers 290 and 400 to contact an upper surface of the pad 280.

**[0107]** A bit line 430 may be formed to contact an upper surface of the contact plug 410 so that the vertical memory device may be manufactured.

**[0108]** As illustrated above, the first nitridation process may be performed on the preliminary charge storage structure 250 including the preliminary charge trapping pattern 230 to form a plurality of charge trapping patterns 232 spaced apart from each other, and the first oxidation process may be performed to form the division pattern 234 between the charge trapping patterns 232. For example, instead of a physical process such as a cutting process and/or a patterning process on the preliminary charge trapping pattern 230 extending in the first direction, a chemical process such as the nitridation process and/or the oxidation process may be performed so that the charge trapping patterns 232 facing the gate electrodes 372, 374 and 376 may be formed to be spaced apart from each other in the first direction.

**[0109]** FIG. 12 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments, and an enlarged cross-sectional view of the region X of FIG. 1. This vertical memory device may be substantially the same as or similar to that of FIGS. 1 and 2, except for the charge storage structure. Thus, like reference numerals refer to like elements, and repetitive descriptions thereon are omitted herein.

**[0110]** Referring to FIG. 12, the vertical memory device may include a second charge storage structure 254 instead of, or in addition to, the first charge storage structure 252, and the second charge storage structure 254 may include the tunnel insulation pattern 240, the preliminary charge trapping pattern 230, the charge trapping pattern 232, and the first blocking pattern 220 that are sequentially stacked in the horizontal direction from the outer sidewall of the channel 260. The second charge storage structure 254 may further include the division pattern 234.

**[0111]** The preliminary charge trapping pattern 230 may be the remaining portion of the preliminary charge trapping pattern 230 that has not been converted into the charge trapping pattern 232 by the first nitridation process, which may be referred to as a first charge trapping pattern hereinafter, and the charge trapping pattern 232 may be referred to as a second charge trapping pattern.

**[0112]** For example, the second charge storage structure 254 may include the first and second charge trapping patterns 230 and 232 facing a corresponding one of the gate electrodes 372, 374, and 376 spaced apart from each other in the first direction between the tunnel insulation pattern 240 and the first blocking pattern 220, each of which may extend in the first direction. The first charge trapping pattern 230 may include silicon or silicon compounds, e.g., at least one of silicon carbonitride, silicon boronitride, or silicon doped with at least one of nitrogen or carbon. The second charge trapping pattern 232 may include, e.g., silicon nitride.

**[0113]** In some example embodiments, a fifth length L5 in the first direction of the first charge trapping pattern 230 may gradually decrease from the tunnel insulation pattern 240 to the second charge trapping pattern 232.

**[0114]** In some example embodiments, the second charge trapping pattern 232 may include a first portion 232a covering an outer sidewall of the first charge trapping pattern 230 and

contacting the first blocking pattern 220, and a second portion 232b extending from the first portion 232a toward the tunnel insulation pattern 240 to cover upper and lower surfaces of the first charge trapping pattern 230. A length in the first direction of the first portion 232a of the second charge trapping pattern 232 may gradually increase as it approaches the first blocking pattern 220, and the second portion 232b of the second charge trapping pattern 232 may be slanted with respect to the upper surface of the substrate 100.

**[0115]** In some example embodiments, a length, e.g. a maximum length in the first direction of the second charge trapping pattern 232, that is, a sixth length L6 of the first portion 232a of the second charge trapping pattern 232 contacting the first blocking pattern 220 may be greater than the fourth length L4 in the first direction of the corresponding ones of the gate electrodes 372, 374 and 376 or the third length L3 in the first direction of the second gap 350 in which each of the gate electrodes 372, 374 and 376 may be formed.

**[0116]** The division pattern 234 may be formed between neighboring ones of the first and second charge trapping patterns 230 and 232 in the first direction, and thus the first and second charge trapping patterns 230 and 232 may be spaced apart from each other in the first direction. The division pattern 234 may face the insulation pattern 175 in the horizontal direction, particularly, a central portion in the first direction of the insulation pattern 175.

**[0117]** In some example embodiments, the division pattern 234 may include a first portion 234a of which a length in the first direction may gradually increase from the tunnel insulation pattern 240 toward the first blocking pattern 220, and a second portion 234b of which a length in the first direction may gradually decrease from the first portion 234a toward the first blocking pattern 220. A length, e.g. a minimum length in the first direction of the first portion 234a of the division pattern 234, that is, a seventh length L7 in the first direction of an inner sidewall of the first portion 234a of the division pattern 234 contacting the tunnel insulation pattern 240 may be greater than a length, e.g. a minimum length in the

first direction of the second portion 234b of the division pattern 234, that is, an eighth length L8 in the first direction of the second portion 234b of the division pattern 234 contacting the first blocking pattern 220.

**[0118]** In some example embodiments, the division pattern 234 may include a material substantially the same as that of the first blocking pattern 220, e.g., silicon oxide, and thus may be merged therewith, e.g. may be merged therewith in subsequent thermal processing steps.

**[0119]** FIGS. 13 to 16 are cross-sectional views, particularly, enlarged cross-sectional views of the region X of FIG. 1 illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments. This method may include processes substantially the same as or similar to those of FIGS. 3 to 11 and FIGS. 1 and 2, and thus repetitive descriptions thereon are omitted herein.

**[0120]** Referring to FIG. 13, processes substantially the same as or similar to those illustrated with reference to FIGS. 3 to 9 may be performed.

**[0121]** However, in addition to or alternative to the process illustrated with reference to FIGS. 3 to 9, the first nitridation process may be performed on the preliminary charge storage structure 250 through the second gap 350, so that only a portion of the preliminary charge trapping pattern 230 adjacent the first blocking pattern 220 may be nitridated to form the charge trapping pattern 232.

**[0122]** Referring to FIG. 14, processes substantially the same as or similar to those illustrated with reference to FIG. 10 may be performed.

**[0123]** For example, the first oxidation process may be performed on the preliminary charge storage structure 250 through the second gap 350, and thus a portion of the preliminary charge trapping pattern 230 facing the insulation pattern 175 in the horizontal direction may be oxidized to form the division pattern 234.

**[0124]** The charge trapping pattern 232 contacting the first blocking pattern 220 and the preliminary charge trapping pattern 230 contacting the tunnel insulation pattern 240 may be formed between neighboring ones of the division patterns 234 in the first direction.

**[0125]** Referring to FIG. 15, a second nitridation process may be performed on the preliminary charge storage structure 250 through the second gap 350 to form a second charge storage structure 254.

**[0126]** The second nitridation process may be substantially the same as the first nitridation process, and thus the preliminary charge trapping pattern 230 may be partially nitridated to further form the charge trapping pattern 232.

**[0127]** In some example embodiments, lower and upper ends of the preliminary charge trapping pattern 230 may be nitridated by the second nitridation process, and the nitridated portion may be merged to the charge trapping pattern 232 having been already formed.

**[0128]** Referring to FIG. 16, a curing process may be performed on the second charge storage structure 254 through the second gap 350.

**[0129]** The curing process may be performed on the first blocking pattern 220 including, e.g., silicon oxide, and may cure the damaged first blocking pattern 220 by the previous first and second nitridation processes. In some example embodiments, the curing process may include a wet etching process.

**[0130]** The wet etching process may affect the division pattern 234, and thus the division pattern 234 and the first blocking pattern 220 may include substantially the same material to be merged therewith.

**[0131]** Processes substantially the same as or similar to those illustrated with reference to FIG. 11 and FIGS. 1 and 2 may be performed to complete the fabrication of the vertical memory device.

**[0132]** FIG. 17 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments, and an enlarged cross-sectional view of the region X of FIG. 1.

**[0133]** Referring to FIG. 17, the vertical memory device may include a third charge storage structure 256 instead of, or in addition to, the first charge storage structure 252, and the third charge storage structure 256 may include the tunnel insulation pattern 240, the first charge trapping pattern 230, a third charge trapping pattern 236, and the first blocking pattern 220 that are sequentially stacked in the horizontal direction from the outer sidewall of the channel 260. The third charge storage structure 256 may further include the division pattern 234.

**[0134]** The third charge storage structure 256 may include the first and third charge trapping patterns 230 and 236 facing a corresponding one of the gate electrodes 372, 374, and 376 spaced apart from each other in the first direction between the tunnel insulation pattern 240 and the first blocking pattern 220, each of which may extend in the first direction. The third charge trapping pattern 236 may include, e.g., silicon nitride.

**[0135]** In some example embodiments, the third charge trapping pattern 236 may cover an outer sidewall and lower and upper surfaces of the first charge trapping pattern 230. The division pattern 234 may extend in the first direction to cover an outer sidewall and lower and upper surfaces of the third charge trapping pattern 236. Thus, the first and third charge trapping patterns 230 and 236 may be spaced apart from each other in the first direction by the division pattern 234.

**[0136]** In some example embodiments, a thickness of the division pattern 234 may be greater than that of the tunnel insulation pattern 240 or the first blocking pattern 220. The division pattern 234 may include a material substantially the same as that of the first blocking pattern 220, and thus may be merged therewith.

[0137] FIGS. 18 to 22 are cross-sectional views, particularly, enlarged cross-sectional views of the region X of FIG. 1 illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments.

[0138] Referring to FIG. 18, processes substantially the same as or similar to those illustrated with reference to FIGS. 3 to 9 may be performed.

[0139] However, a thickness of the preliminary charge trapping pattern 230 may be greater than that of the tunnel insulation pattern 240 or the first blocking pattern 220, and when the first nitridation process is performed on the preliminary charge storage structure 250 through the second gap 350, only a portion of the preliminary charge trapping pattern 230 adjacent the first blocking pattern 220 may be nitridated to form the charge trapping pattern 232.

[0140] Referring to FIG. 19, processes substantially the same as or similar to those illustrated with reference to FIG. 10 may be performed.

[0141] For example, the first oxidation process may be performed on the preliminary charge storage structure 250 through the second gap 350, and thus a portion of the preliminary charge trapping pattern 230 facing the insulation pattern 175 in the horizontal direction may be oxidized to form the division pattern 234. However, as the preliminary charge trapping pattern 230 has the relatively large thickness, only a portion of the preliminary charge trapping pattern 230 adjacent the insulation pattern 175 may be oxidized to form the division pattern 234, and the preliminary charge trapping pattern 230 may not be divided into a plurality of pieces in the first direction by the first oxidation process.

[0142] Referring to FIG. 20, a second oxidation process may be performed on the preliminary charge storage structure 250 through the second gap 350.

[0143] In some example embodiments, the second oxidation process may include a radical oxidation process using at least one of oxygen radical ( $O^*$ ), hydroxyl radical ( $OH^*$ ), etc.,

and not only the preliminary charge trapping pattern 230 but also the charge trapping pattern 232 including silicon nitride may be oxidized, unlike the first oxidation process.

**[0144]** Thus, the division pattern 234 may be enlarged by the second oxidation process to cover an outer sidewall and lower and upper surfaces of the preliminary charge trapping pattern 230 that may extend in the first direction and has not been converted into the charge trapping pattern 232. The division pattern 234 before being enlarged may be referred to as a preliminary division pattern in comparison with the division pattern 234 after being enlarged. The preliminary charge trapping pattern 230 may be divided into a plurality of pieces spaced apart from each other in the first direction by the second oxidation process.

**[0145]** Referring to FIG. 21, the second nitridation process may be performed on the preliminary charge storage structure 250 through the second gap 350 to form a third charge storage structure 256.

**[0146]** As the second nitridation process is performed, the outer sidewall and the lower and upper surfaces of the preliminary charge trapping pattern 230 may be nitridated to form a third charge trapping pattern 236 including silicon nitride.

**[0147]** Referring to FIG. 22, the curing process may be performed on the third charge storage structure 256 through the second gap 350, and thus the damaged first blocking pattern 220 by the previous first and second nitridation processes may be cured.

**[0148]** The curing process may affect the division pattern 234, and thus the division pattern 234 and the first blocking pattern 220 may include substantially the same material to be merged therewith.

**[0149]** Processes substantially the same as or similar to those illustrated with reference to FIG. 11 and FIGS. 1 and 2 may be performed to complete the fabrication of the vertical memory device.

**[0150]** FIG. 23 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments, and an enlarged cross-sectional view of the region X of FIG. 1. This vertical memory device may be substantially the same as or similar to that of FIG. 17, except for the division pattern and the first blocking pattern.

**[0151]** Referring to FIG. 23, the vertical memory device may include a fourth charge storage structure 258 instead of or in addition to the third charge storage structure 256, and the fourth charge storage structure 258 may include the tunnel insulation pattern 240, the first charge trapping pattern 230, the third charge trapping pattern 236, and the first blocking pattern 220 sequentially stacked in the horizontal direction from the outer sidewall of the channel 260. The first blocking pattern 220 may extend in the first direction to divide each of the first and third charge trapping patterns 230 and 236, and thus may serve as the division pattern 234.

**[0152]** FIGS. 24 to 26 are cross-sectional views, particularly, enlarged cross-sectional views of the region X of FIG. 1 illustrating a method of manufacturing a vertical memory device in accordance with some example embodiments. This method may include processes substantially the same as or similar to those illustrated with reference to FIGS. 18 to 22 and FIG. 17, and thus repetitive descriptions thereon are omitted herein.

**[0153]** Referring to FIG. 24, processes substantially the same as or similar to those illustrated with reference to FIG. 18 may be performed.

**[0154]** However, the preliminary charge storage structure 250 may not include the first blocking pattern 220, and thus the first nitridation process may be performed directly on the preliminary charge trapping pattern 230 not through the first blocking pattern 220. By the first nitridation process, only the portion of the preliminary charge trapping pattern 230 adjacent the second gap 350 may be nitridated to form the charge trapping pattern 232.

**[0155]** Referring to FIG. 25, processes substantially the same as or similar to those illustrated with reference to FIG. 19 may be performed, and thus the portion of the preliminary charge trapping pattern 230 adjacent the insulation pattern 175 may be oxidized to form the division pattern 234.

**[0156]** Referring to FIG. 26, processes substantially the same as or similar to those illustrated with reference to FIGS. 20 and 21 may be performed, so that the first and third charge trapping patterns 230 and 236 spaced apart from each other by the division pattern 234 may be formed.

**[0157]** Processes substantially the same as or similar to those illustrated with reference to FIG. 22 may be performed to form a fourth charge storage structure 258.

**[0158]** For example, a curing process such as a wet etching process may be performed to cure the division pattern 234, and the cured division pattern 234 may serve as the first blocking pattern 220.

**[0159]** Processes substantially the same as or similar to those illustrated with reference to FIG. 11 and FIGS. 1 and 2 may be performed to complete the fabrication of the vertical memory device.

**[0160]** FIG. 27 is a cross-sectional view illustrating a vertical memory device in accordance with some example embodiments. This vertical memory device may be substantially the same as or similar to that of FIGS. 1 and 2, except for the channel, the dummy charge storage structure, and the gate electrode.

**[0161]** Referring to FIG. 27, the vertical memory device may not include the dummy charge storage structure 250, the channel connection pattern 330, the support layer 160 and the support pattern 165, unlike that of FIGS. 1 and 2.

**[0162]** Meanwhile, a semiconductor pattern 210 may be formed in a lower portion of the channel hole 200, and the channel 260 and the first charge storage structure 252 may be formed on the semiconductor pattern 210.

**[0163]** The first gate electrode 372 may surround a sidewall of the semiconductor pattern 210, and each of the second and third gate electrodes 374 and 376 may surround an outer sidewall of the first charge storage structure 252.

**[0164]** FIG. 27 shows that the vertical memory device includes the first charge storage structure 252, however, the inventive concept may not be limited thereto, and may include one of the second to fourth charge storage structures 254, 256 and 258.

**[0165]** FIGS. 28 to 30 are cross-sectional views illustrating a vertical memory device in accordance with some example embodiments.

**[0166]** Referring to FIG. 28, processes substantially the same as or similar to those illustrated with reference to FIG. 3 may be performed. However, the sacrificial layer structure 140, the support layer 160 and the support pattern 165 may not be formed on the substrate 100, and the mold including the insulation layer 170 and the fourth sacrificial layer 180 alternately and repeatedly stacked may be formed on the substrate 100.

**[0167]** Referring to FIG. 29, processes substantially the same as or similar to those illustrated with reference to FIG. 4 may be performed. However, a semiconductor pattern 210 may be formed by a selective epitaxial growth (SEG) process to fill a lower portion of the channel hole 200, and the preliminary charge storage structure 250, the channel 260, the filling pattern 270, and the pad 280 may be formed on the semiconductor pattern 210 to fill the channel hole 200.

**[0168]** Referring to FIG. 30, processes substantially the same as or similar to those illustrated with reference to FIGS. 5 to 8 may be performed. However, the channel connection pattern 330 may not be formed on the substrate 100, and the fourth sacrificial

pattern 185 exposed by the second opening 300 may be removed to form the second gap 350 exposing the preliminary charge storage structure 250 and the semiconductor pattern 210.

**[0169]** Referring to FIG. 27 again, processes substantially the same as or similar to those illustrated with reference to FIGS. 9 to 11 and FIGS. 1 and 2 may be performed to complete the fabrication of the vertical memory device.

**[0170]** While example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the claims.

WHAT IS CLAIMED IS:

1. A vertical memory device comprising:

a channel on a substrate, the channel extending in a vertical direction that is perpendicular to an upper surface of the substrate;

a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern, and a first blocking pattern that are sequentially stacked in a horizontal direction, the horizontal direction parallel to the upper surface of the substrate; and

gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure,

wherein the charge storage structure includes charge trapping patterns spaced apart from each other in the vertical direction, each of the charge trapping patterns facing one of the gate electrodes in the horizontal direction, and

wherein a first length in the vertical direction of an inner sidewall of at least one of the charge trapping patterns facing the tunnel insulation pattern is less than a second length in the vertical direction of an outer sidewall of a respective at least one of the charge trapping patterns facing the first blocking pattern.

2. The vertical memory device of claim 1, wherein the first length of the at least one of the charge trapping pattern is greater than a third length in the vertical direction of a respective one of the gate electrodes.

3. The vertical memory device of claim 1 or claim 2, wherein an absolute value of a slope of an upper surface of each of the charge trapping patterns with respect to the upper surface of the substrate gradually decreases from the tunnel insulation pattern toward

the first blocking pattern.

4. The vertical memory device of any one of claims 1 to 3, wherein the charge storage structure is between ones of the charge trapping patterns neighboring in the vertical direction and contacting the tunnel insulation pattern and the first blocking pattern, and wherein the charge storage structure further includes a division pattern including silicon oxide.

5. The vertical memory device of claim 4, wherein an absolute value of a slope of an upper surface of the division pattern with respect to the upper surface of the substrate gradually decreases from the tunnel insulation pattern toward the first blocking pattern.

6. The vertical memory device of any one of claims 1 to 5, wherein each of the tunnel insulation pattern and the first blocking pattern extends in the vertical direction, and the charge trapping patterns are between the tunnel insulation pattern and the first blocking pattern.

7. The vertical memory device of any one of claims 1 to 6, wherein the charge trapping patterns include silicon nitride, and each of the tunnel insulation pattern and the first blocking pattern includes silicon oxide.

8. The vertical memory device of any one of claims 1 to 7, further comprising:  
a second blocking pattern covering lower surfaces, upper surfaces, and a sidewall of each of the gate electrodes, the second blocking pattern including a metal oxide, the sidewall facing the charge storage structure in the horizontal direction.

9. The vertical memory device of any one of claims 1 to 8, wherein the gate electrodes include second and third gate electrodes configured to serve as a word line and an SSL, respectively, and

wherein the vertical memory device further includes,

a semiconductor pattern on the substrate, the semiconductor pattern contacting bottom surfaces of the channel and the charge storage structure, and

a first gate electrode under the second gate electrode on the substrate, the first gate electrode surrounding the semiconductor pattern and configured to serve as a GSL.

10. A vertical memory device comprising:

a channel on a substrate, the channel extending in a vertical direction that is perpendicular to an upper surface of the substrate;

a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern structure, and a blocking pattern that are sequentially stacked in a horizontal direction parallel to the upper surface of the substrate; and

gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure,

wherein the charge storage structure includes charge trapping pattern structures spaced apart from each other in the vertical direction, each of the charge trapping pattern structures facing a corresponding one of the gate electrodes in the horizontal direction, and

wherein each of the charge trapping pattern structures includes first and second charge trapping patterns that are sequentially stacked in the horizontal direction on an outer

sidewall of the tunnel insulation pattern, the first and second trapping patterns including different materials from each other.

11. The vertical memory device of claim 10, wherein the first charge trapping pattern includes at least one of silicon carbonitride, silicon boronitride, silicon, or silicon doped with at least one of nitrogen or carbon, and the second charge trapping pattern includes silicon nitride.

12. The vertical memory device of claim 10 or claim 11, wherein a length in the vertical direction of the first charge trapping pattern gradually decreases from the tunnel insulation pattern toward the second charge trapping pattern.

13. The vertical memory device of any one of claims 10 to 12, wherein the second charge trapping pattern covers an outer sidewall and lower and upper surfaces of the first charge trapping pattern.

14. The vertical memory device of any one of claims 10 to 13, wherein a length in the vertical direction of the second charge trapping pattern is greater than a length in the vertical direction of the corresponding one of the gate electrodes.

15. The vertical memory device of any one of claims 10 to 14, wherein the blocking pattern extends in the vertical direction, and covers an outer sidewall and lower and upper surfaces of the charge trapping patterns.

16. A vertical memory device comprising:

a channel on a substrate, the channel extending in a vertical direction perpendicular to an upper surface of the substrate;

a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern, and a blocking pattern that are sequentially stacked in a horizontal direction parallel to the upper surface of the substrate;

a dummy charge storage structure spaced apart from the charge storage structure in the vertical direction on the substrate, the dummy charge storage structure including a dummy tunnel insulation pattern, a dummy charge trapping pattern, and a dummy blocking pattern that are sequentially stacked; and

gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure,

wherein the charge storage structure includes charge trapping patterns spaced apart from each other in the vertical direction, each of the charge trapping patterns facing a corresponding one of the gate electrodes in the horizontal direction, and

wherein the dummy tunnel insulation pattern and the dummy blocking pattern include materials substantially the same as those of the tunnel insulation pattern and the blocking pattern, respectively, and the dummy charge trapping pattern includes a material different from that of the charge trapping patterns.

17. The vertical memory device of claim 16, wherein each of the charge trapping patterns includes silicon nitride, and the dummy charge trapping pattern includes at least one of silicon carbonitride, silicon boronitride, silicon, or silicon doped with at least one of nitrogen or carbon.

18. The vertical memory device of claim 16, wherein

each of the charge trapping patterns includes first and second charge trapping patterns sequentially stacked from the tunnel insulation pattern in the horizontal direction, and

the first charge trapping pattern includes a material substantially the same as that of the dummy charge trapping pattern, and the second charge trapping pattern includes a material different from that of the dummy charge trapping pattern.

19. The vertical memory device of any one of claims 16 to 18, wherein a length in the vertical direction of an inner sidewall of each of the charge trapping patterns contacting the tunnel insulation pattern is less than a length in the vertical direction of an outer sidewall of each of the charge trapping patterns contacting the blocking pattern.

20. The vertical memory device of any one of claims 16 to 19, further comprising:

a division pattern between ones of the charge trapping patterns that neighbor in the vertical direction, the division pattern contacting the tunnel insulation pattern and the blocking pattern and including silicon oxide.