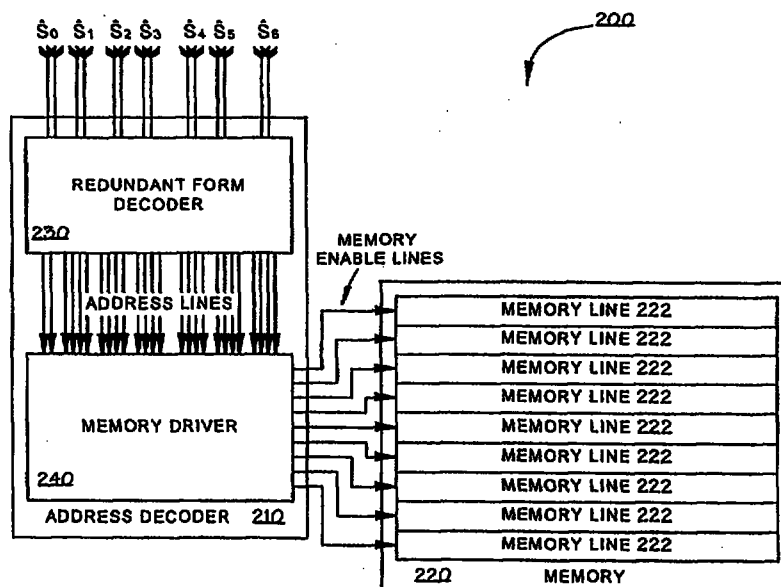




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

51) International Patent Classification ⁷ : G06F 12/00	A2	(11) International Publication Number: WO 00/17757 (43) International Publication Date: 30 March 2000 (30.03.00)
21) International Application Number: PCT/US99/27873 22) International Filing Date: 27 August 1999 (27.08.99) 30) Priority Data: 09/148,314 4 September 1998 (04.09.98) US 71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, P.O. Box 58119, Santa Clara, CA 95052-8119 (US). 72) Inventor: SAGER, David, J.; 9540 N.W. Skyview Drive, Portland, OR 97231 (US). 74) Agents: HELLER, Paul, H. et al.; Kenyon & Kenyon, Suite 700, 1500 K Street, N.W., Washington, DC 20005 (US).		(81) Designated States: BR, CN, KR, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>Without international search report and to be republished upon receipt of that report.</i>

54) Title: REDUNDANT FORM ADDRESS DECODER FOR MEMORY SYSTEM



7) Abstract

The present invention provides a memory system (200) that retrieves data based upon redundant form address data. The memory system (200) includes a memory (220) having a plurality of memory lines (222) and an address decoder (210) that enables one of the memory lines (222) in response to a redundant form address signal. A redundant form decoder (230) decodes redundant form data into differential pair of decoded address lines for each bit position of a memory address. One of the two differential pairs carries correct address data. The one address line to be used is determined on a memory line by memory line basis, using the address of the memory lines themselves. The redundant form address decoder (230) avoids a completion add that would otherwise be required, yielding very fast access to memory.