

Packetized Digital Datastream Apparatus

Abstract Of The Disclosure

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A transmission processor (16) receives an input packetized datastream (14) containing packets of data bytes including MPEG coded video information. The transmission processor outputs (18) a symbol datastream (representing a sequence of data fields comprising groups of data segments (X) with an associated field sync segment. The transmission processor inserts overhead information, eg., FEC error coding information, into each data segment, and inserts the longer duration field sync overhead segment between groups of data field segments. The frequency of the transmission processor input byte clock ($SC/2$) is an integer sub-multiple of an output symbol clock (SC) frequency. The input datastream (14) exhibits constant uniform inter-packet data gaps and a constant uniform data rate, thereby facilitating the seamless insertion (18) of the field sync overhead segment into the datastream without interrupting the datastream. Similar but inverse processing occurs at a receiver.

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Figure 2