

A Clock Switching Circuit

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Background and Field of the Invention

5 This invention relates to a clock switching circuit for switching between a plurality of clock signals.

A clock switching circuit is employed in a wide variety of applications, for example, as a variable timing reference in a processor, in phase lock loop
10 systems for synchronising to different signals or in data telecommunications when communicating at different data rates.

Conventional switching circuits suffer from a drawback that the switching between clock signals causes "glitches" to occur at the output of the switching
15 circuit which are undesirable since such glitches can create timing errors. There has been proposed switching circuits which alleviate this problem and an example of which is described in a patent document US5,652,536. In this prior art, glitches are minimised or eliminated by synchronising a clock select signal, which is used to indicate the switching between a current to a new clock signal,
20 to a falling edge of the new clock signal.

It is an object of the invention to provide an alternative clock switching circuit which is easy to implement.

Summary of the invention

According to a first aspect of the invention, there is provided a clock switching circuit comprising

- 5 i) a switch having a first input arranged to receive a first clock signal, a second input arranged to receive a second clock signal, a control input, and a switch output, the control input selectively connecting the switch output to the said first clock signal or the said second clock signal;
- 10 ii) a first flip flop having a data input arranged to receive a clock select signal which provides an indication to switch from the first clock signal to the second clock signal, a clock input, and a data output;
- 15 iii) a second flip flop having a first data input coupled to the data output of the first flip-flop, a clock input coupled to the switch output of the switch, and a data output,
- iv) an XNOR logic gate having a first input coupled to the data output of the first flip-flop, a second input coupled to the data output of the second flip-flop, and an output; and
- 20 v) an AND logic gate having a first input coupled to the output of the XNOR logic gate, a second input coupled to the switch output, and an output; the output of the AND gate arranged to provide the first clock signal and is coupled to the clock input of the first flip flop;

the arrangement being such that on detection of the indication for the switching by the first flip-flop, the output of the AND gate switches from the first clock signal to an intermediate state and subsequently to the second clock signal; the

switching from the intermediate state to the second clock signal being synchronised to a falling edge of the second clock signal.

An advantage of the described embodiment of the invention is that with the
5 switching from the first clock signal (current) to the second clock signal (new) being synchronised to a falling edge of the second clock signal, glitch is minimised or eliminated.

The described embodiment also has a further advantage that the arrangement
10 is simpler and easier to implement as compared to the conventional design.

Brief Description of the Drawings

An embodiment of the invention will now be described, by way of example, with
15 reference to the accompanying drawings, in which: -

Figure 1 is a circuit diagram of a clock switching circuit according to the invention; and

Figure 2 depicts a timing diagram of the various input and output signals
20 of the clock switching circuit of Figure 1;

Detailed Description of the Preferred Embodiment

Figure 1 illustrates a clock switching circuit 10 according to the invention which comprises two flip-flops and in this embodiment, they are in the form of a first D-type flip flop 20 cascaded with a second D-type flip flop 30. The clock switching
5 circuit 10 further comprises a switch such as a multiplexer 40, an "XNOR" gate 50 and an "AND" gate 60.

The multiplexer 40 comprises a first input 41, a second input 42 and a switch
10 output 43. The multiplexer 40 is arranged to receive two clock signals, CLK A and CLK B, typically of different frequencies, via the two inputs 41,42. In this example, CLK A is of a higher frequency than CLK B. Each clock signal, CLK A and CLK B, may be provided using a crystal oscillator (not shown) to generate the required continuous clock frequency. The multiplexer 40 further comprises a
15 control input 44 which selectively connects the switch output 43 either to the first input 41 or to the second input 42 of the multiplexer 40, and thus one of the two clock frequencies, CLK A or CLK B will be output by the switch output 43.

A first data input 21 of the first flip-flop 20 is arranged to receive a clock select
20 signal, CLK SEL, having a logic level which serves as an indication to select which of the two clock signals, CLK A and CLK B, is output by the clock switching circuit 10. Depending on the application, a processor or a controller chip (not shown) may be used to generate the CLK SEL signal and the required logic level. The first flip-flop 20 also has a clock input (CLK) 22 which is used to

latch the clock select signal, CLK SEL, to a data output 23 of the first flip-flop 20. The CLK input 22 is coupled to the output of the clock switching circuit 10 provided by an output 63 of the AND gate 60.

- 5 The first flip-flop 20 further comprises a data output 23 which is coupled to a first data input 31 of the second flip-flop 30, a first input 51 of the XNOR gate 50 and the control input 44 of the multiplexer 40.

The second flip-flop 30 further comprises a clock input (CLK) 32 and a data
10 output 33. The CLK input 32 is coupled to the switch output 43 of the multiplexer 40 so that the clock signal, CLK A or CLK B, is used to latch the first input 31 of the second flip-flop 30 to its output 33, in accordance with a falling edge of the selected clock signal, CLK A or CLK B.

- 15 In this example, both the clock inputs 22,32 of the first and second flip-flops 20,30 are negative-edge triggered.

The data output 33 of the second flip-flop 30 is subsequently coupled to a second input 52 of the XNOR gate 50. The output 53 of the XNOR gate 50 is
20 logically "ANDed" with the switch output 43 of the multiplexer 40 by the AND gate 60 to produce the output 63, CLK OUT, of the clock switching circuit 10.

Preferably, each flip-flop 20,30 further comprises a reset input 24,34, RESET_N, which when RESET_N is "active" (logic "low" in this case), the CLK

OUT signal 63 would be defaulted to output one of the two clock signals, CLK A or CLK B.

The operation of the clock switching circuit 10 will now be described by reference to Figure 2, which illustrates timing waveforms of the signals RESET_N, CLK SEL, CLK A, CLK B and CLK OUT.

Assuming at state 0, the RESET_N signal 24,34 of the flip-flops 20,30 is pulled low to "reset" the clock switching circuit 10. During this period, the status of the clock select signal, CLK SEL, has no effect on the first flip-flop 20. With the RESET_N at "low", the outputs 23,33 of the flip-flops 20,30 would be a "low" and thus the output 53 of the XNOR gate 50 would be "high". Correspondingly, the second input 62 of the AND gate 60 is a "high" and thus the output 63 of the AND gate 60 would be dependent on its first input 61, which is coupled to the switch output 43 of the multiplexer 40.

In this embodiment, with the control input 44 of the multiplexer 40 a "low", corresponding to the output 23 of the first flip-flop 20, the switch output 43 of the multiplexer 40 is defaulted to output the first clock signal CLK A.

The output 63 of the AND gate 60 is coupled to the CLK input 22 of the first flip-flop 20 and is used to latch the first data input 21 to the data output 23 of the first flip-flop 20. Similarly, the switch output 43 of the multiplexer 40 is used to "clock" the CLK input 32 of the second flip-flop 30 so that the first data input 31

is latched out of the second flip-flop 30 in accordance with a falling edge of the CLK input 32.

At state 1, RESET_N is set to "high" and thus the outputs 23,33 of the flip-flops 20,30 would now be dependent on their respective first data inputs 21,31. In this case, at state 1, the clock select signal CLK SEL is set to "low" and with each "high-low" transition of the CLK input 22 (being negative-edge triggered), the state of the CLK SEL signal is latched to the data output 23 of the first flip-flop 20.

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Correspondingly, the control input 44 of the multiplexer 40 is "low" and thus the multiplexer's output 43 is switched to output CLK A as before. The output 53 of the XNOR gate 50, which depends on the outputs 23,33 of the two flip-flops 20,30 would still be a "high". Thus, the CLK OUT signal 63 of the clock switching circuit 10 would still be generating the clock signal CLK A.

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The clock switching circuit 10 continues outputting CLK A until the CLK SEL signal changes state, which is an indication to switch clock signals from CLK A to CLK B, for example during state 2 in Figure 2.

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During this state, the CLK SEL signal is pulled "high" by, for example a processor. The output 63 of the clock switching circuit 10 does not change immediately due to the design of the circuit 10 to minimise or eliminate glitch.

The switching of the CLK SEL signal is only registered at the next falling edge of the CLK input 22 of the first flip-flop 20. When this happens, as shown by the arrow X, the CLK SEL signal will be latched to the output 23 of the first flip-flop 20 and used to control the multiplexer 40, the second flip-flop 30 and the XNOR gate 50.

With the control input 44 a "high", the switch output 43 of the multiplexer 40 outputs CLK B to the first input 61 of the AND gate 60 and to the CLK input 32 of the second flip-flop 30. With this change, on the next falling edge of CLK B, a "high" state of the CLK SEL signal would be latched to the second flip-flop's data output 33. Therefore, the start of the CLK SEL signal at the data output 33 of the second flip-flop 30 would be synchronised to a falling edge of the CLK B signal being output by the switch output 43. This is shown using an arrow Y in Figure 2.

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It should also be apparent to a skilled reader that there is a latency between when the data output 23 of the first flip-flop 20 and when the data output 33 of the second flip-flop 30 outputs a "high", since at this point, the first flip-flop 20 is synchronised to the CLK A signal whereas the second flip-flop 30 is synchronised to the CLK B signal. During this period of latency, the first input 51 of the XNOR gate 50 is a "high" but the second input 52 is still a "low". Therefore, the output 53 of the XNOR gate 50 would be a "low" which means that the output 63 of the AND gate 60 is also a "low", as illustrated using arrow Z in Figure 2. This "low" state is an intermediate state of the clock switching

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circuit 10 before the output 63 of the AND gate 60 switches to the new clock signal CLK B. The presence of this intermediate state eliminates or prevents glitches from occurring when the output 63 of the AND gate 60 switches to the new clock signal CLK B.

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When the "high" state of the input 31 of the second flip-flop 30 is eventually latched to its data output 33, the output 53 of the XNOR gate 50 changes state to a "high" and the output 63 of the AND gate 60 switches from the intermediate state to CLK B such that the switching is synchronised to a falling edge of the
10 new clock signal, CLK B.

When the CLK_SEL signal goes back to "low", at state 3 of Figure 2, the data output 23 of the first flip-flop 20 changes state only at the next "high-low" transition as illustrated by arrow U. A similar latency, as represented by the
15 intermediate state, is observed for the output 63 of the clock switching circuit 10 to change but since CLK A is of a higher frequency than CLK B, the latency is shorter than when CLK SEL signal switches from "low" to "high". The transition from the intermediate state to the CLK A would be synchronised to a falling edge of the new clock signal, CLK A, as shown by an arrow W in Figure 2.

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In any case, the worst case latency would be one clock cycle of the clock signal at the CLK input 32 of the second flip-flop 30. In this case, this means that the worse case latency would be one clock cycle of the second clock signal, CLK B or the first clock signal, CLK A, as the case may be. With this arrangement, the

clock switching circuit 10 can switch between two clock signals minimising or without generating any glitch. In addition, this is achieved using a simpler circuit design.

- 5 The embodiment described is not to be construed as limitative. For example, although the described embodiment uses a "low" at CLK SEL to select CLK A and a "high" to select CLK B, the reverse can be used. In addition, other suitable types of flip-flops may be used in place of the D-type flip-flops.
- 10 Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the scope of the invention as claimed.

Claims

1. A clock switching circuit comprising
- 5 i) a switch having a first input arranged to receive a first clock signal, a second input arranged to receive a second clock signal, a control input, and a switch output, the control input selectively connecting the switch output to the said first clock signal or the said second clock signal;
- 10 ii) a first flip flop having a data input arranged to receive a clock select signal which provides an indication to switch from the first clock signal to the second clock signal, a clock input, and a data output;
- iii) a second flip flop having a first data input coupled to the data output of the first flip-flop, a clock input coupled to the switch output, and a data output,
- 15 iv) an XNOR logic gate having a first input coupled to the data output of the first flip-flop, a second input coupled to the data output of the second flip-flop, and an output; and
- v) an AND logic gate having a first input coupled to the output of the XNOR logic gate, a second input coupled to the switch output, and an output; the output of the AND gate arranged to provide the first clock
- 20 signal and is coupled to the clock input of the first flip flop;
- the arrangement being such that on detection of the said indication by the first flip-flop, the output of the AND gate switches from the first clock signal to an intermediate state and subsequently to the second clock signal; the switching from the intermediate state to the second clock
- 25 signal being synchronised to a falling edge of the second clock signal.

2. A clock switching circuit according to claim 1, wherein the first and/or second flip-flop is a D-type flip-flop.

5 3. A clock switching circuit according to claim 1 or claim 2, further comprising reset means.

4. A clock switching circuit according to claim 3, wherein the reset means is coupled to the first and the second flip-flops such that when a reset
10 signal is generated, the output of the AND gate is defaulted to output either the first or the second clock signals, independent of the clock select signal.

5. A clock switching circuit according to any one of the preceding claims,
15 wherein the switch is a multiplexer.

6. A clock switching circuit according to any one of the preceding claims, wherein the intermediate state is logic low.