

PATENT SPECIFICATION

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DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Electrical Voltage Divider Circuits.

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electrical voltage divider circuits, in general, and to electrical voltage divider circuits in particular for providing control voltages to amplifiers.

As used herein, the term "integrated circuit" refers to a unitary or monolithic semiconductor device or chip which is the equivalent of a network of interconnected active and passive circuit elements.

Various problems are presented in the design of such a semiconductor device. One problem is the cascading of resistance-capacitance coupled amplifiers. This is due to the fact that an integrated circuit capacitor occupies a large area of the semiconductor chip, even for a small amount of capacitance.

The physical dimensions of the chip are limited. Thus, the size of the capacitor and the amount of capacitance available for interstage coupling must also be limited. Restricting the size of the capacitor, however, limits not only the low frequency response of the amplifier, but the high frequency response as well. Therefore, the gain at the desired signal frequency is limited. The high frequency response of the amplifier will be limited still further because of the parasitic shunt capacitance existing across the integrated circuit capacitor structure.

With the limitations in the processing techniques presently used for fabricating inte-

grated circuit capacitors, these size restrictions may be a substantial source of trouble due to increased shorting between the plates of the capacitor. Consequently, it would be desirable to direct current (d.c.) couple amplifier stages in integrated circuit design wherever possible.

The cascading of d.c. coupled amplifier stages, however, offers problems of its own. For example, since the d.c. voltage appearing at the output electrode of one stage comprises the input voltage for the next succeeding stage, complicated biasing networks are generally needed to establish the desired operating points for each of the cascaded stages. D.C. feedback must also be provided for maintaining each operating point stable. Where substantial gain is to be provided in a single integrated circuit device, the phase shifts within the d.c. feedback loop may cause circuit instability. Both the amplifier stage itself and the manner in which its operating point is established and stabilized must be made substantially insensitive to variations in power supply voltages and environmental temperatures before d.c. coupled amplifier stages can be cascaded effectively.

Such an amplifier stage has been fully described in Patent Specification No. 1,127,801. Briefly, that stage includes: (a) a first and a second transistor connected as an emitter coupled amplifier, with the first transistor operating in the base-input, common collector mode and with the second transistor operating in the emitter-input, common base, collector-output mode; (b) a third transistor connected as an emitter follower and directly coupled to receive the signals developed at the collector electrode of the second transistor; and (c) a resistor connected in common to the emitter elec-

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SPECIFICATION AMENDED - SEE ATTACHED SLIP

trodes of the first and second transistors and substantially one-half the value of a load resistor connected to the collector electrode of the second transistor. More will be said about that amplifier stage in the following paragraphs of this specification.

Accordingly, it is an object of the present invention to provide a voltage divider circuit particularly for producing control voltages suitable for establishing and maintaining a stable operating point in the presence of supply voltage and temperature variations.

In accordance with the present invention a voltage divider circuit includes first and second terminals for connection to a source of energizing potential, a plurality of transistors $N+2$, each having an emitter electrode, a base electrode and a collector electrode, wherein N represents a positive integer of zero or more. First circuit means are provided coupled to the emitter, base and collector electrodes of a first transistor of the $N+2$ plurality for connecting the first transistor in a degenerated common emitter configuration. The first circuit means includes a first resistor connected between the collector electrode of the first transistor and said first terminal and a second resistor connected between the emitter electrode of the first transistor and said second terminal. The first resistor has a resistance value which is $N+1$ times the resistance value of the second resistor. Second circuit means are provided coupled to the emitter, base and collector electrodes of a second transistor of the $N+2$ plurality for connecting the second transistor in a common collector configuration. Coupling means are included having N transistors of the $N+2$ plurality for coupling the collector electrode of the first transistor to the base electrode of the second transistor, the emitter electrode of the second transistor being coupled to the base electrode of the first transistor, and output means coupled to the second transistor of the plurality for deriving an output voltage therefrom.

In the accompanying drawings:

Figure 1 is a schematic circuit diagram of an electrical circuit embodying the invention;

Figure 2 is a schematic circuit diagram showing a modification of the circuit of Figure 1; and

Figure 3 is a schematic circuit diagram of an amplifier stage, with control voltages being provided by a circuit embodying the invention.

Referring to the drawings and more particularly to Figure 1, the circuit there shown includes a pair of transistors 10 and 12. Transistor 10 is arranged in a degenerated common emitter type configuration, with its collector electrode connected to an energizing potential terminal 14 through a first

resistor 16 and its emitter electrode connected to a reference terminal 18 through a second resistor 20.

The other transistor 12 is arranged in a common collector type configuration, with its collector electrode directly connected to the energizing potential terminal 14 and its emitter electrode connected to the reference terminal 18 through a third resistor 22. The emitter electrode of transistor 12 is also connected to the base electrode of transistor 10 and to an output terminal 24 while the collector electrode of transistor 10 is additionally connected to the base electrode of transistor 12.

A load circuit 26 is connected between the output terminal 24 and the reference terminal 18. Potential terminal 14 and reference terminal 18 are adapted to be connected to a source of energizing potential of proper polarity (not shown). In the present example, resistor 16 is selected to be of substantially the same resistance value as resistor 20.

If the current drawn by the load 26 is sufficient to permit the proper V_{be} voltage drop to develop across the base-emitter junction of transistor 12, then resistor 22 may be omitted from the biasing circuit of Figure 1. As used herein, the term " V_{be} voltage" represents the average base-to-emitter voltage of a transistor which is operating as the active device in an amplifier circuit or the like. For silicon transistors, this V_{be} voltage may be approximately 0.7 volts, which is within the range of the proper V_{be} voltage for Class A amplification.

In the discussion that follows, it will be understood that the transistors 10 and 12 are each composed of the same semiconductor material, such as would be the case in monolithic silicon integrated circuits, so that their respective V_{be} voltages are equal.

In operation, i.e. with a proper polarity potential source connected between the terminals 14 and 18, the circuit of Figure 1 develops an output control voltage between the terminals 24 and 18 which is equal to one-half the value of the applied energizing potential. This can be seen from the following derivation:

At equilibrium, the output voltage (V_{out}) developed between the terminals 24 and 18 is equal to the applied energizing potential (V_{in}) minus the voltage drop across the resistor 16 (V_{R16}) and the V_{be} of the transistor 12, that is

$$V_{out} = V_{in} - V_{R16} - V_{be12} \quad (1)$$

The voltage drop across the resistor 20 (V_{R20}) at equilibrium is equal to the output voltage (V_{out}) developed between the terminals 24 and 18 minus the V_{be} of the transistor 10 or:

$$V_{R20} = V_{out} - V_{be10} \quad (2)$$

Since the resistors 16 and 20 are equal and since the same current flows through each, the voltage drop across the resistor 20 (V_{R20}) equals that across the resistor 16 (V_{R16}) and the expression (2) can be substituted for V_{R16} in equation (1), thusly:

$$V_{out} = V_{in} - V_{out} + V_{be10} - V_{be12} \quad (3)$$

With the V_{be} voltages of transistors 10 and 12 equal when those transistors are composed of the same semiconductor material, as was previously mentioned, the expression (3) reduces to:

$$V_{out} = \frac{V_{in}}{2} \quad (4)$$

illustrating that the control voltage delivered by the circuit to load 26 equals one-half that of the applied energizing potential.

Figure 2 shows a modified circuit embodying the present invention. Like the circuit of Figure 1, the circuit of Figure 2 also includes a first transistor arranged in a degenerated common emitter type configuration and a second transistor arranged in a common collector type configuration. Unlike that circuit, however, the circuit of Figure 2 uses transistor coupling to connect the output electrode of the first transistor to the input electrode of the second transistor, rather than the direct coupling used in Figure 1.

Referring to Figure 2, the circuit there shown includes, for example, six transistors 30, 32, 34, 36, 38 and 40. One transistor 30 is arranged in the degenerated common emitter configuration, with its collector electrode connected to an energizing potential terminal 42 through a first resistor 44 and with its emitter electrode connected to a reference terminal 46 through a second resistor 48. Another transistor 32 is arranged

in a common collector configuration, with its collector electrode directly connected to the energizing potential terminal 42 and with its emitter electrode connected to the reference terminal 46 through a third resistor 50. The emitter electrode of transistor 32 is also connected to the base electrode of transistor 30 and to an output terminal 52, to which an appropriate load (not shown) may be connected.

The collector electrode of transistor 30 is additionally connected to the base electrode of transistor 32 through the transistors 34, 36, 38 and 40, which together with the transistor 32 effectively comprise a "Darlington" type common collector configuration. More particularly: the collector electrode of transistor 30 is connected to the base electrode of transistor 34, the emitter electrode of transistor 34 to the base electrode of transistor 36, the emitter electrode of transistor 36 to the base electrode of transistor 38, the emitter electrode of transistor 38 to the base electrode of transistor 40, the emitter electrode of transistor 40 to the base electrode of transistor 32 and the collector electrodes of transistors 34, 36, 38 and 40 to the energizing potential terminal 42.

With this mode of transistor coupling, the resistor 44 connected to the collector electrode of transistor 30 is selected to be of five times the resistance value of the resistor 48 connected to the emitter electrode of that transistor.

In operation, i.e. with a proper polarity potential source connected between the terminals 42 and 46, a point of equilibrium is reached at which the output voltage (V_{out}) developed between the output terminals 52 and 46 is equal to the applied energizing potential (V_{in}) minus the voltage drop across the resistor 44 (V_{R44}) and the V_{be} voltages of the transistors 32, 34, 36 and 40 or:

$$V_{out} = V_{in} - V_{R44} - V_{be32} - V_{be34} - V_{be36} - V_{be38} - V_{be40} \quad (5)$$

The voltage drop across the resistor 48 (V_{R48}) at equilibrium is equal to the output voltage (V_{out}) developed between the terminals 52 and 46 minus the V_{be} of the transistor 30 or:

$$V_{R48} = V_{out} - V_{be30} \quad (6)$$

Since resistor 44 is selected to be five times the value of resistor 48 and since the same current flows through each, the voltage drop across the resistor 44 is five times that across the resistor 48 and the equation (6) can be multiplied by five and substituted for V_{R44} in equation (5) thusly:

$$V_{out} = V_{in} - 5V_{out} + 5V_{be30} - V_{be32} - V_{be34} - V_{be36} - V_{be38} - V_{be40} \quad (7)$$

Assuming that the transistors 30, 32, 34, 36, 38 and 40 are each composed of the same semiconductor material, such as would be the case in monolithic silicon integrated circuits, then their respective V_{be} voltages are all equal and the expression (7) reduces to:

$$V_{out} = \frac{V_{in}}{6} \quad (8)$$

Expression (8) thus illustrates that the control voltage delivered by the circuit of Figure 105

2 to a load (not shown) connected to its output terminal 52 equals one-sixth that of the applied energizing potential.

Other integral fractions of the applied energizing potential can be developed as output control voltages by changing the transistor coupling between the degenerated common emitter stage and the output common collector stage and by changing the ratio of the resistors in the degenerated common emitter stage accordingly. To be more specific, with N representing the number of stages of transistor coupling between the stages 30 and 32, output voltages equal to

$\frac{1}{N+2}$ times the applied energizing potential

can be developed simply by selecting the collector resistor in the degenerated common emitter stage to be N+1 times the value of the emitter resistor of that stage. A one-third fraction therefore requires one stage of transistor coupling and a 2:1 resistance ratio, a one-fourth fraction requires two stages of transistor coupling and a 3:1 resistance ratio, etc.

Throughout the foregoing derivation, the output voltage of the circuit of Figure 2 was considered as being developed between the terminals 52 and 46. If the output voltage is considered as being developed between terminals 52 and 42, instead, analysis will show that the output voltage can be expressed as

$\frac{N+1}{N+2}$ times the applied energizing potential.

Thus, in the arrangement of Figure 2, where N equals 4, the voltage developed at output terminal 52 with respect to that at terminal 42 is given by:

$$V_{out} = \frac{5V_{in}}{6} \quad (9)$$

It will be appreciated by one skilled in the art that these general $\frac{1}{N+2}$ and $\frac{N+1}{N+2}$ expressions for output voltage apply equally as well to the circuit of Figure 1, which represents the particular case of N equal to zero.

Figure 3 shows how the circuit of Figure 1 provides control voltages to establish and maintain the operating point of the semiconductor amplifier circuit described in Patent Specification No. 1,127,801. In the discussion that follows, it will be understood that both the circuit and the amplifier are formed on a single semiconductor body and comprise at least a portion of an integrated circuit chip. Those numerals used to designate the various components of the biasing circuit in Figure 1 are used to identify similar

components in Figure 3. Reference terminal 18 has, in addition, been connected to ground.

The amplifier circuit portion of Figure 3 includes three transistors 60, 62 and 64. One transistor 60 is arranged in a common collector type configuration, with its collector electrode directly connected to the energizing potential terminal 14 and with its emitter electrode connected to ground through a resistor 66. A second transistor 62 is arranged in a common base type configuration, with its collector electrode connected to the potential terminal 14 through a resistor 68 and with its emitter electrode connected to ground through the resistor 66.

A third transistor 64 is arranged in a common collector type configuration, with its collector electrode directly connected to the terminal 14 and with its emitter electrode connected to ground through a resistor 70. The base electrode of transistor 60 is connected via a conductor 72 to an input terminal 74 while the base electrode of transistor 62 is by-passed to ground at signal frequencies by a capacitor 76. The capacitor 76 is not ordinarily a part of the integrated circuit chip.

The collector electrode of transistor 62 is connected to the base electrode of transistor 64, the emitter electrode of which is connected via a conductor 78 to an output terminal 80 to which an appropriate load (not shown) may be connected. In accordance with the principles set forth in Patent Specification No. 1,127,801, resistor 68 is selected to be twice the value of resistor 66 so as to stabilize the amplifier circuit against power supply variations and temperature changes.

The amplifier circuit so described essentially comprises an emitter coupled amplifier stage driving a common collector stage. That is, with a proper polarity potential source connected between terminal 14 and ground, signals supplied to input terminal 74 are amplified first by the combination of transistors 60 and 62 and then by the transistor 64. Amplified signals are developed across the common collector stage resistor 70 and appear at the output terminal 80. Symmetrical amplifier operation is obtained by coupling the output voltage developed at terminal 24 of the circuit including transistors 10 and 12 to the base electrodes of transistors 60 and 62 through equal value resistors 82 and 84, respectively.

That the circuit incorporating the principles of the present invention stabilizes the operating point of the amplifier circuit in the presence of supply voltage variations and temperature changes can be seen from the following discussion. Assume first a variation in the magnitude of the energizing

potential applied between terminal 14 and ground. If the bias control voltage applied to the base electrodes of the transistors 60 and 62 were maintained constant during the energizing potential variation, the d.c. output voltage at the collector electrode of transistor 62 would change accordingly because the current through transistor 62 would remain constant.

Thus, if the voltage at the terminal 14 drops by an amount Δe (becomes less positive), then the output voltage at the collector electrode of transistor 62 would drop a like amount. The bias voltage applied to the base electrode of transistor 62 does not remain constant, however, but drops (becomes less positive) by an amount $\frac{\Delta e}{2}$. This follows since,

as the above equations (1)–(4) show, the voltage delivered by the biasing circuit at its output terminal 24 remains at one-half the value of the applied energizing potential.

As a result, the emitter current of transistor 62 falls by $\frac{\Delta e}{2R_{e6}}$, and its collector

voltage rises by $\frac{\Delta e R_{e8}}{2R_{e6}}$. The net change in

voltage at the collector electrode of transistor 62 is, therefore, $\Delta e - \frac{\Delta e R_{e8}}{2R_{e6}}$, which also

represents the net change at the emitter electrode of transistor 64. Since resistor 68 is selected to be of twice the resistance value of resistor 66, the net change in voltage at the emitter electrode of the transistor 64 is zero. It will be understood that in this paragraph and in the paragraphs that follow R_{e6} and R_{e8} represent the resistance values of resistors 66 and 68, respectively.

A similar analysis will show that the net change in voltage at the emitter electrode of the transistor 64 will also be zero if the voltage at the terminal 14 increases. In other words, for either case, the change in voltage at the collector electrode of transistor 62 with changing energizing potential will be compensated by a corresponding change in the bias voltage applied to the base electrode of that transistor. Symmetrical amplifier operation continues to be maintained by applying the same bias control voltage change to the base electrode of transistor 60.

Consider, next, the effects of temperature change. Temperature change tends to change the V_{be} voltage between the emitter and base electrodes of the transistors 10, 12, 60, 62 and 64. Since these five transistors are composed of the same semiconductor material when incorporated in a monolithic integrated circuit, however, temperature changes affect

their V_{be} voltages in equal amounts and in the same direction. As equations (3) and (4) show, the output control voltage developed by the circuit at terminal 24—and, therefore, the bias voltage applied to the base electrodes of transistors 60 and 62—remains substantially constant at one-half the potential applied between terminal 14 and ground and is independent of any temperature changes that might occur. Assume then that temperature changes cause a change in the V_{be} of transistors 60 and 62 by an amount ΔV_{be} and, as a result, a change in the current of those transistors by an amount Δi .

$$\text{Then } \Delta V_{be} = 2\Delta i R_{e6} \quad (10)$$

$$\text{rearranging } \Delta i = \frac{\Delta V_{be}}{2R_{e6}} \quad (11)$$

The change in the collector voltage of transistor 62 is therefore:

$$\Delta V_c = \Delta i R_{e8} \quad (12)$$

Substituting (11) into (12):

$$\Delta V_c = \frac{\Delta V_{be} R_{e8}}{2R_{e6}} \quad (13)$$

The change in voltage at the emitter electrode of transistor 64 is $\Delta V_c - \Delta V_{be}$ or:

$$\frac{\Delta V_{be} R_{e8}}{2R_{e6}} - \Delta V_{be} = \Delta V_{be} \left(\frac{R_{e8}}{2R_{e6}} - 1 \right) \quad (14)$$

Since $R_{e8} = 2R_{e6}$, the net change in voltage at the emitter electrode of transistor 64 is zero. Analysis of this derivation will show that the net change is zero for both temperature increases and temperature decreases.

An important fact to be noted is that the accuracy with which the output voltage of the circuits of Figures 1, 2 and 3 approximates

$\frac{1}{N+2}$ times the power supply voltage, on

the one hand, and $\frac{N+1}{N+2}$ times that supply

voltage, on the other hand—and, as a result, the stability and balance of bias controlled circuits—is primarily dependent upon the ratio of the collector and emitter resistors for the degenerated common emitter transistor rather than upon their absolute values. This is of special significance in integrated circuit fabrication since the two resistors can be formed at the same time and their ratios can be readily maintained whereas the absolute resistance values are a function of

the variables in the fabrication process. Accordingly, with a given process procedure, a higher yield of usable circuits can be expected where the ratios of the circuit components are more significant than the absolute values.

It should be noted that a conventional resistive type voltage divider cannot be substituted for the circuit incorporating the principles of this invention and yet give the performance characteristics described above. Considering the arrangement of Figure 1 as being illustrative, the output impedance of the circuit there shown is given by the expression:

$$Z_{out} = \frac{1}{2g_m} \quad (14)$$

where g_m represents the transconductance of the transistor 12. This impedance is of the order of 20 ohms, and to employ a resistive divider of such a low output impedance would result in a totally unacceptable current being drawn from the type of power supply normally intended for integrated circuit use.

WHAT WE CLAIM IS:—

1. An electrical voltage divider circuit including first and second terminals for connection to a source of energizing potential a plurality of transistors, $N+2$, each having an emitter electrode, a base electrode and a collector electrode, and wherein N represents a positive integer of zero or more, first circuit means coupled to the emitter, base and collector electrodes of a first transistor of said $N+2$ plurality for connecting said first transistor in a degenerated common emitter configuration, said first circuit means including a first resistor connected between the collector electrode of said first transistor and said first terminal and a second resistor connected between the emitter electrode of said first transistor and said second terminal, said first resistor having $N+1$ times the resistance value of said second resistor, second circuit means coupled to the emitter, base and collector electrodes of a second transistor of said $N+2$ plurality for connecting said second transistor in a common collector configuration; coupling means including N transistors of said $N+2$ plurality for coupling the collector electrode of said first transistor to the base electrode of said second transistor, the emitter electrode of said second transistor being coupled to the base electrode of said first transistor, and output means coupled to said second transistor of said plurality for deriving an output voltage therefrom.

2. An electrical circuit as claimed in Claim 1, characterized in that said out-

put means is coupled between the emitter electrode of said second transistor and the said second terminal for deriving an

output voltage equal to $\frac{1}{N+2}$ times the

voltage of said energizing potential source. 65

3. An electrical circuit as claimed in Claim 1, characterized in that said output means is coupled between the emitter electrode of said second transistor and said first terminal for deriving an output voltage equal

to $\frac{N+1}{N+2}$ times the voltage of said energizing potential source. 70

4. An electrical circuit as claimed in Claim 1, wherein said second resistor having the same resistance value as said first resistor, and including a direct current connection from the collector electrode of said second transistor to said first terminal, a third resistor connected between the emitter electrode of said second transistor and said second terminal, a direct current connection from the collector electrode of said first transistor to the base electrode of said second transistor, and a direct current connection from the emitter electrode of said second transistor to the base electrode of said first transistor. 75

5. An electrical circuit as claimed in Claim 1, wherein said coupling means includes said plurality of transistors N having their base-emitter junctions connected in series between the collector electrode of said first transistor and the base electrode of said second transistor, each transistor of said N plurality having an emitter electrode, a base electrode and a collector electrode, a direct current connection from the collector electrode of each transistor of said N plurality to said first terminal, a direct current connection from the collector electrode of said first transistor to the base electrode of a first transistor of said N plurality, a direct current connection from the base electrode of said second transistor to the emitter electrode of the last transistor of said N plurality, a direct current connection from the emitter electrode of each transistor of said N plurality to the base electrode of the next succeeding transistor of said N plurality within said serial connection; said first resistor being connected between the collector electrode of said first transistor and said first terminal, said second resistor being connected between the emitter electrode of said first transistor and said second terminal, a direct current connection from the collector electrode of said second transistor to said first terminal, a third resistor connected between the emitter electrode of said second transistor and said second terminal, said output means deriving an output voltage between the 80 85 90 95 100 105 110 115 120

the variables in the fabrication process. Accordingly, with a given process procedure, a higher yield of usable circuits can be expected where the ratios of the circuit components are more significant than the absolute values.

It should be noted that a conventional resistive type voltage divider cannot be substituted for the circuit incorporating the principles of this invention and yet give the performance characteristics described above. Considering the arrangement of Figure 1 as being illustrative, the output impedance of the circuit there shown is given by the expression:

$$Z_{out} = \frac{1}{2g_m} \quad (14)$$

where g_m represents the transconductance of the transistor 12. This impedance is of the order of 20 ohms, and to employ a resistive divider of such a low output impedance would result in a totally unacceptable current being drawn from the type of power supply normally intended for integrated circuit use.

WHAT WE CLAIM IS:—

1. An electrical voltage divider circuit including first and second terminals for connection to a source of energizing potential a plurality of transistors, $N+2$, each having an emitter electrode, a base electrode and a collector electrode, and wherein N represents a positive integer of zero or more, first circuit means coupled to the emitter, base and collector electrodes of a first transistor of said $N+2$ plurality for connecting said first transistor in a degenerated common emitter configuration, said first circuit means including a first resistor connected between the collector electrode of said first transistor and said first terminal and a second resistor connected between the emitter electrode of said first transistor and said second terminal, said first resistor having $N+1$ times the resistance value of said second resistor, second circuit means coupled to the emitter, base and collector electrodes of a second transistor of said $N+2$ plurality for connecting said second transistor in a common collector configuration; coupling means including N transistors of said $N+2$ plurality for coupling the collector electrode of said first transistor to the base electrode of said second transistor, the emitter electrode of said second transistor being coupled to the base electrode of said first transistor, and output means coupled to said second transistor of said plurality for deriving an output voltage therefrom.

2. An electrical circuit as claimed in Claim 1, characterized in that said out-

put means is coupled between the emitter electrode of said second transistor and the said second terminal for deriving an

output voltage equal to $\frac{1}{N+2}$ times the

voltage of said energizing potential source.

3. An electrical circuit as claimed in Claim 1, characterized in that said output means is coupled between the emitter electrode of said second transistor and said first terminal for deriving an output voltage equal to $\frac{1}{N+1}$ times the voltage of said energizing

potential source.

4. An electrical circuit as claimed in Claim 1, wherein said second resistor having the same resistance value as said first resistor, and including a direct current connection from the collector electrode of said second transistor to said first terminal, a third resistor connected between the emitter electrode of said second transistor and said second terminal, a direct current connection from the collector electrode of said first transistor to the base electrode of said second transistor, and a direct current connection from the emitter electrode of said second transistor to the base electrode of said first transistor.

5. An electrical circuit as claimed in Claim 1, wherein said coupling means includes said plurality of transistors N having their base-emitter junctions connected in series between the collector electrode of said first transistor and the base electrode of said second transistor, each transistor of said N plurality having an emitter electrode, a base electrode and a collector electrode, a direct current connection from the collector electrode of each transistor of said N plurality to said first terminal, a direct current connection from the collector electrode of said first transistor to the base electrode of a first transistor of said N plurality, a direct current connection from the base electrode of said second transistor to the emitter electrode of the last transistor of said N plurality, a direct current connection from the emitter electrode of each transistor of said N plurality to the base electrode of the next succeeding transistor of said N plurality within said serial connection; said first resistor being connected between the collector electrode of said first transistor and said first terminal, said second resistor being connected between the emitter electrode of said first transistor and said second terminal, a direct current connection from the collector electrode of said second transistor to said first terminal, a third resistor connected between the emitter electrode of said second transistor and said second terminal, said output means deriving an output voltage between the





emitter electrode of said second transistor
and said 'second' terminal equal to $\frac{1}{N+2}$
times the voltage of said energizing potential
source.

6. An electrical circuit as defined in
Claim 5 wherein $N=4$.

7. An electrical circuit for providing control
voltages to establish and maintain a
selected operating point of a semiconductor
amplifier characterized by first and second
transistors, each having an emitter electrode,
a base electrode and a collector electrode,
first and second terminals for the connection
of a source of energizing potential, a first
resistor connected between the collector electrode
of said first transistor and said first
terminal, a second resistor connected between
the emitter electrode of said first transistor
and said second terminal, and being of substantially
the same resistance value as said first resistor,
a direct current connection from the collector
electrode of said second transistor to said first
terminal, a third resistor connected between the
emitter electrode of said second transistor
and said second terminal, a direct current
connection from the collector electrode of
said first transistor to the base electrode of
said second transistor, a direct current
connection from the emitter electrode of said
second transistor to the base electrode of
said first transistor, and output means for
deriving an output voltage at low impedance
equal to one-half the voltage of said energizing
potential source between the emitter
electrode of said second transistor and said
second terminal to establish and maintain
said semiconductor amplifier at said operating
point.

8. An electrical circuit as defined in
Claim 7 wherein the output impedance
exhibited at the emitter electrode of said
second transistor is given by the expression

$$Z_{out} = \frac{1}{2g_m}$$

in which g_m represents the transconductance
of said second transistor.

9. An electrical circuit characterized by
an integrated circuit amplifier configuration
of the type including: (a) an input transistor
having a collector electrode directly connected
to a first energizing potential terminal, an emitter
electrode connected to a second energizing
potential terminal by means of a coupling resistor
and a base electrode directly connected to a source
of input signals to be amplified; (b) an intermediate
transistor having a collector electrode

connected to said first terminal by means of a load resistor of substantially twice
the resistance value of said coupling resistor,
an emitter electrode connected to said second
terminal by means of said coupling resistor
and a base electrode; and (c) an output transistor
having a collector electrode directly
connected to said first terminal, an emitter
electrode connected to said second terminal
by means of an output resistor and a base
electrode directly connected to the collector
electrode of said intermediate transistor; first
and second transistors incorporated as part
of said integrated circuit amplifier configuration,
each having an emitter electrode, a base
electrode and a collector electrode, a first
resistor connected between the collector electrode
of said first transistor and said first
terminal, a second resistor connected between
the emitter electrode of said first transistor
and said second terminal, and being substantially
of the same resistance value as said first resistor,
a direct current connection from the collector
electrode of said second transistor to said first
terminal, a third resistor connected between the
emitter electrode of said second transistor
and said second terminal, a direct current
connection from the collector electrode of
said first transistor to the base electrode of
said second transistor, a direct current
connection from the emitter electrode of said
second transistor to the base electrode of
said first transistor, output means for deriving
an output voltage equal to one-half the
voltage of a source of energizing potential
coupled across said first and said second
terminals, said output voltage being derived at
low impedances between the emitter electrode
of said second transistor and said second
terminal; and means including fourth and fifth
resistors of substantially equal resistance value
for coupling said output voltage to the base
electrodes of said input and intermediate
transistors to bias said amplifier configuration
at said operating point.

10. An electrical voltage divider circuit as
defined in any one of Claims 1—8, characterized
in that all of said transistors and resistors
are arranged on a single monolithic semiconductor
device.

11. An electrical voltage divider circuit
substantially as described and illustrated with
respect to Figure 1.

12. An electrical voltage divider circuit
substantially as described and illustrated with
respect to Figure 2.

13. An integrated circuit amplifier and
voltage divider circuit substantially as described
and illustrated with respect to Figure 3.

A. A. THORNTON & CO.