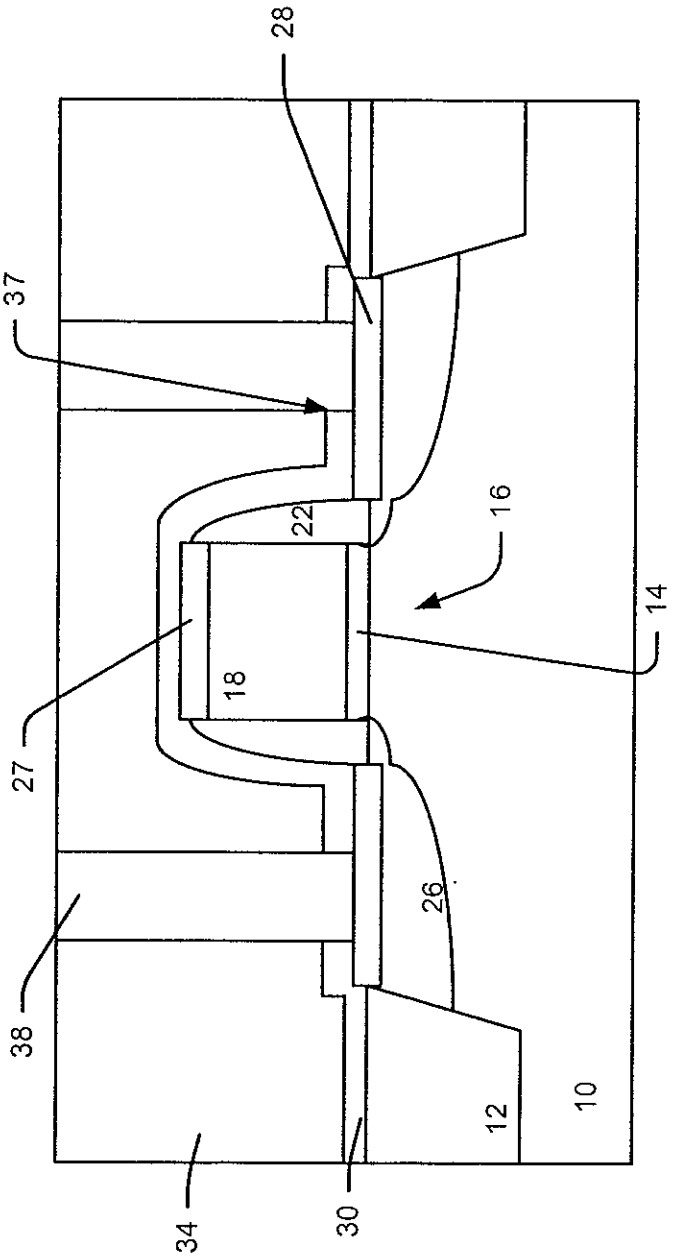


FIGURE 1

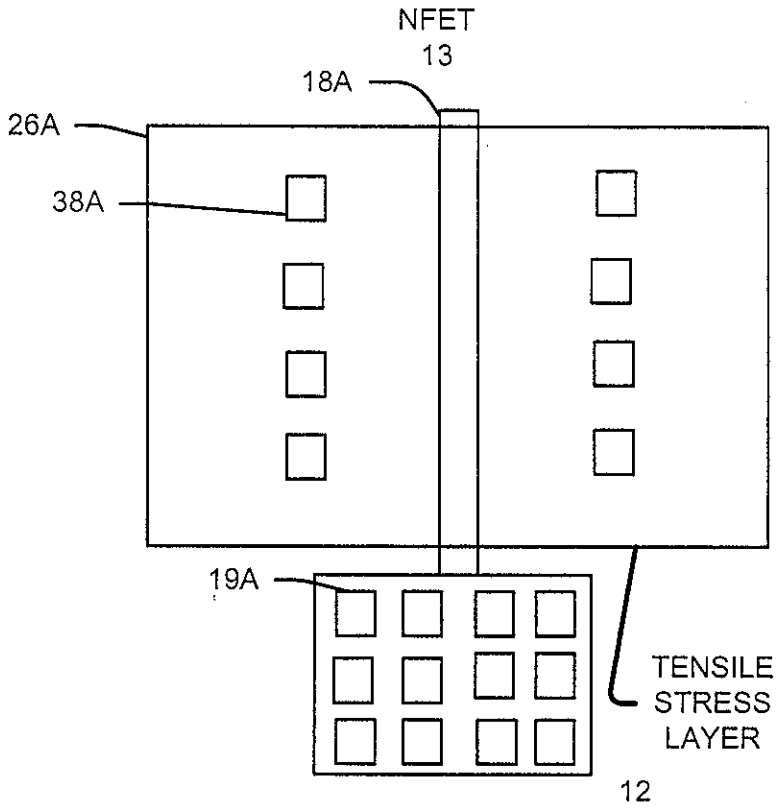


FIGURE 2A

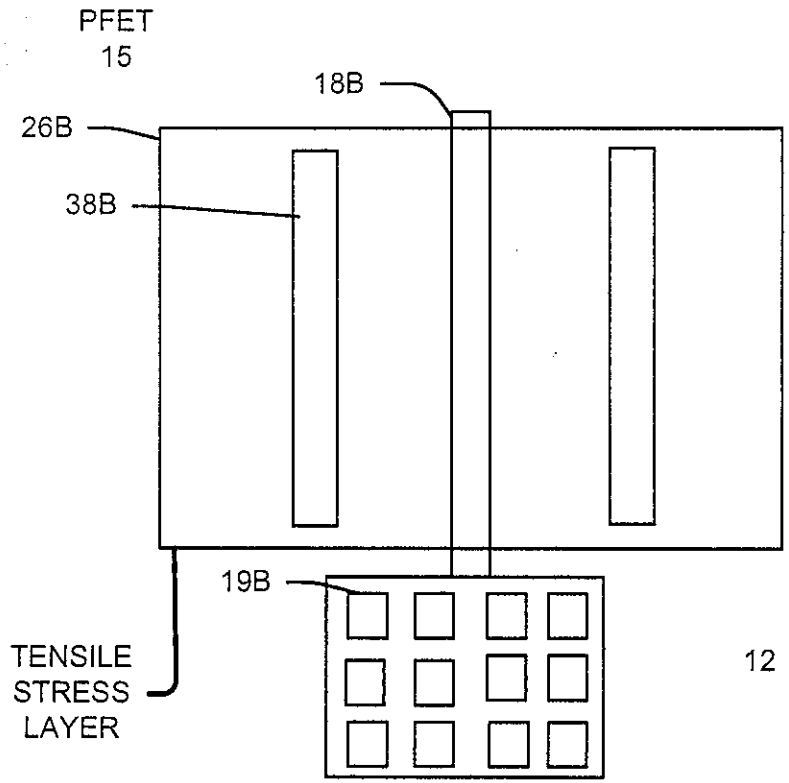


FIGURE 2B

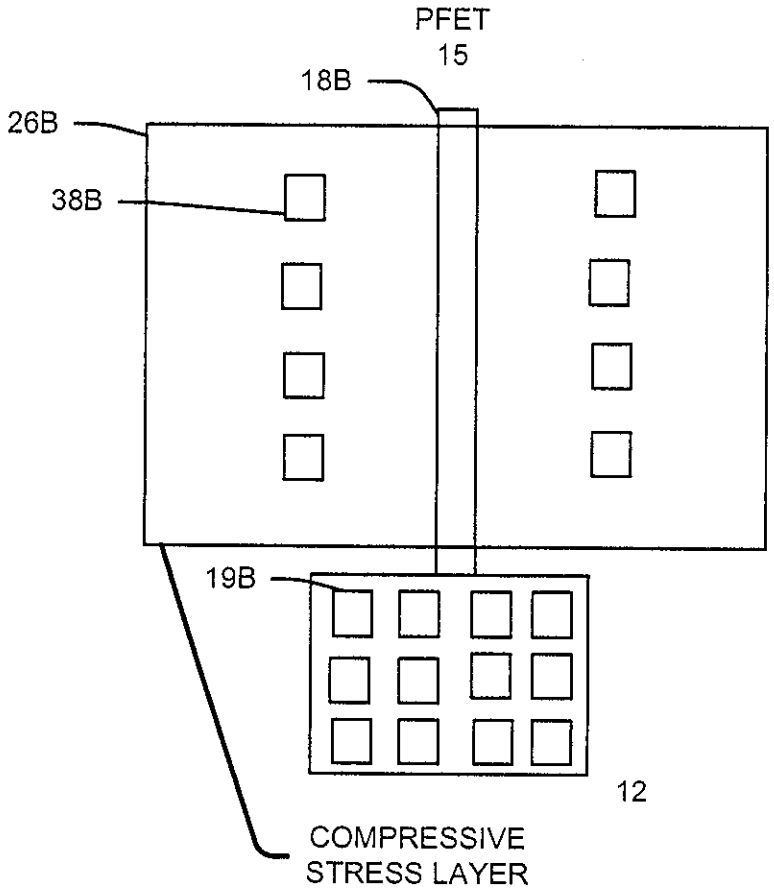
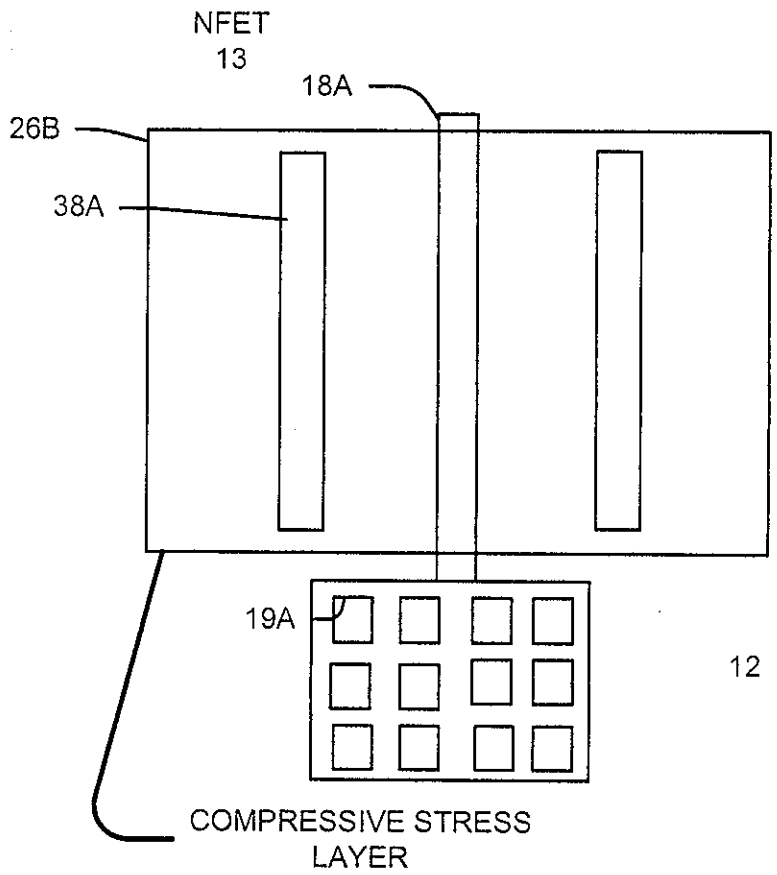


FIGURE 3A



Larger NFET contact hole(s) area to Reduce compressive stress on NFET

FIGURE 3B

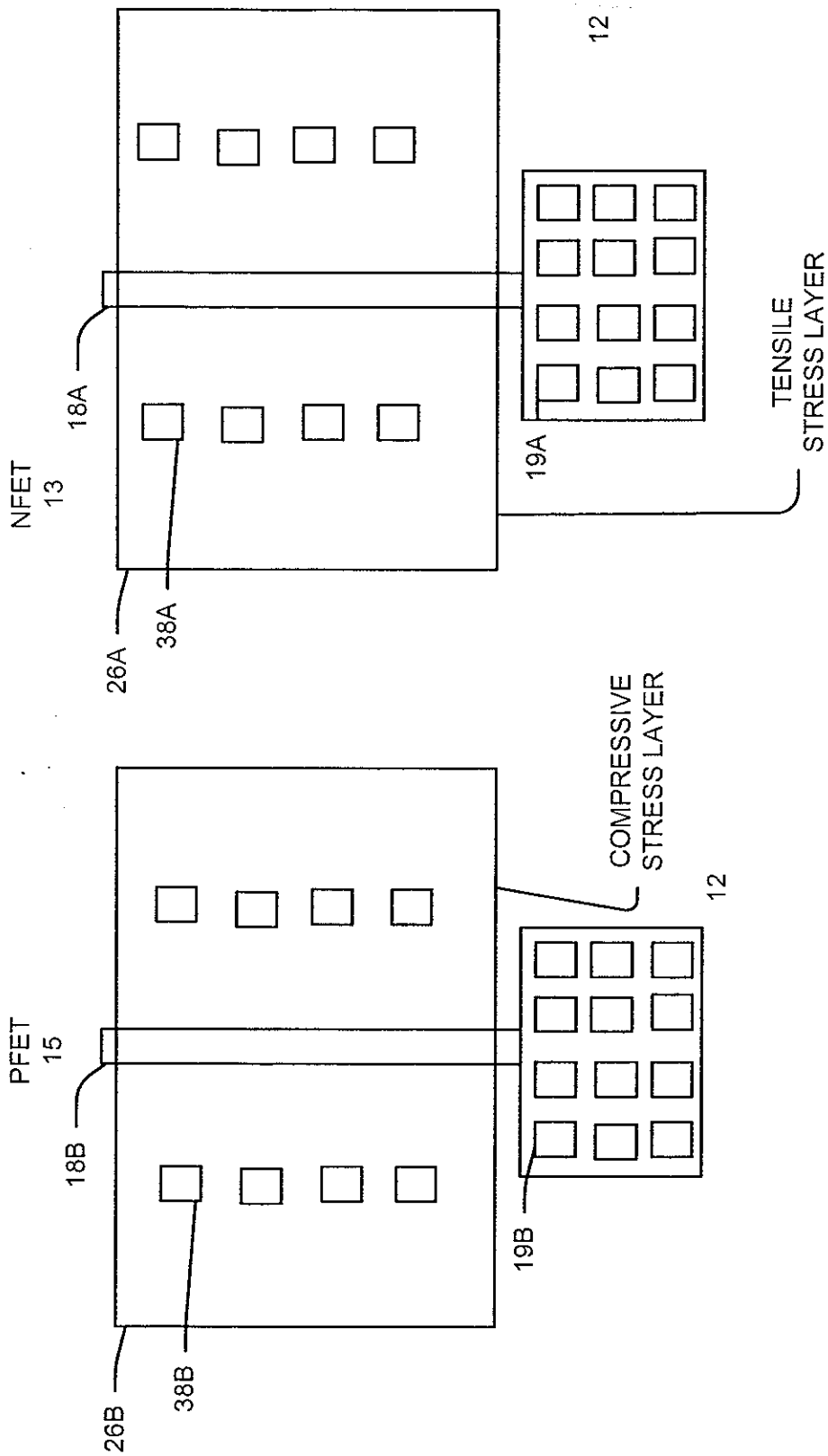
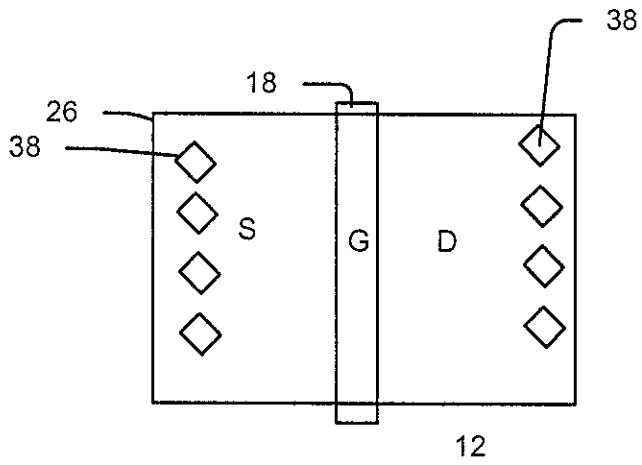


FIGURE 4A

FIGURE 4B



SMALL CONTACT AND FAR
AWAY FROM GATE

FIGURE 5A

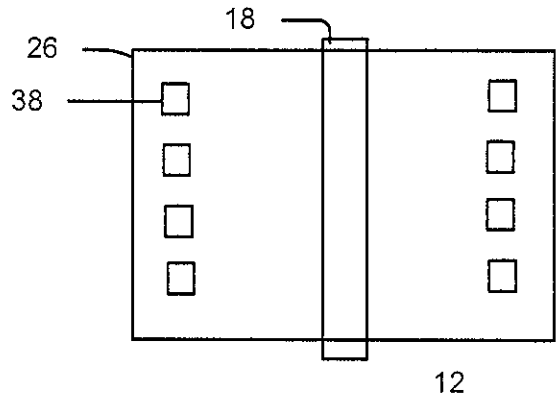


FIGURE 5B

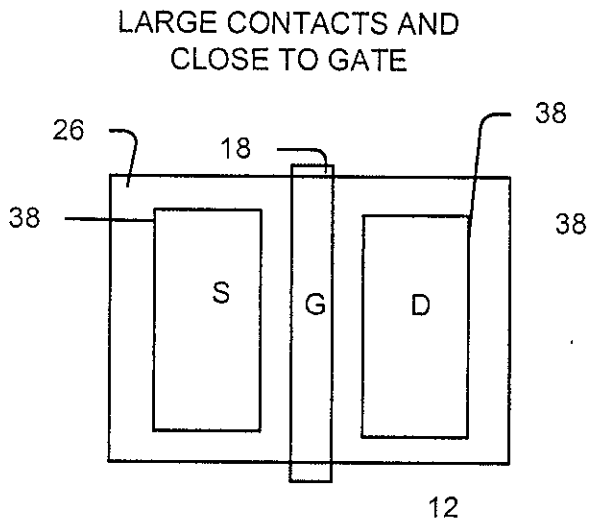


FIGURE 6A

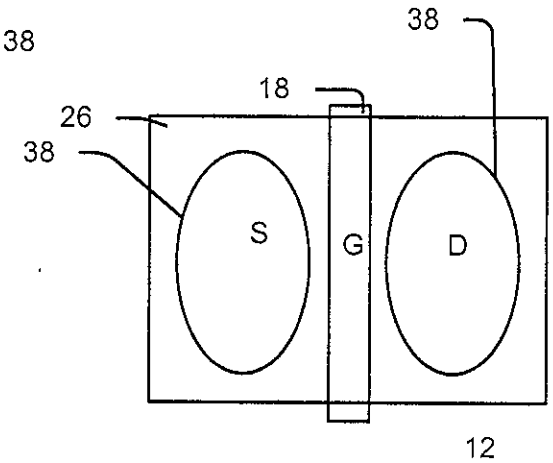


FIGURE 6B

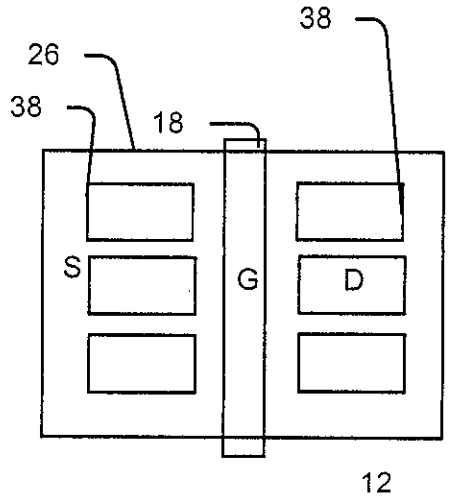


FIGURE 6C

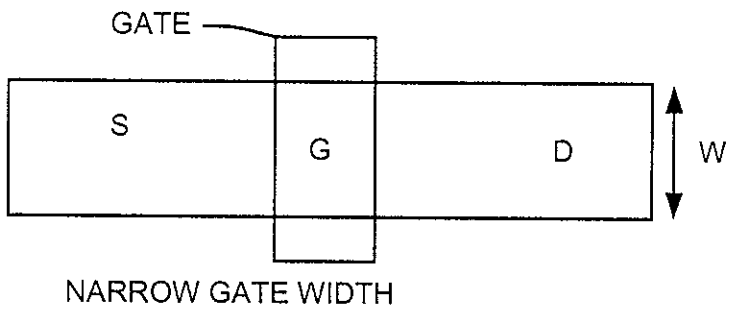


FIGURE 7A

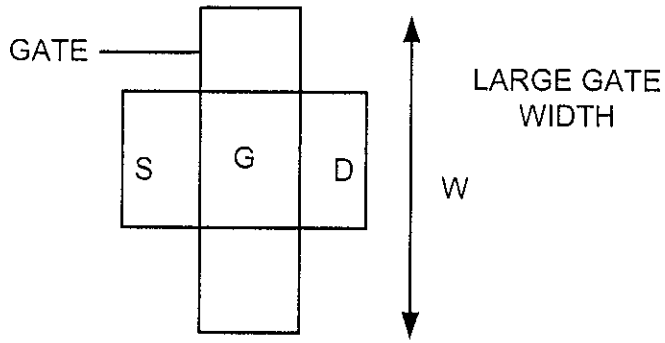


FIGURE 7B

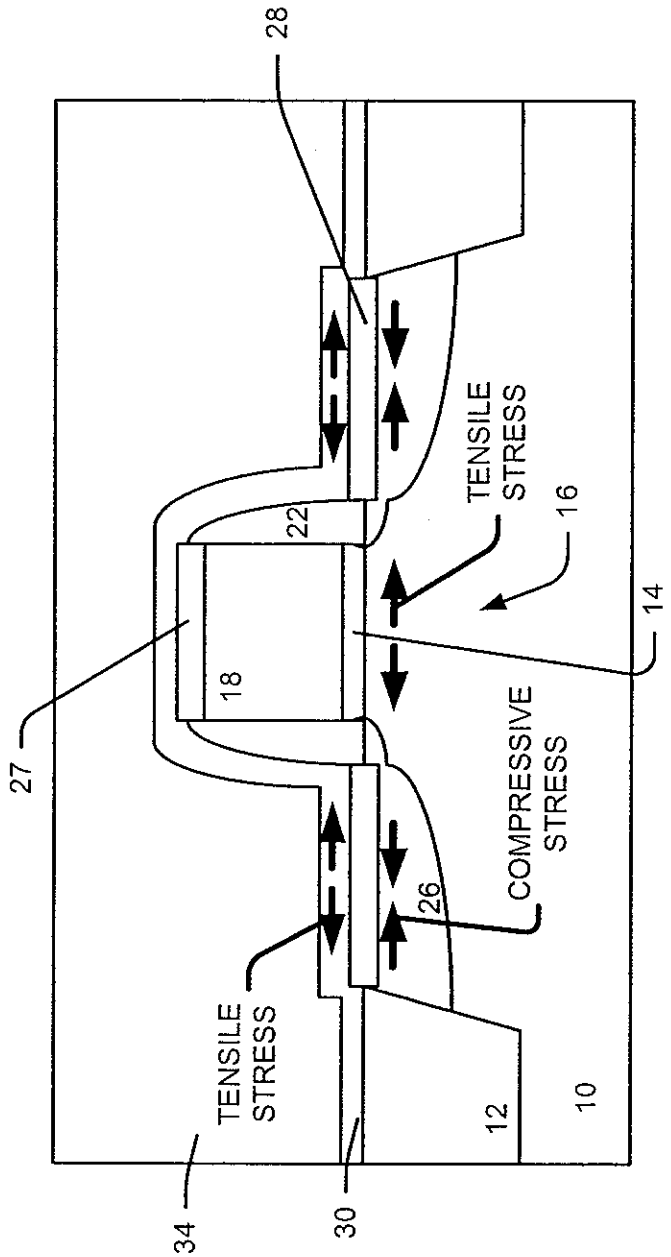

28
TENSILE
STRESS
16
22
14
18
27
COMPRESSIVE
STRESS
26
TENSILE
STRESS
12
10
34
30

FIGURE 8