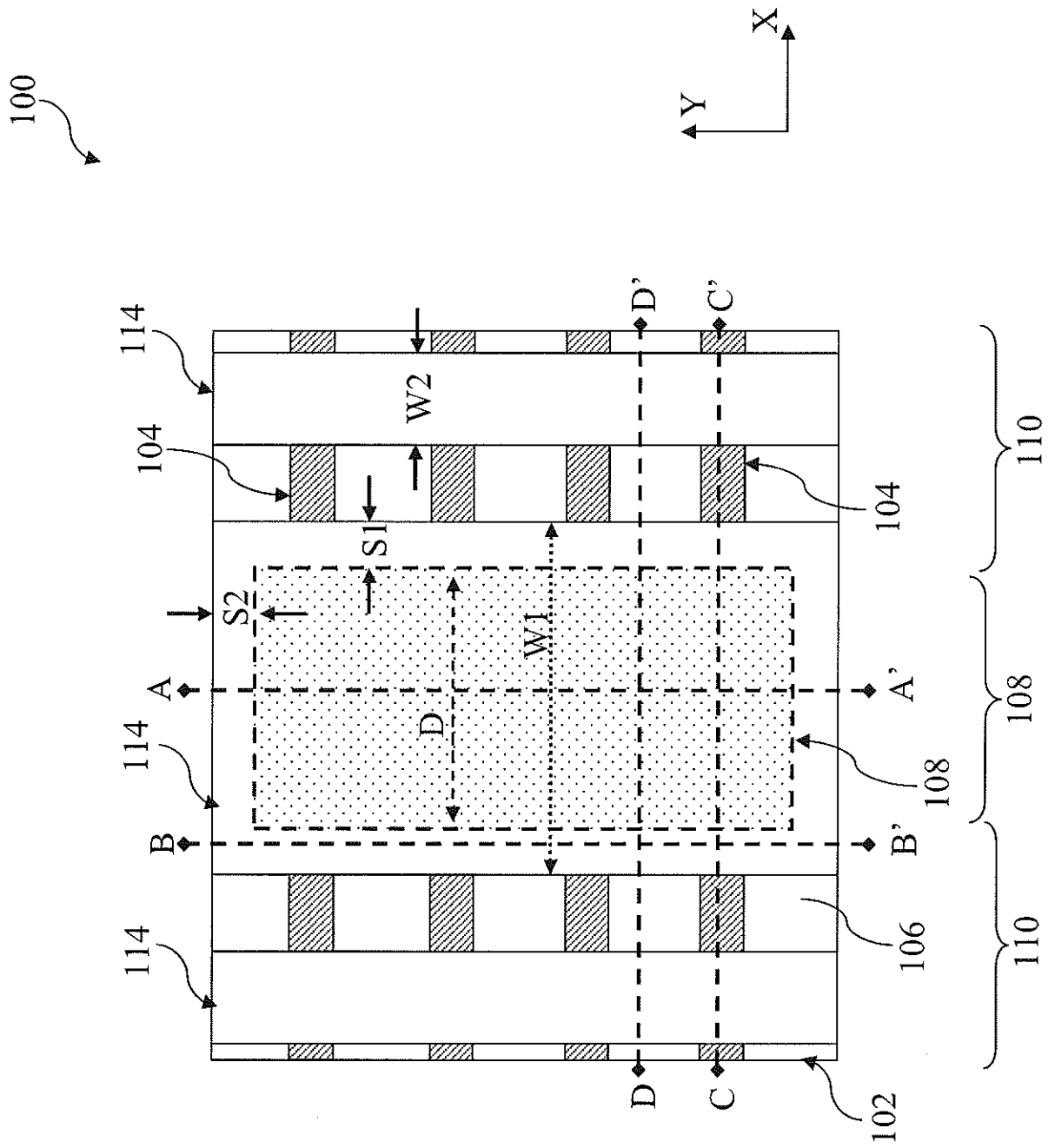


Fig. 1

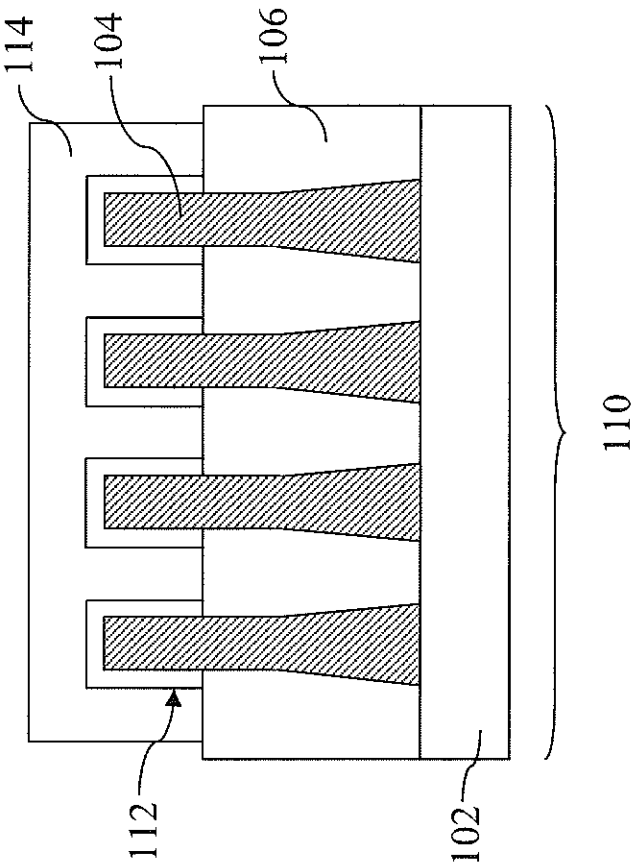


Fig. 3

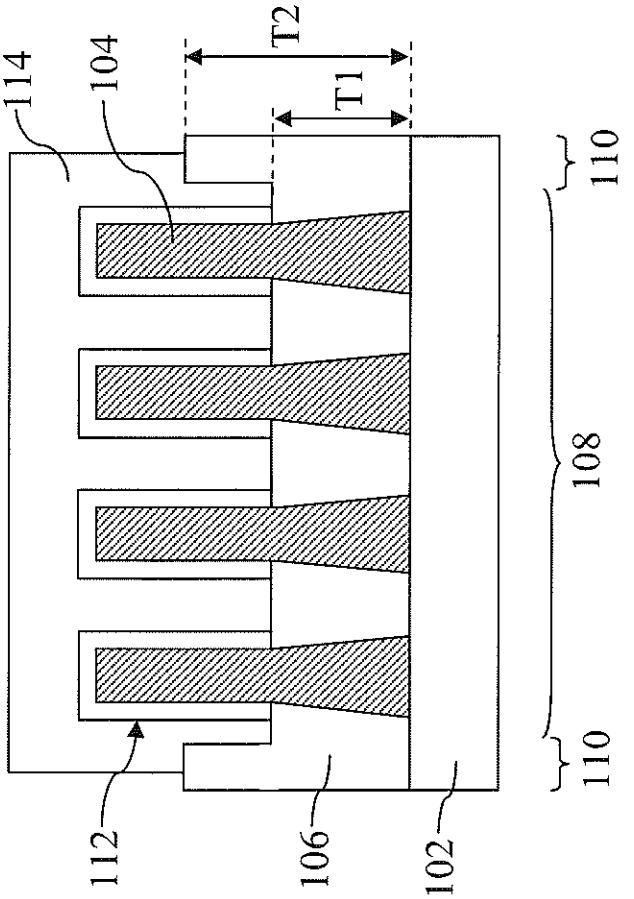


Fig. 2

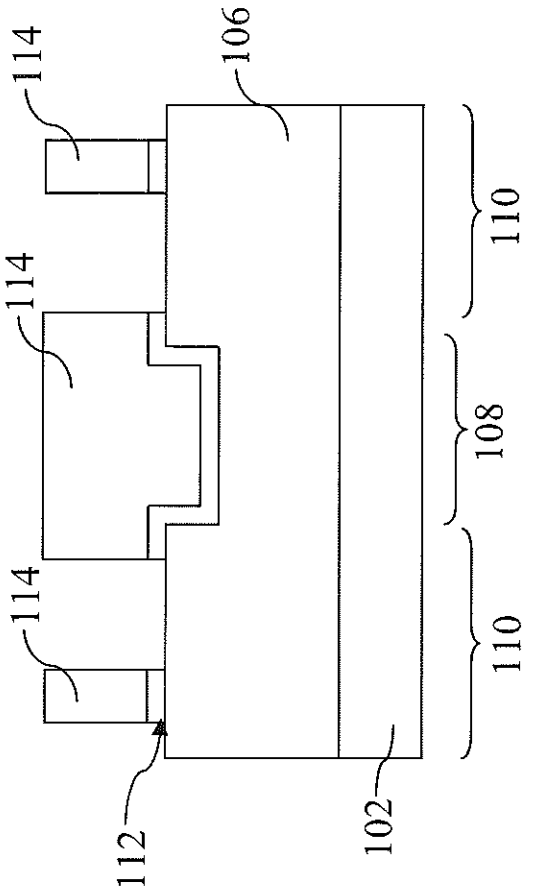


Fig. 5

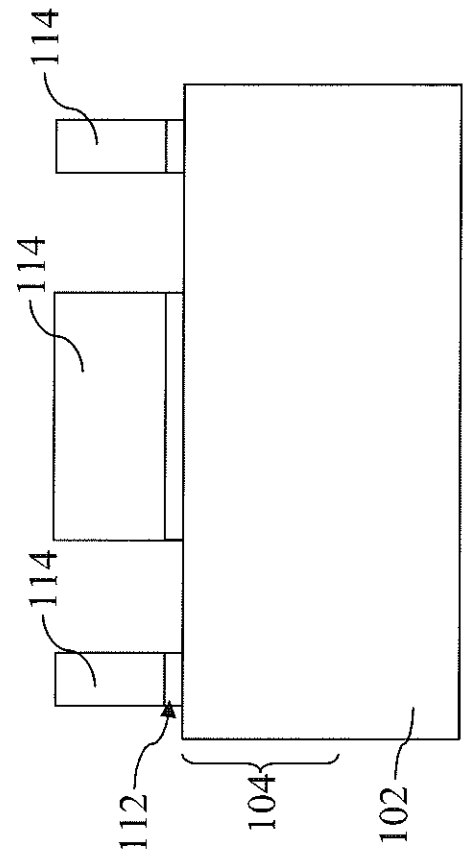


Fig. 4

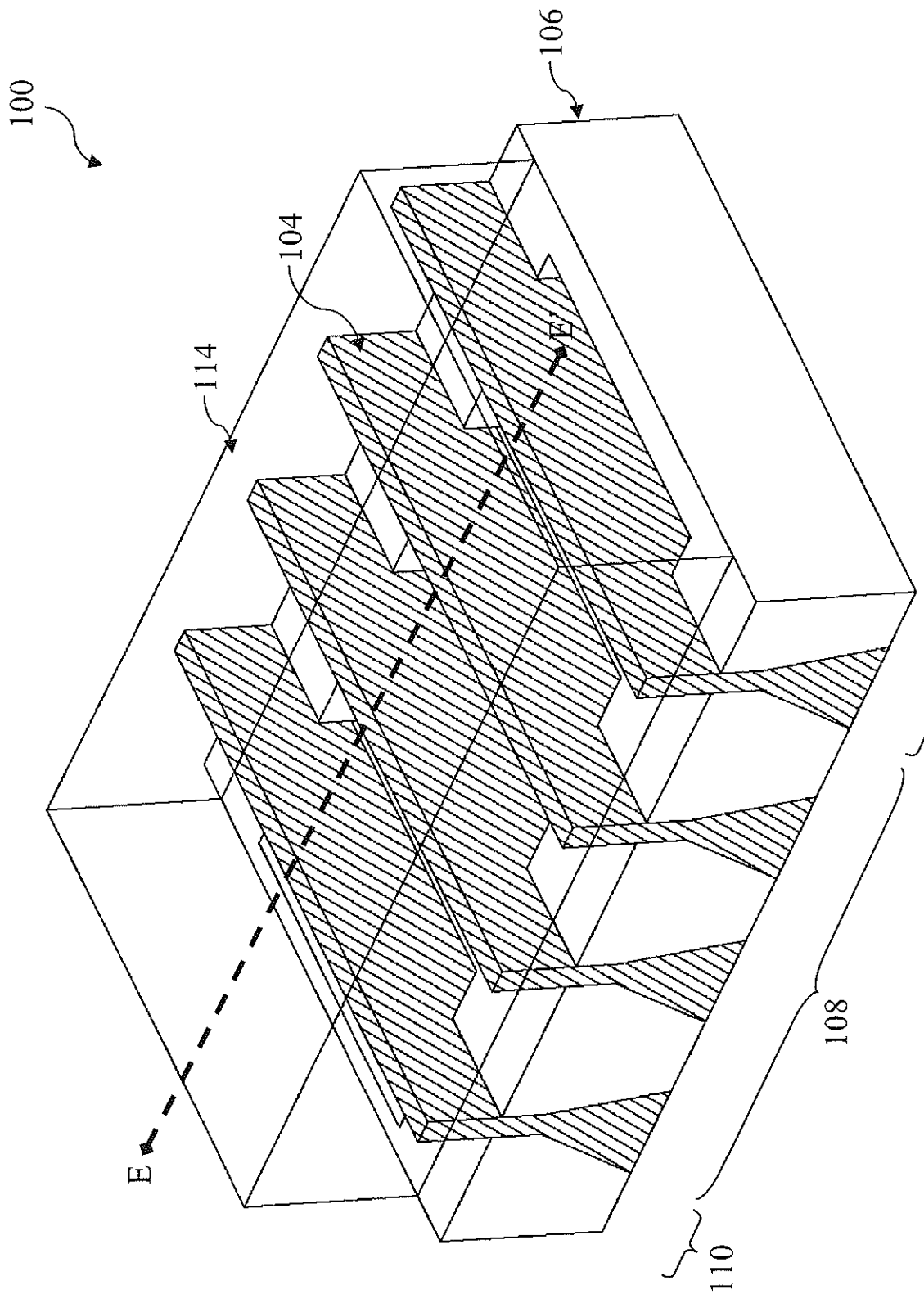


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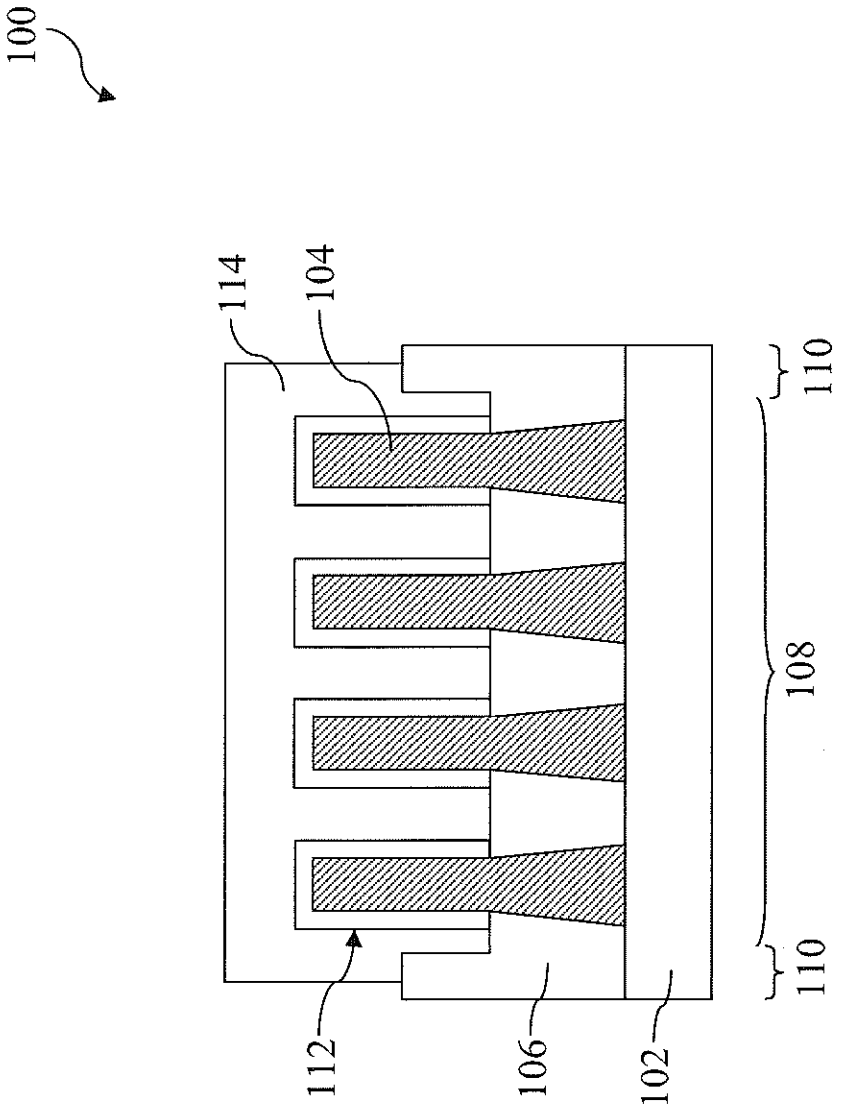


Fig. 7

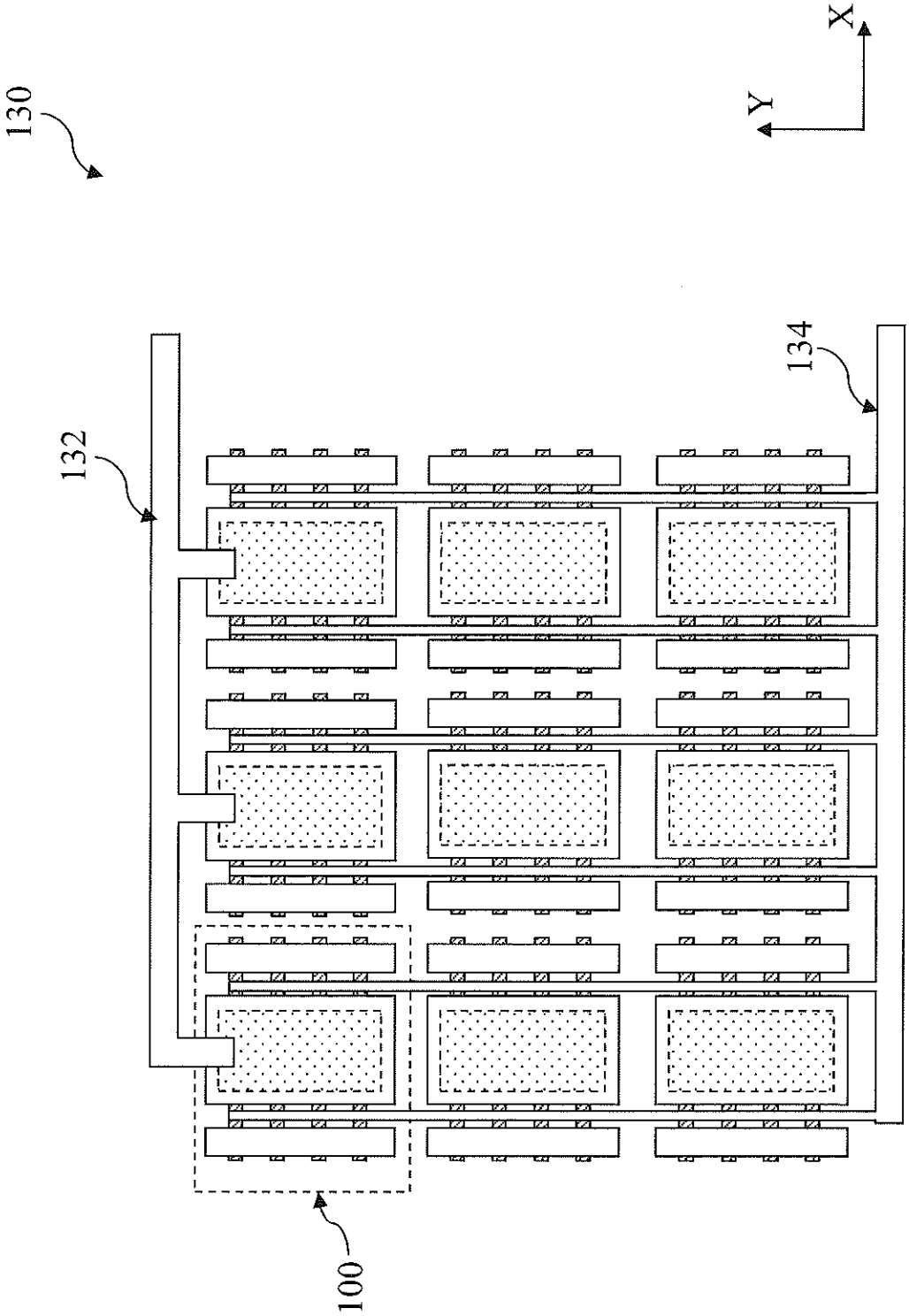


Fig. 8

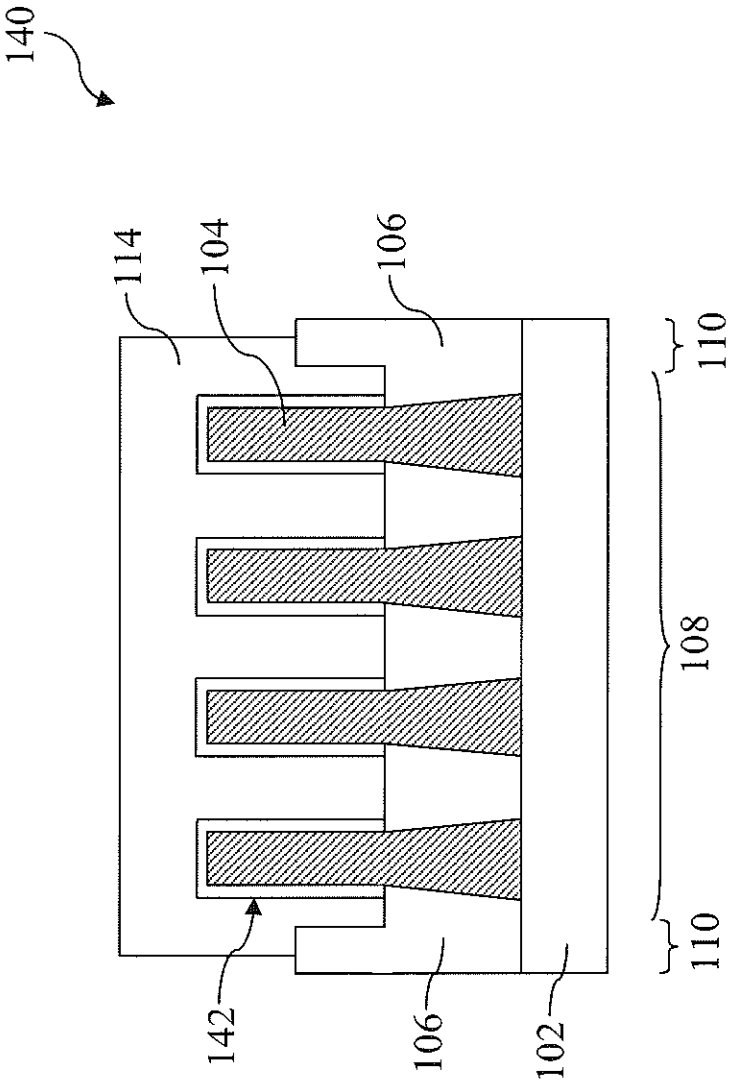


Fig. 9

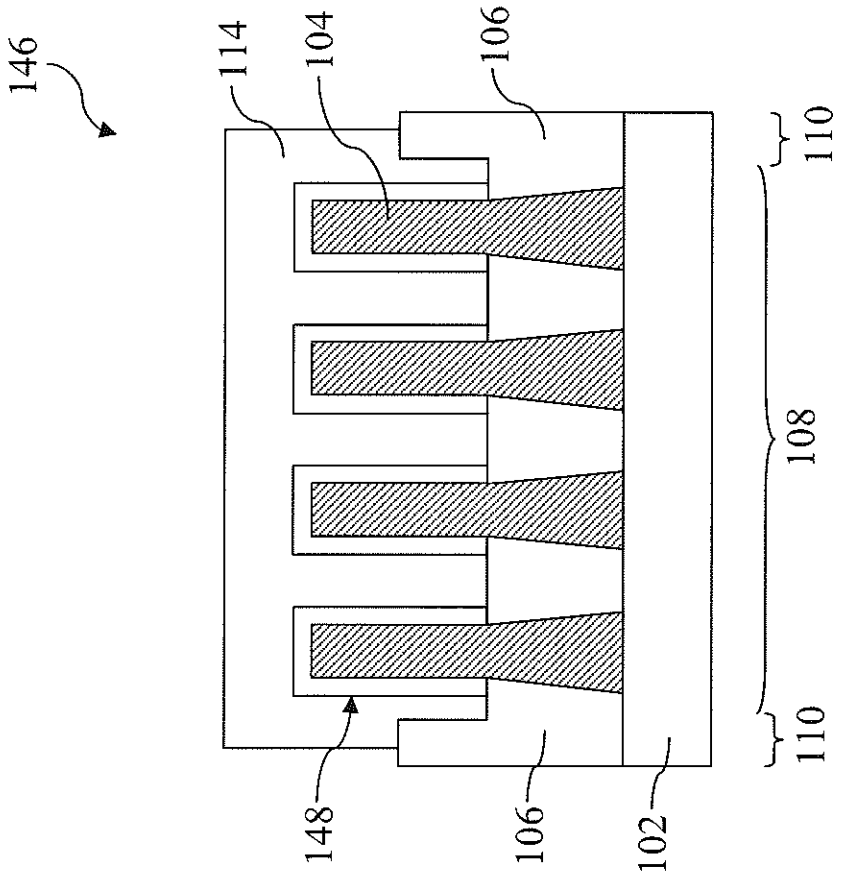


Fig. 10

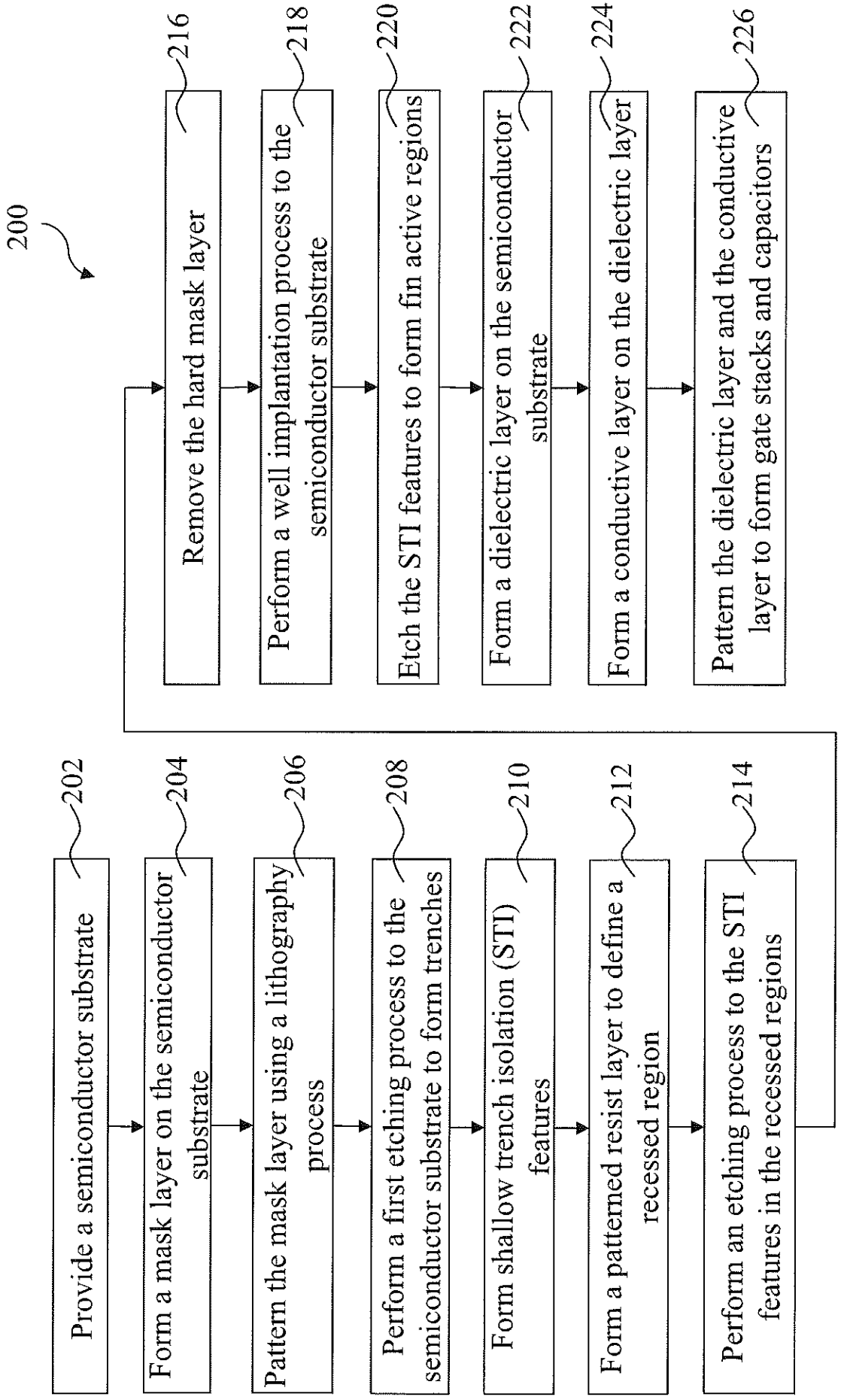

200
Provide a semiconductor substrate
202
Form a mask layer on the semiconductor substrate
204
Pattern the mask layer using a lithography process
206
Perform a first etching process to the semiconductor substrate to form trenches
208
Form shallow trench isolation (STI) features
210
Form a patterned resist layer to define a recessed region
212
Perform an etching process to the STI features in the recessed regions
214
Remove the hard mask layer
216
Perform a well implantation process to the semiconductor substrate
218
Etch the STI features to form fin active regions
220
Form a dielectric layer on the semiconductor substrate
222
Form a conductive layer on the dielectric layer
224
Pattern the dielectric layer and the conductive layer to form gate stacks and capacitors
226

Fig. 11

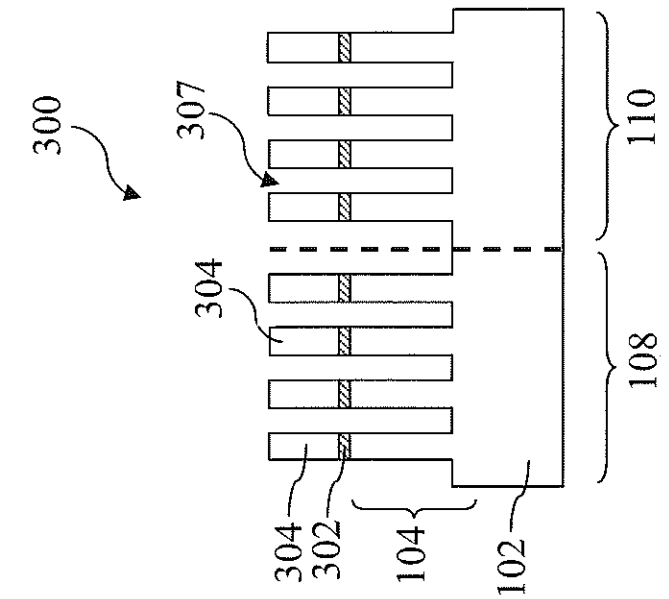

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Fig. 13

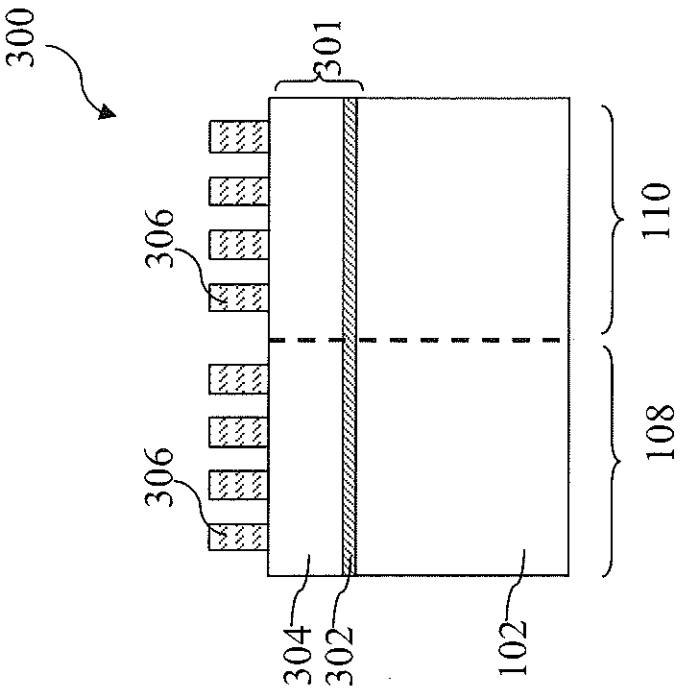

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Fig. 12

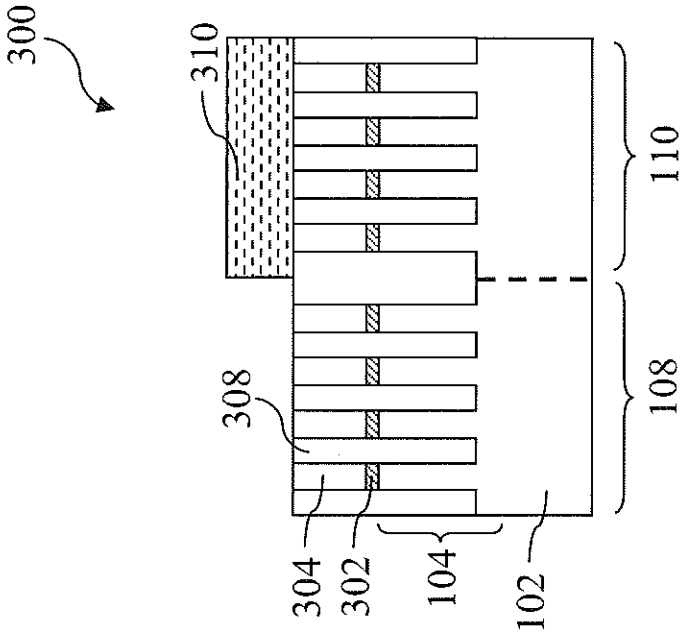

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Fig. 15

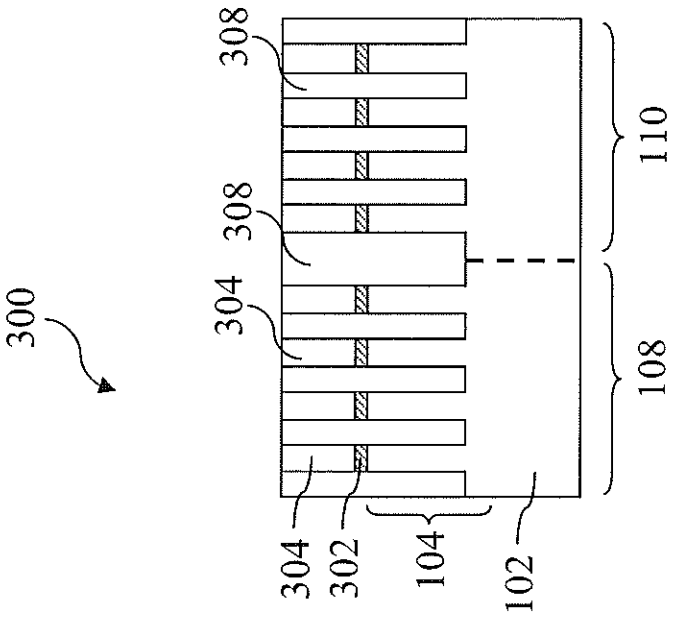

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Fig. 14

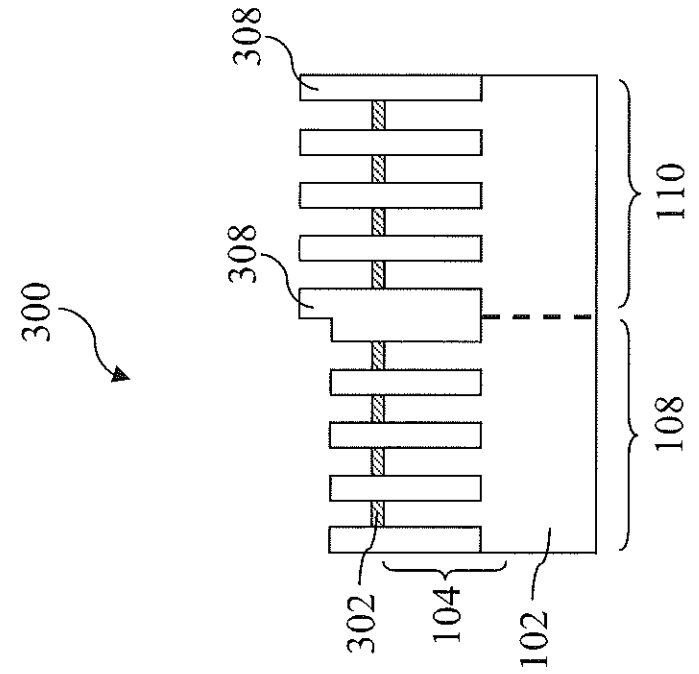

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Fig. 17

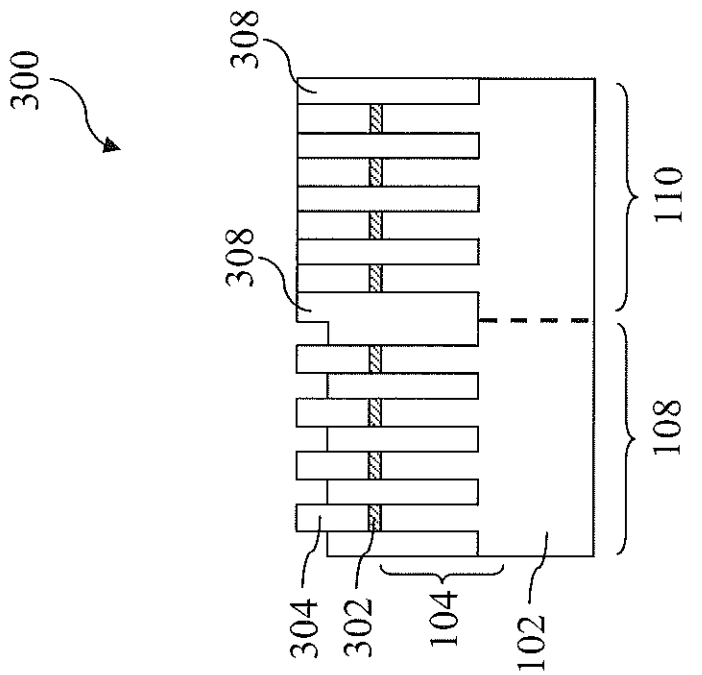

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Fig. 16

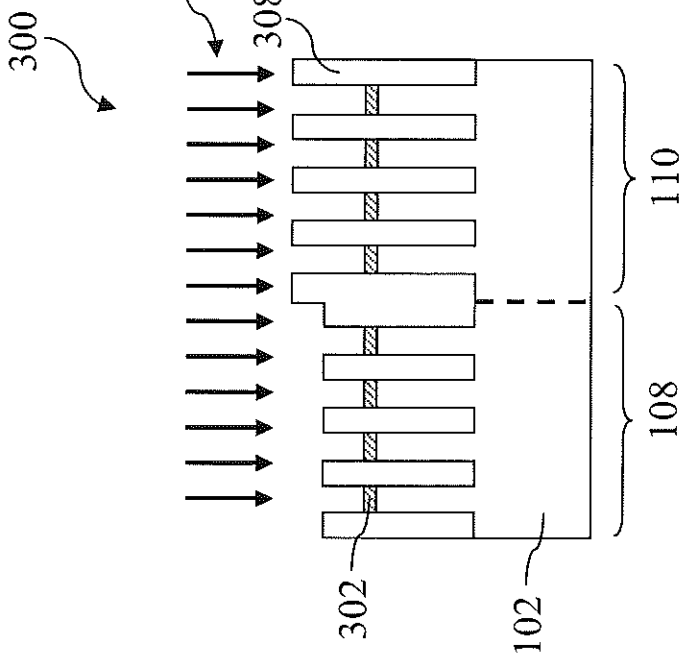


Fig. 18

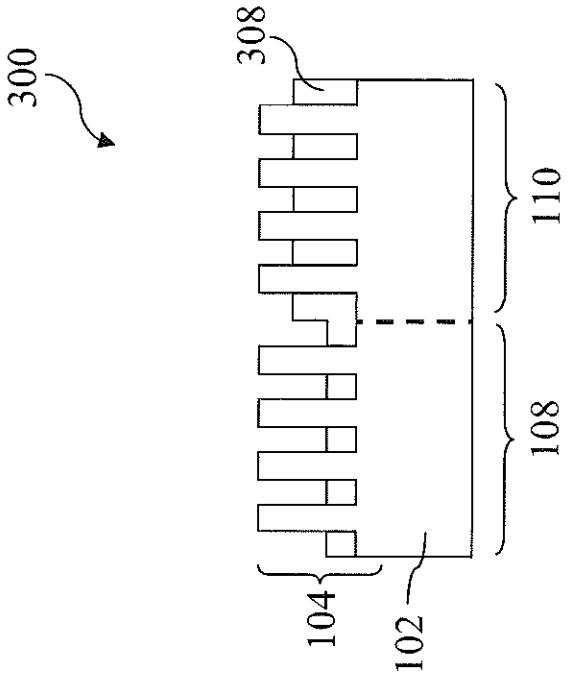


Fig. 19

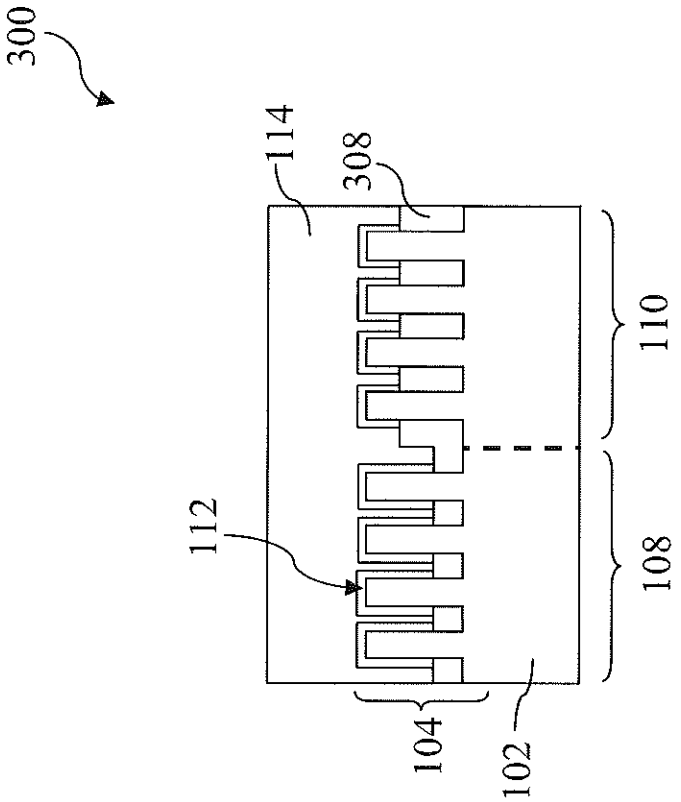


Fig. 21

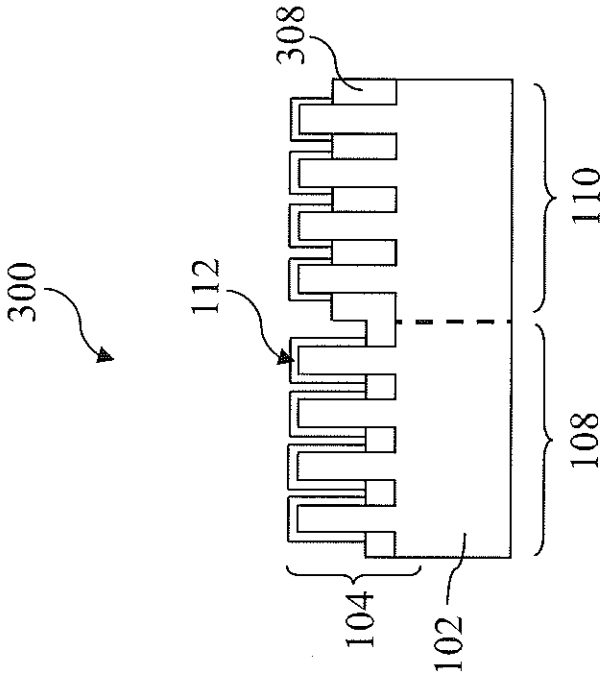


Fig. 20