FIG. 1

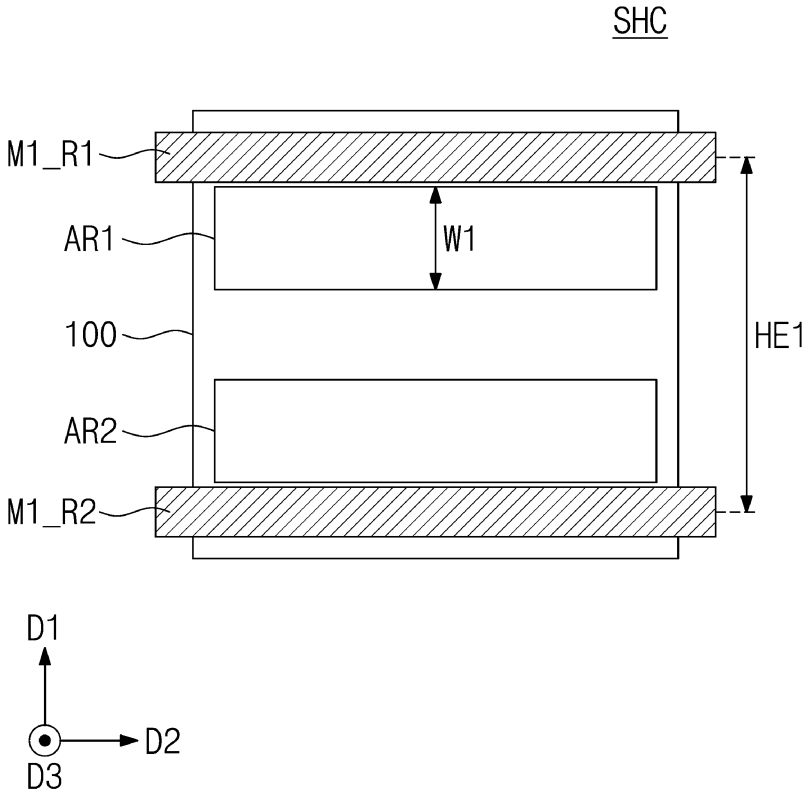


FIG. 2

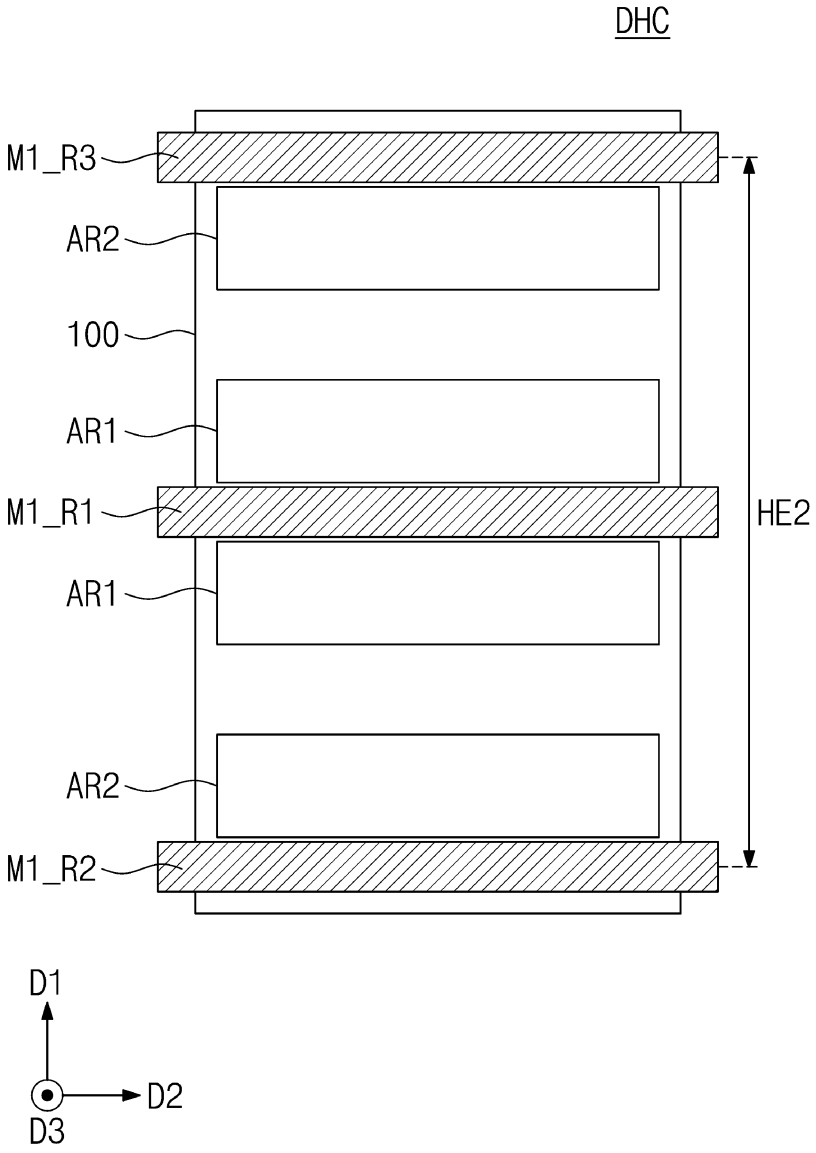


FIG. 3

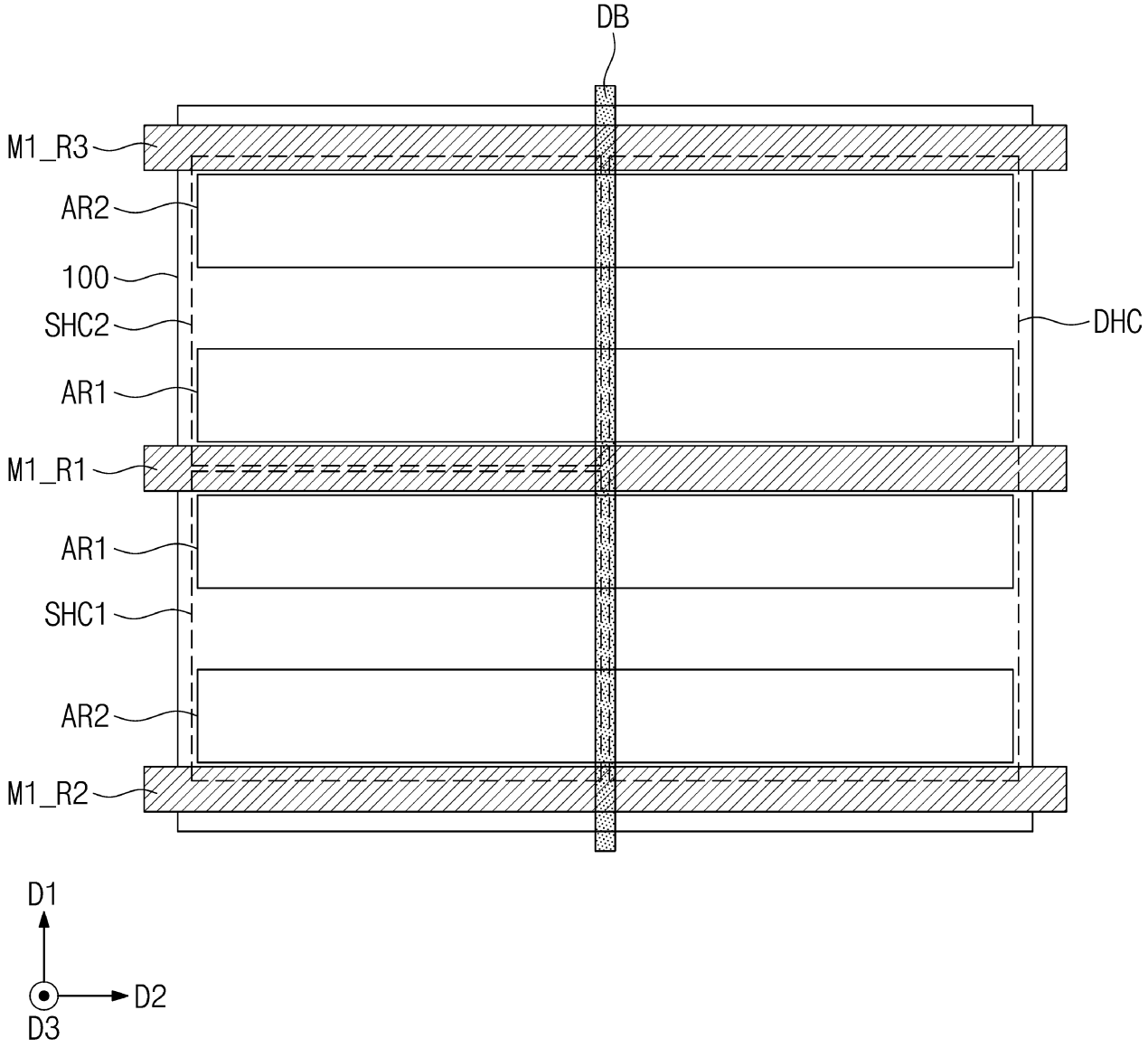


FIG. 4

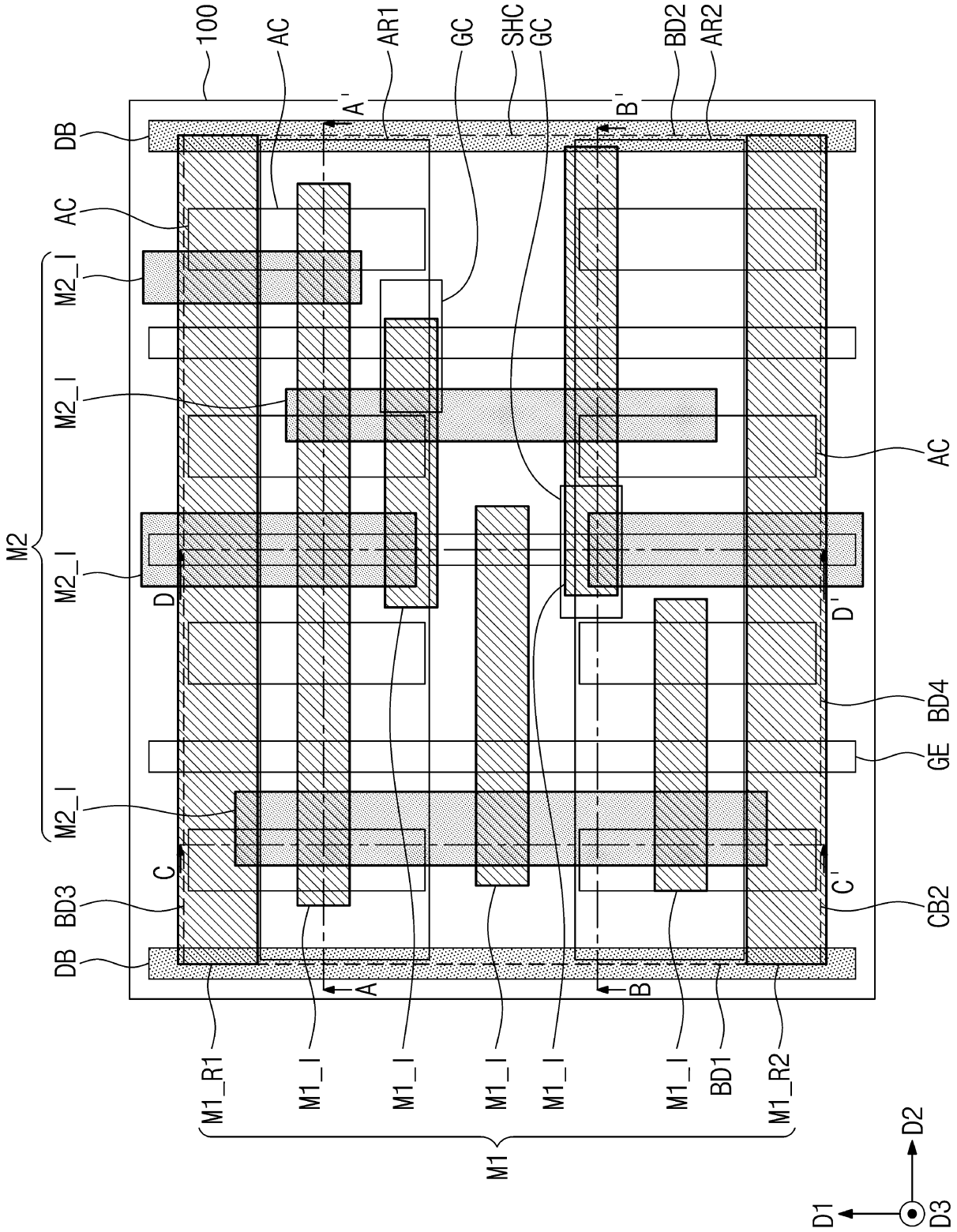

100
AC
AR1
GC
SHC
GC
BD2
AR2
A'
B'
DB
AC
M2_I
M2_I
M2_I
M2_I
M2
D
D'
C
C'
BD3
DB
AC
BD4
GE
CB2
A
B
M1_R1
M1_I
M1_I
M1_I
M1_I
M1_I
BD1
M1_R2
M1
D1
D2
D3

FIG. 5A

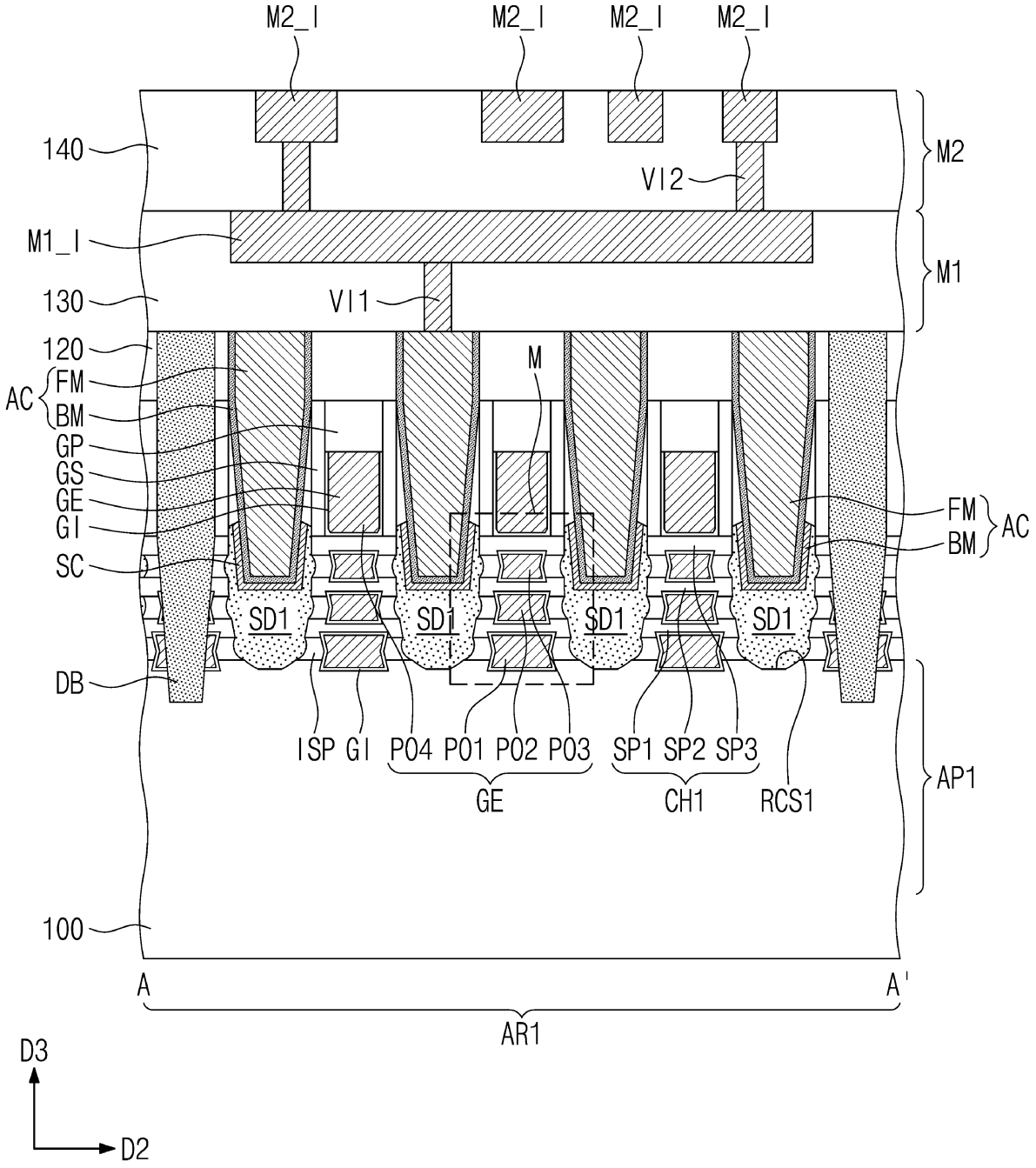

M2_I
M2_I
M2_I
M2_I
140
M2
VI2
M1_I
M1
130
VI1
120
M
AC
FM
BM
GP
GS
GE
GI
SC
FM
BM
AC
SD1
SD1
SD1
SD1
DB
ISP GI P04 P01 P02 P03 SP1 SP2 SP3
GE
CH1
RCS1
AP1
100
A
A'
AR1
D3
D2

FIG. 5B

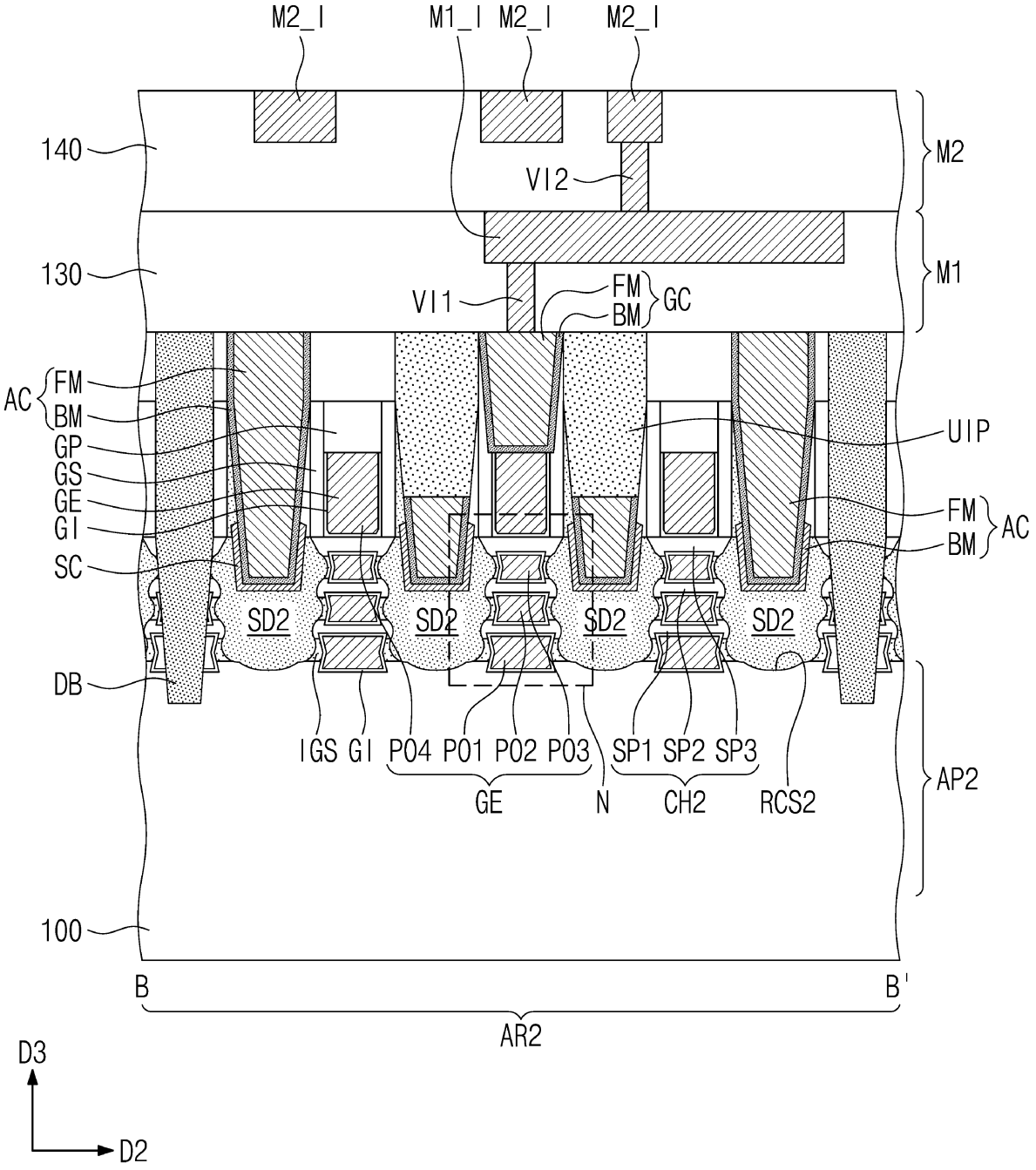

M2_I
M1_I
M2_I
M2_I
140
VI2
M2
130
M1
VI1
FM
BM
GC
AC
FM
BM
GP
GS
GE
GI
SC
UIP
FM
BM
AC
SD2
SD2
SD2
SD2
DB
IGS
GI
P04
P01
P02
P03
SP1
SP2
SP3
GE
N
CH2
RCS2
AP2
100
B
B'
AR2
D3
D2

FIG. 5C

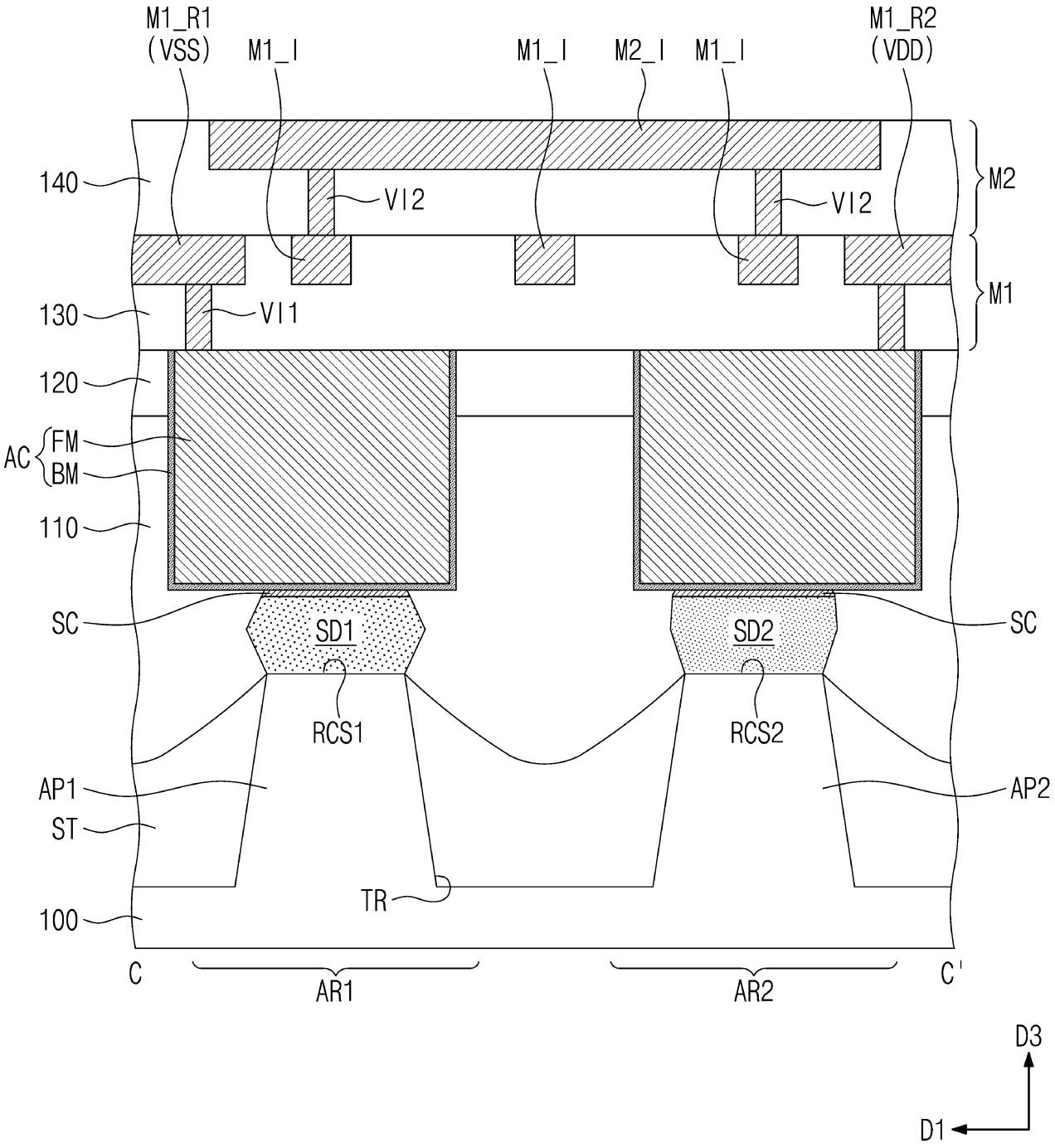

M1_R1
(VSS)
M1_I
M1_I
M2_I
M1_I
M1_R2
(VDD)
140
VI2
VI2
M2
M1
130
VI1
120
AC
FM
BM
110
SC
SD1
SD2
SC
RCS1
RCS2
AP1
AP2
ST
TR
100
C
AR1
AR2
C'
D3
D1

FIG. 5D

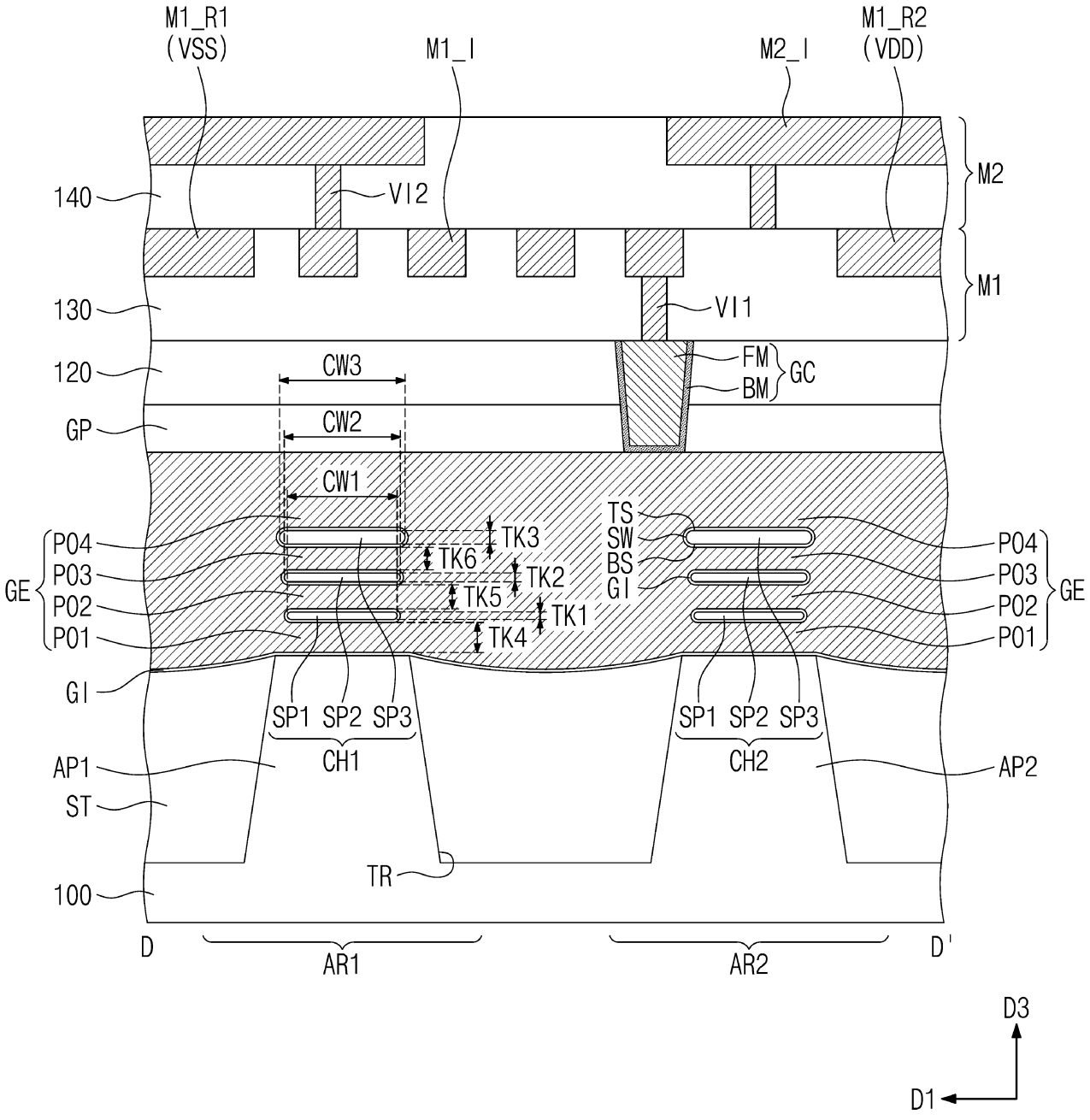

M1_R1
(VSS)
M1_I
M2_I
M1_R2
(VDD)
M2
M1
140
VI2
130
VI1
120
CW3
FM
BM
GC
GP
CW2
CW1
TS
SW
BS
GI
P04
P03
P02
P01
GE
TK3
TK6
TK2
TK5
TK1
TK4
SP1
SP2
SP3
CH1
CH2
AP1
AP2
ST
TR
100
D
D'
AR1
AR2
D3
D1

FIG. 6A

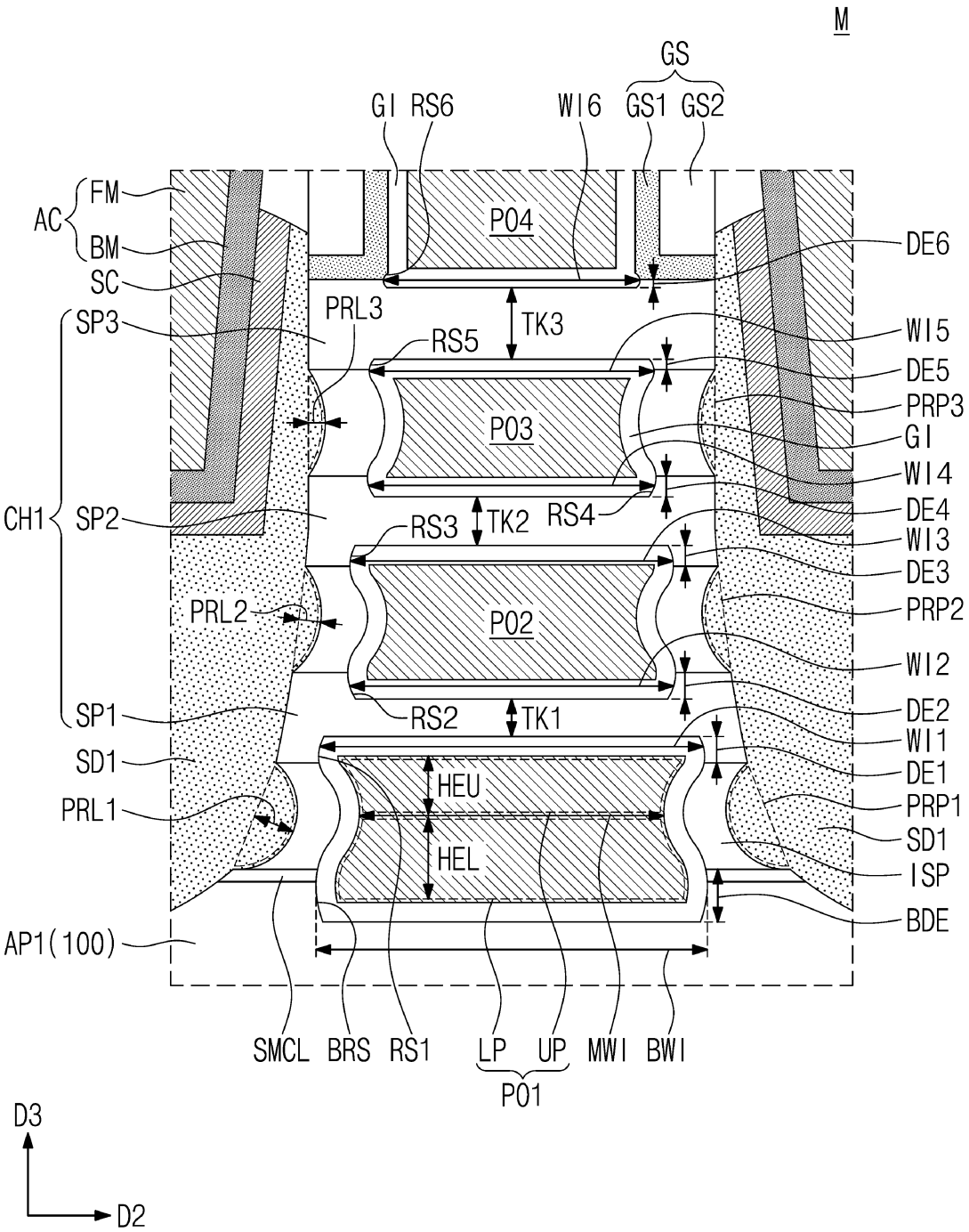

M
GS
GI
RS6
WI6
GS1
GS2
AC
FM
BM
SC
P04
DE6
SP3
PRL3
TK3
RS5
WI5
DE5
PRP3
P03
GI
WI4
CH1
SP2
RS3
TK2
RS4
DE4
WI3
DE3
PRL2
P02
PRP2
WI2
SP1
RS2
TK1
DE2
WI1
SD1
HEU
DE1
PRL1
PRP1
HEL
SD1
ISP
BDE
AP1(100)
SMCL
BRS
RS1
LP
UP
MWI
BWI
P01
D3
D2

FIG. 6B

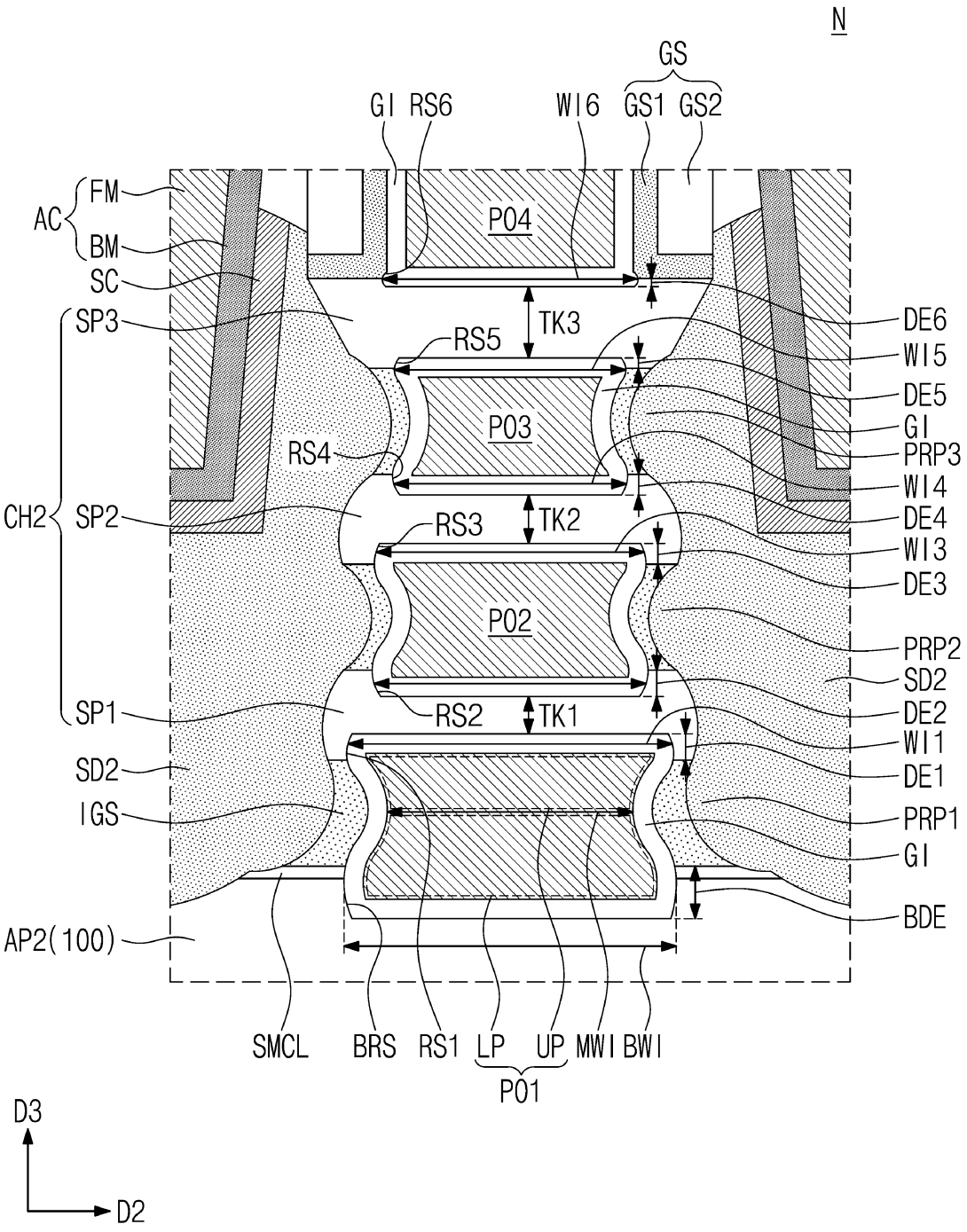

N
GS
GI
RS6
WI6
GS1
GS2
AC
FM
BM
SC
P04
SP3
TK3
RS5
DE6
WI5
DE5
GI
P03
RS4
PRP3
WI4
DE4
CH2
SP2
RS3
TK2
WI3
DE3
P02
PRP2
SD2
SP1
RS2
TK1
DE2
WI1
SD2
DE1
IGS
PRP1
GI
BDE
AP2(100)
SMCL
BRS
RS1
LP
UP
MWI
BWI
P01
D3
D2

FIG. 7A

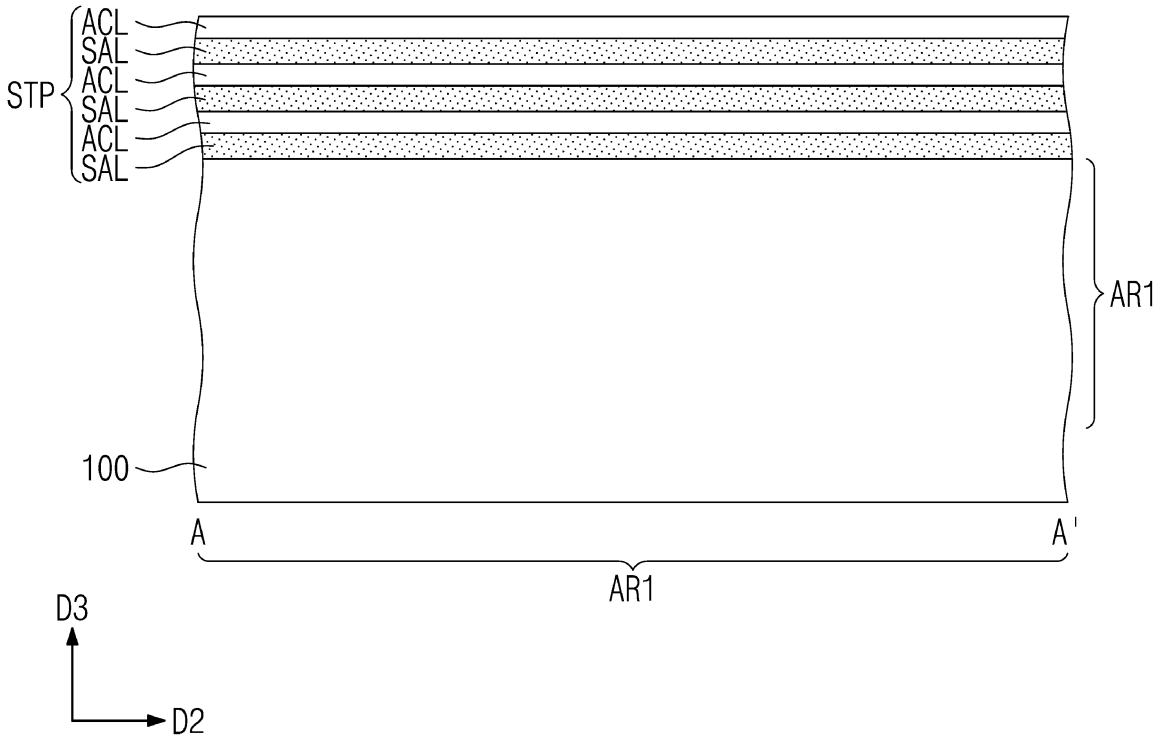


FIG. 7B

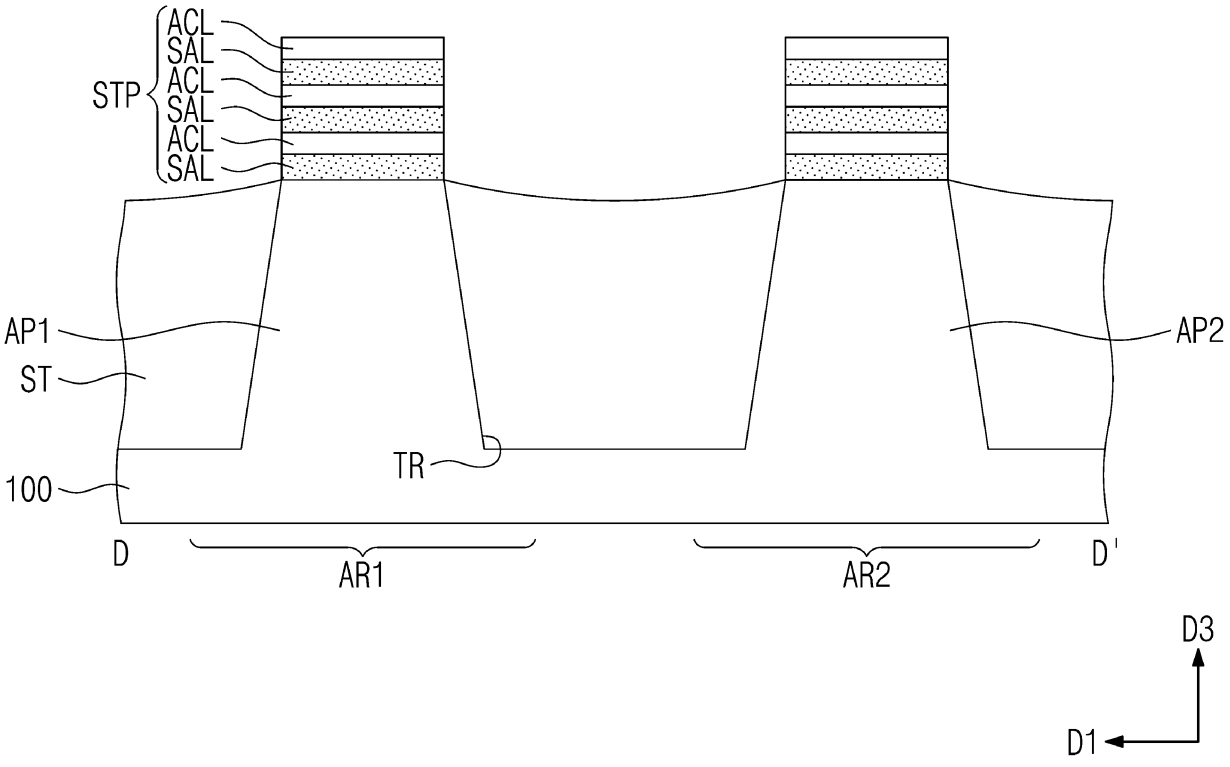


FIG. 8A

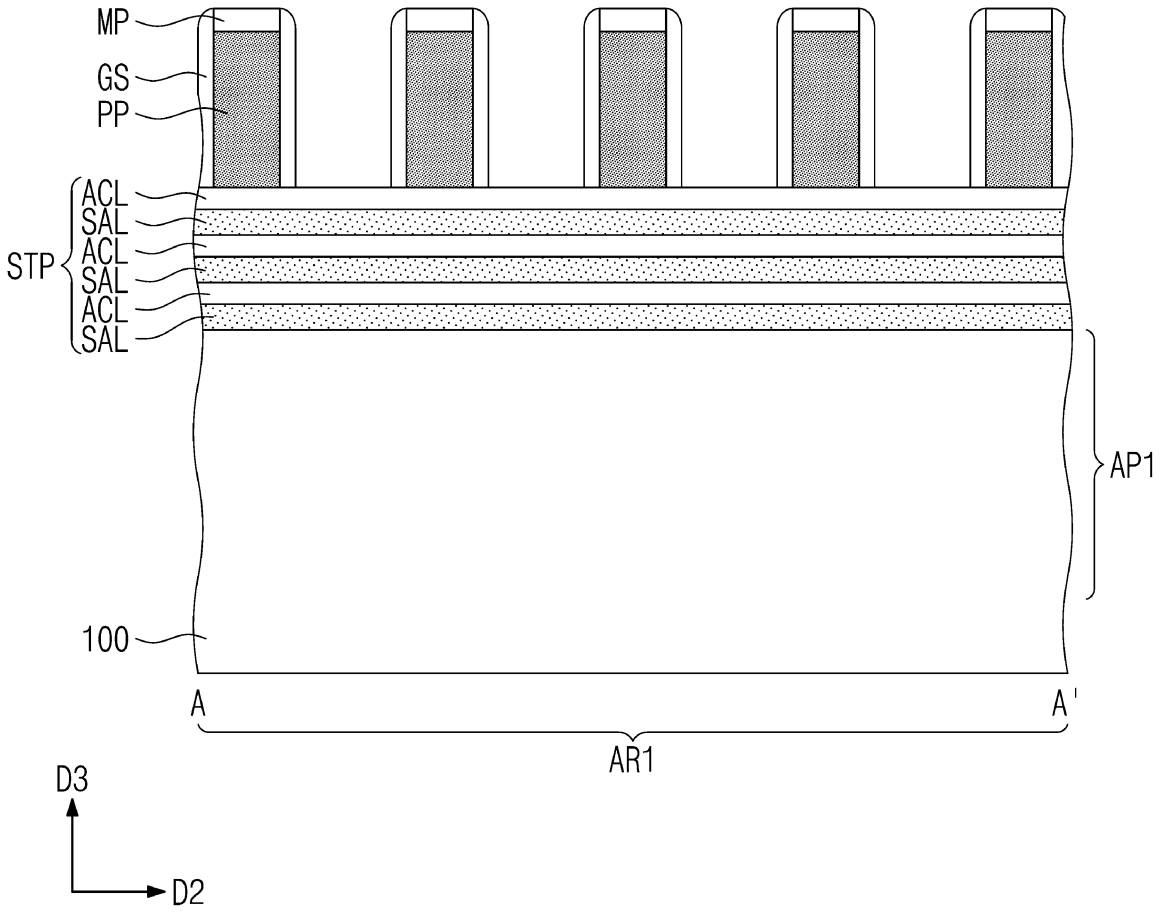


FIG. 8B

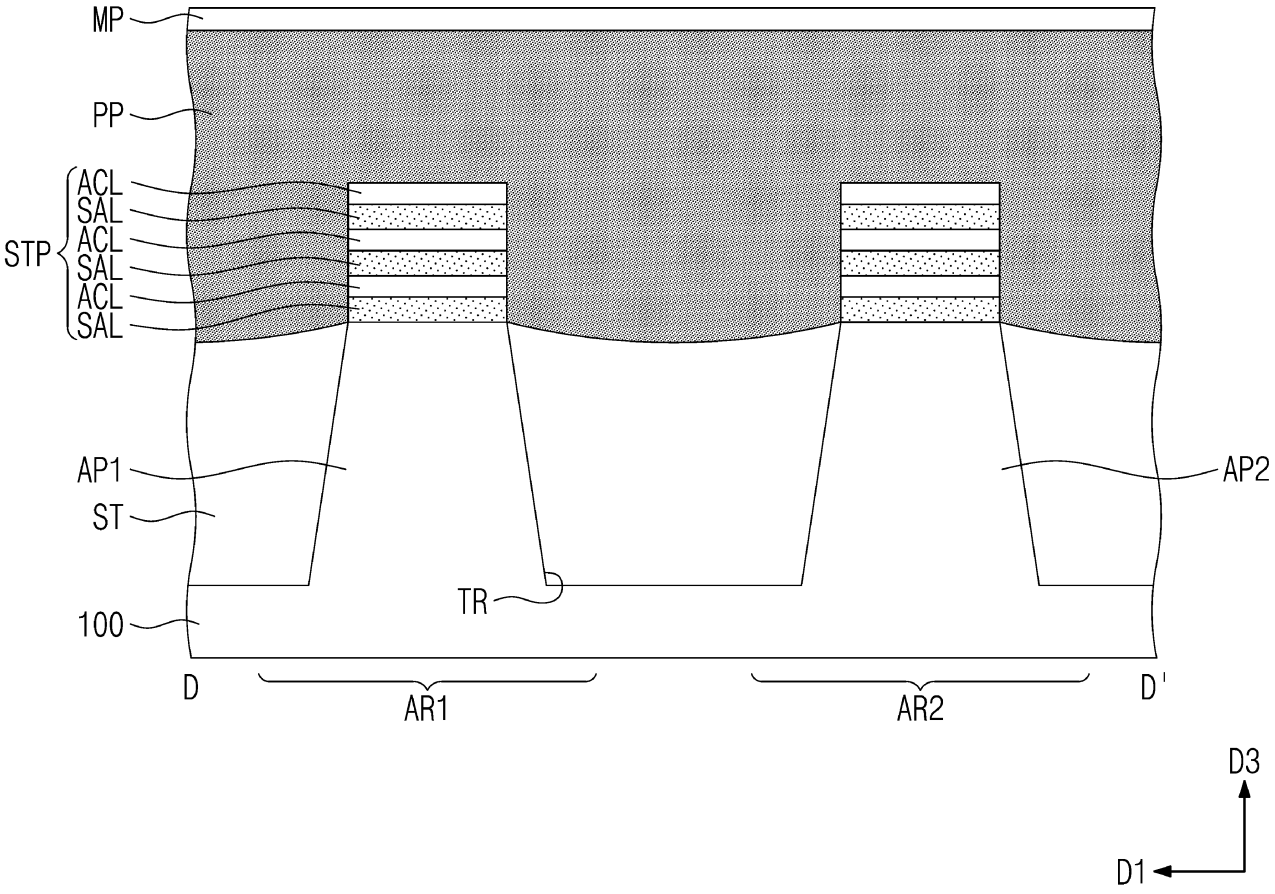

MP
PP
ACL
SAL
ACL
SAL
ACL
SAL
STP
AP1
AP2
ST
TR
100
D
AR1
AR2
D'
D3
D1

FIG. 9A

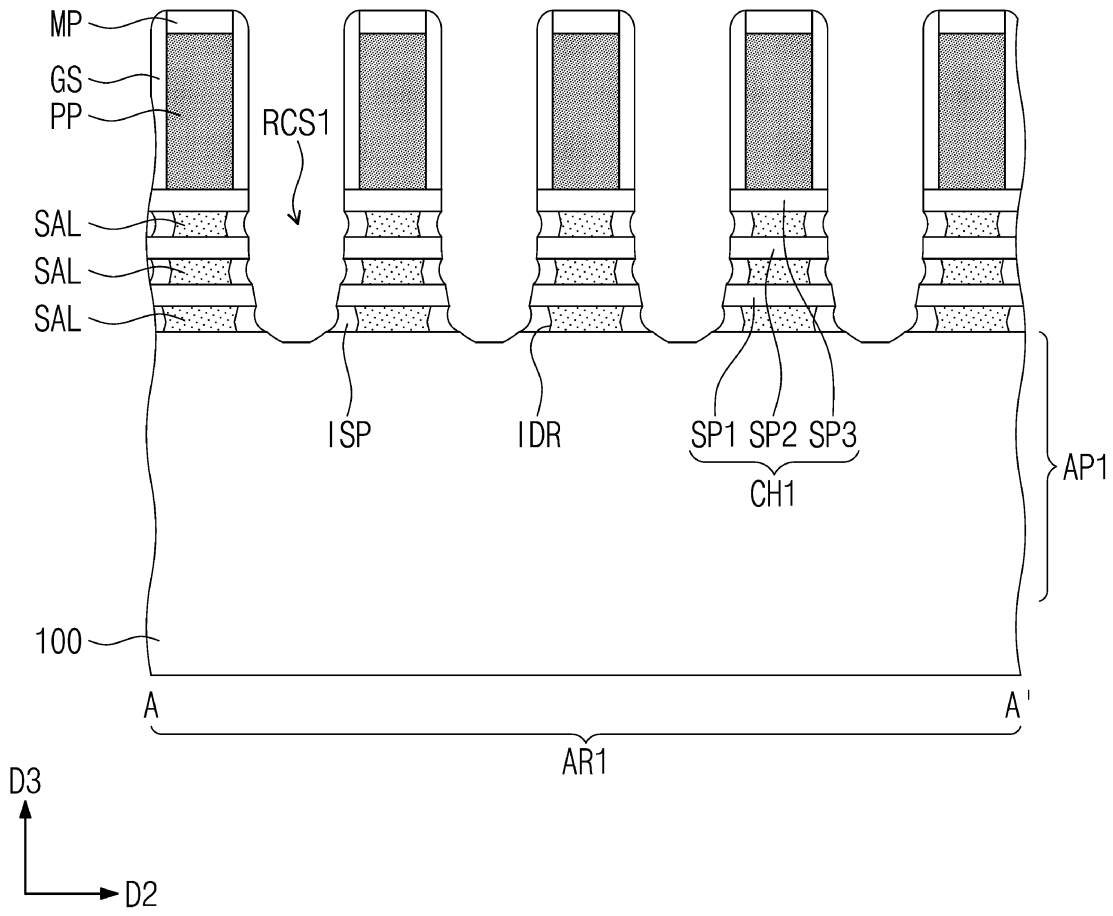

MP
GS
PP
RCS1
SAL
SAL
SAL
ISP
IDR
SP1 SP2 SP3
CH1
AP1
100
A
A'
AR1
D3
D2

FIG. 9B

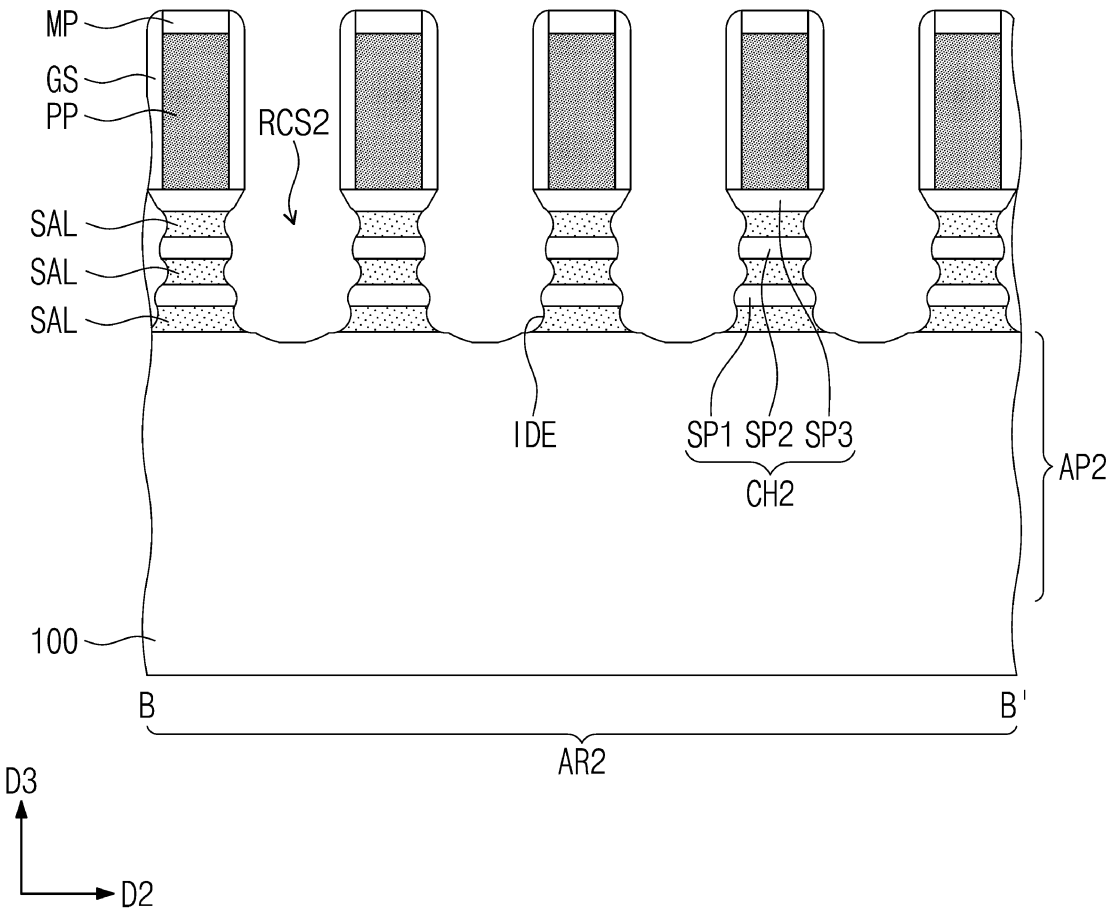


FIG. 9C

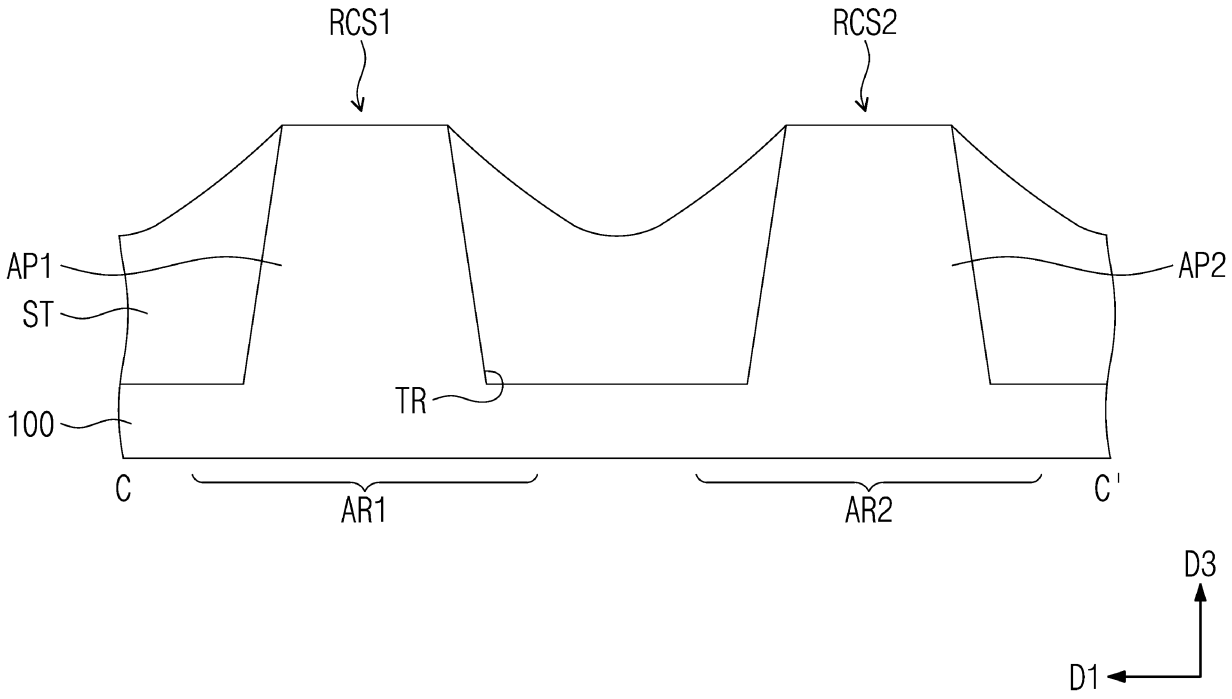


FIG. 10A

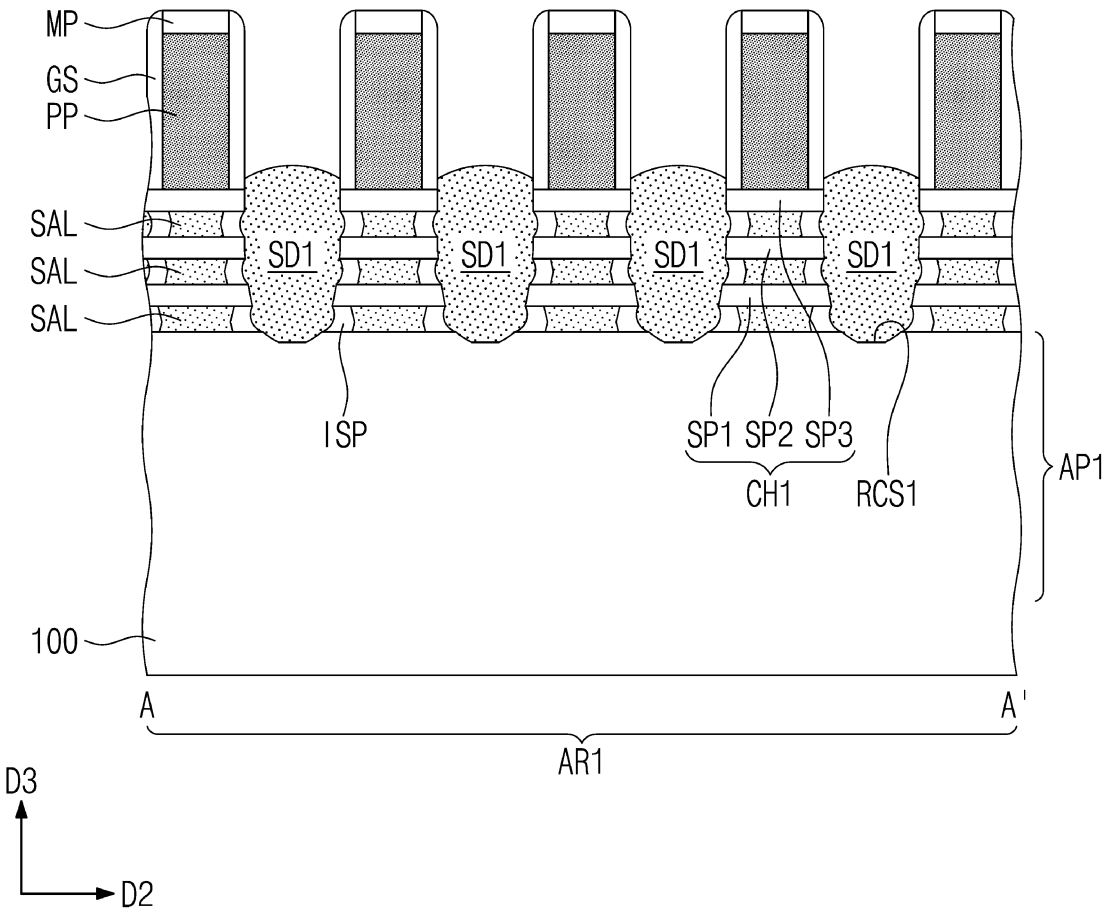

MP
GS
PP
SAL
SAL
SAL
SD1
SD1
SD1
SD1
ISP
SP1 SP2 SP3
CH1
RCS1
AP1
100
A
A'
AR1
D3
D2

FIG. 10B

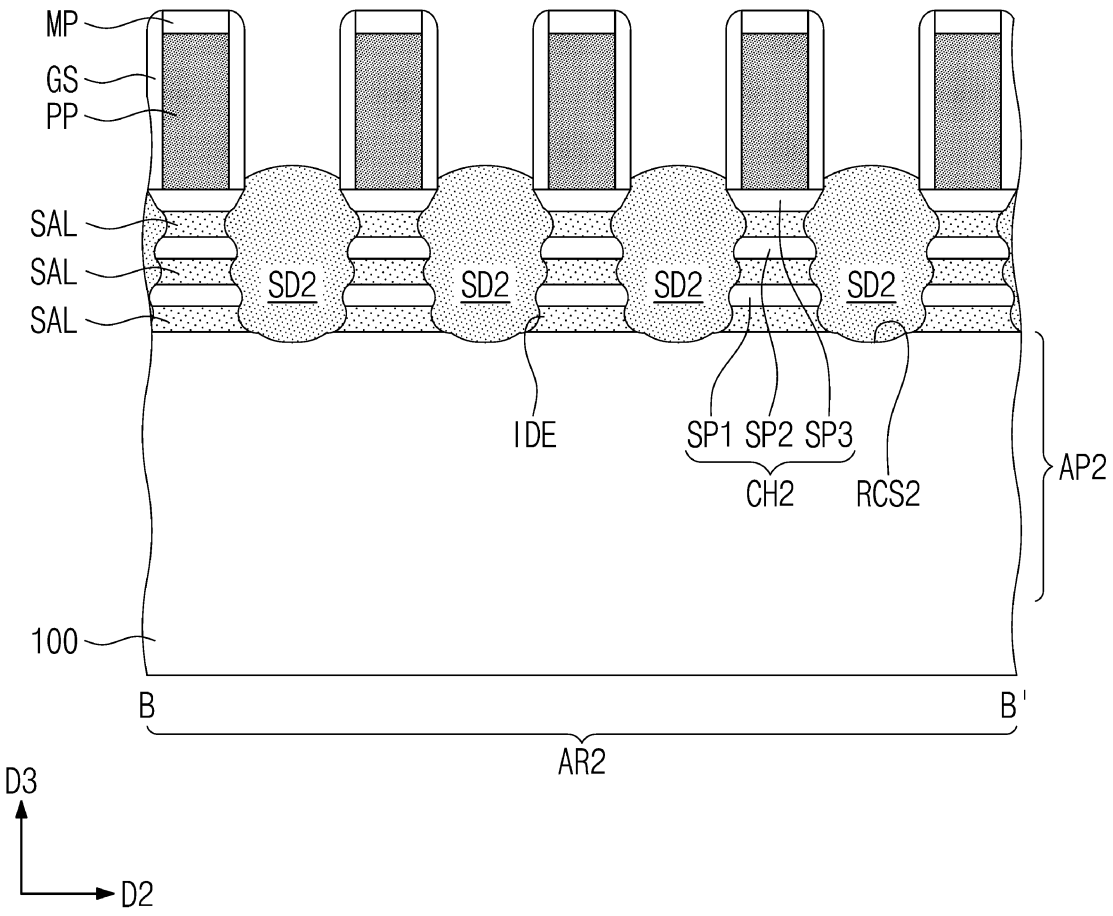

MP
GS
PP
SAL
SAL
SAL
SD2
SD2
SD2
SD2
IDE
SP1 SP2 SP3
CH2
RCS2
AP2
100
B
B'
AR2
D3
D2

FIG. 10C

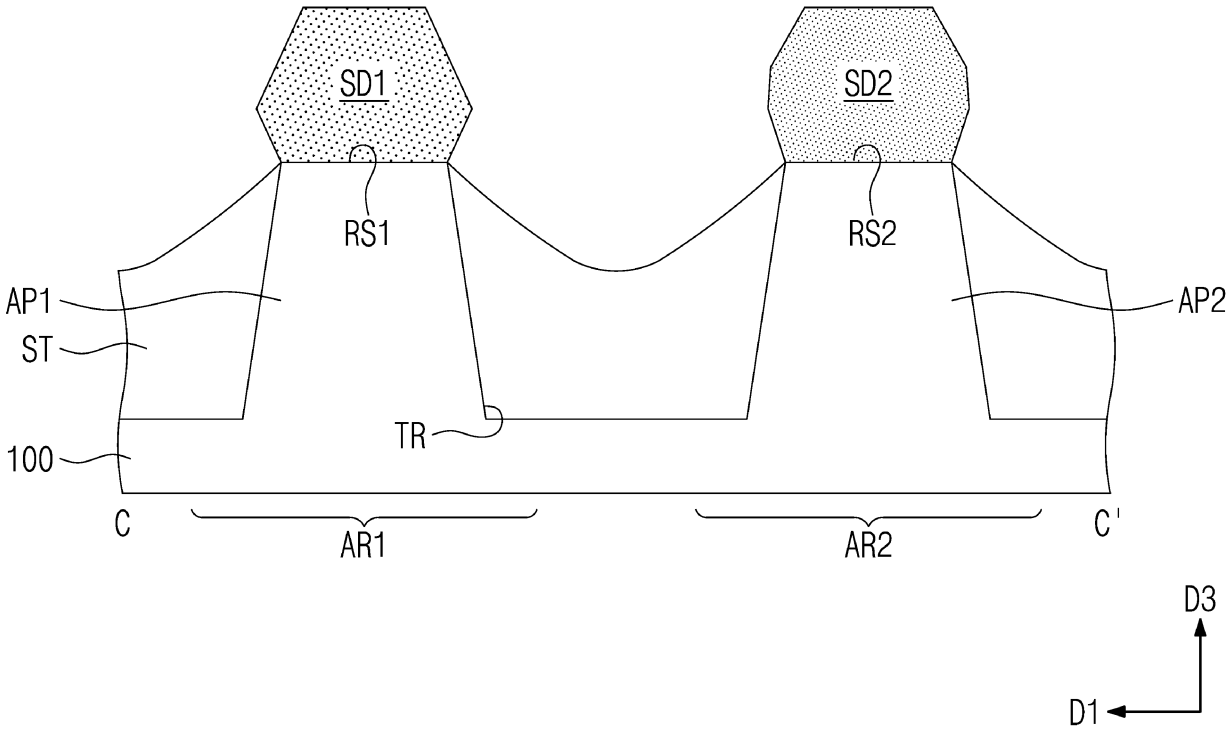


FIG. 11A

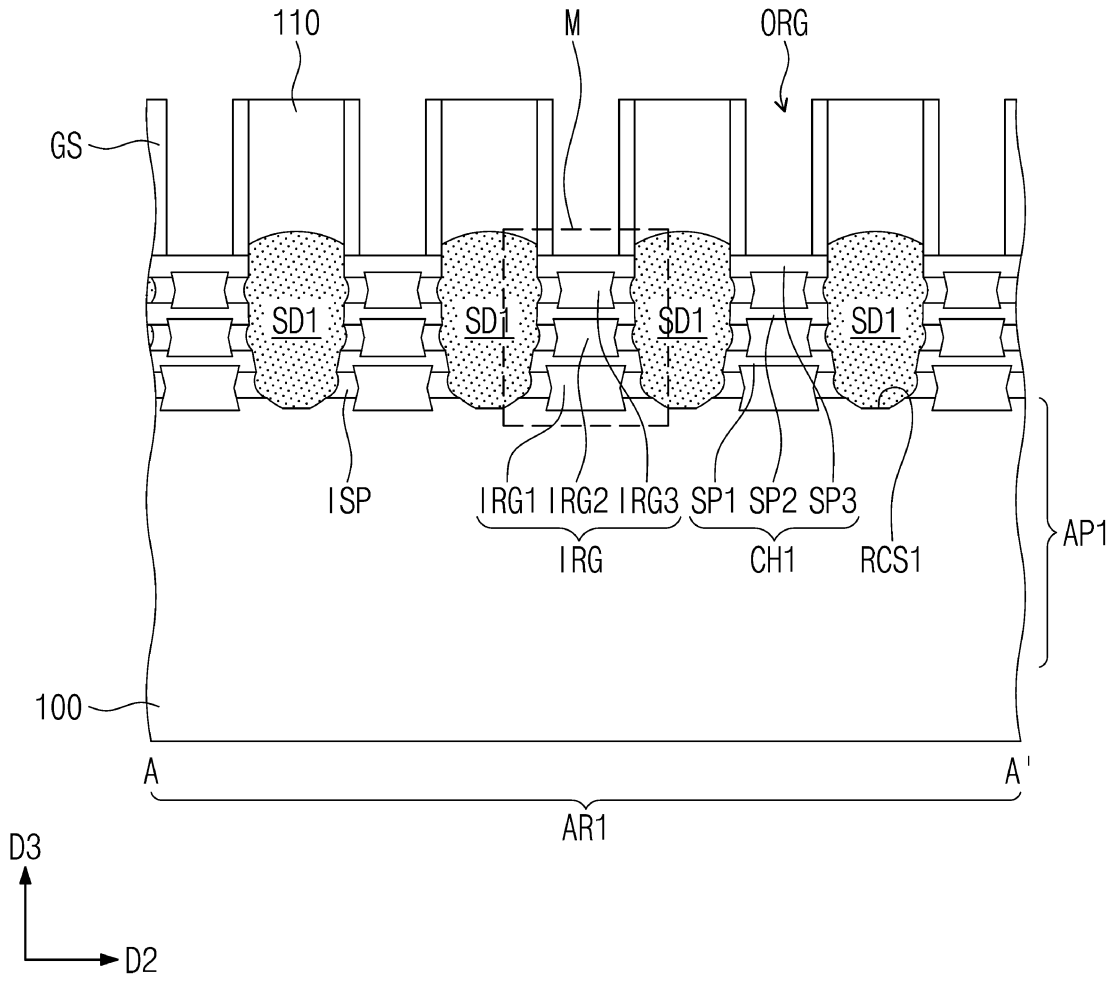

110
M
ORG
GS
SD1
SD1
SD1
SD1
ISP
IRG1
IRG2
IRG3
SP1
SP2
SP3
IRG
CH1
RCS1
AP1
100
A
A'
AR1
D3
D2

FIG. 11B

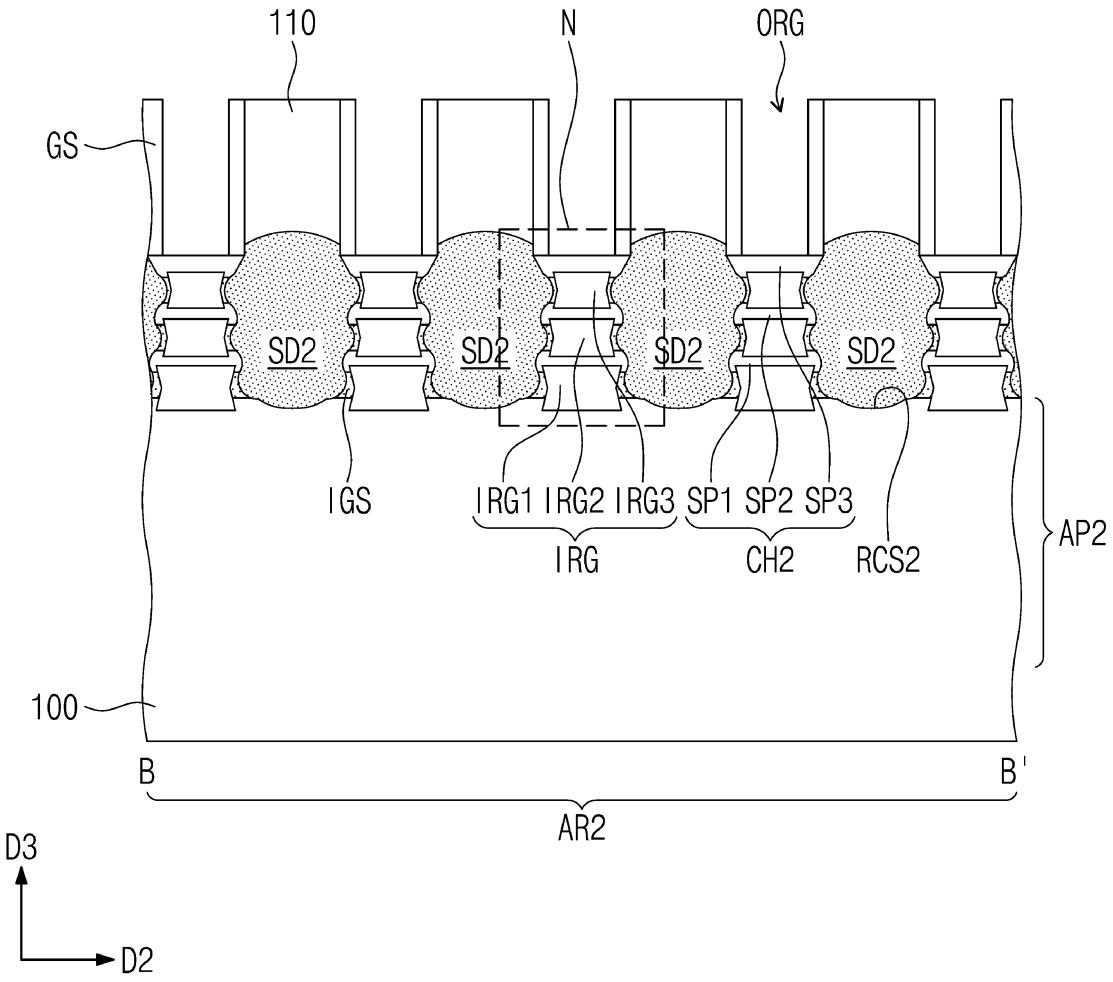

110
N
ORG
GS
SD2
SD2
SD2
SD2
IGS
IRG1
IRG2
IRG3
SP1
SP2
SP3
IRG
CH2
RCS2
AP2
100
B
B'
AR2
D3
D2

FIG. 11C

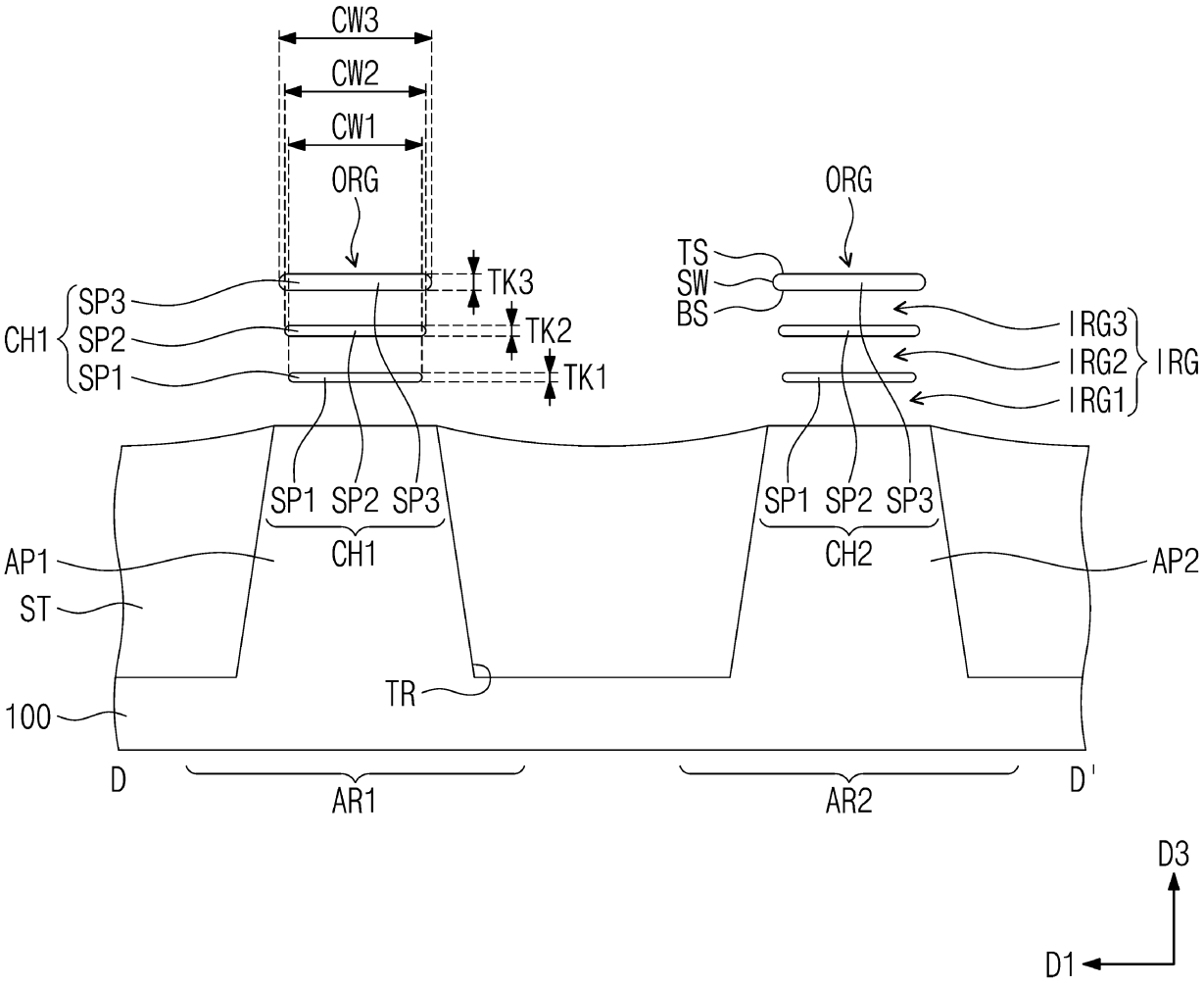

CW3
CW2
CW1
ORG
ORG
TS
SW
BS
TK3
TK2
TK1
CH1
SP3
SP2
SP1
IRG3
IRG2
IRG1
IRG
SP1 SP2 SP3
CH1
SP1 SP2 SP3
CH2
AP1
AP2
ST
TR
100
D
D'
AR1
AR2
D3
D1

FIG. 12A

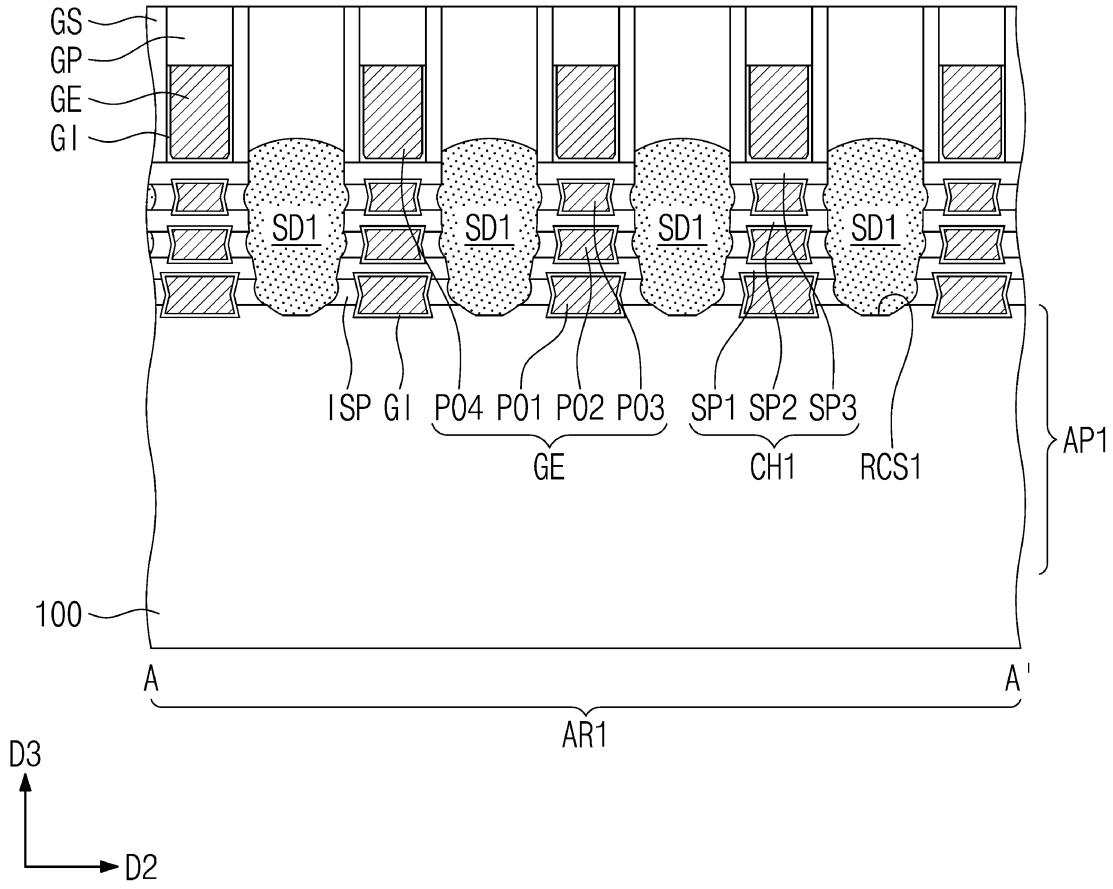

GS
GP
GE
GI
SD1
SD1
SD1
SD1
ISP
GI
P04
P01
P02
P03
SP1
SP2
SP3
GE
CH1
RCS1
AP1
100
A
A'
AR1
D3
D2

FIG. 12B

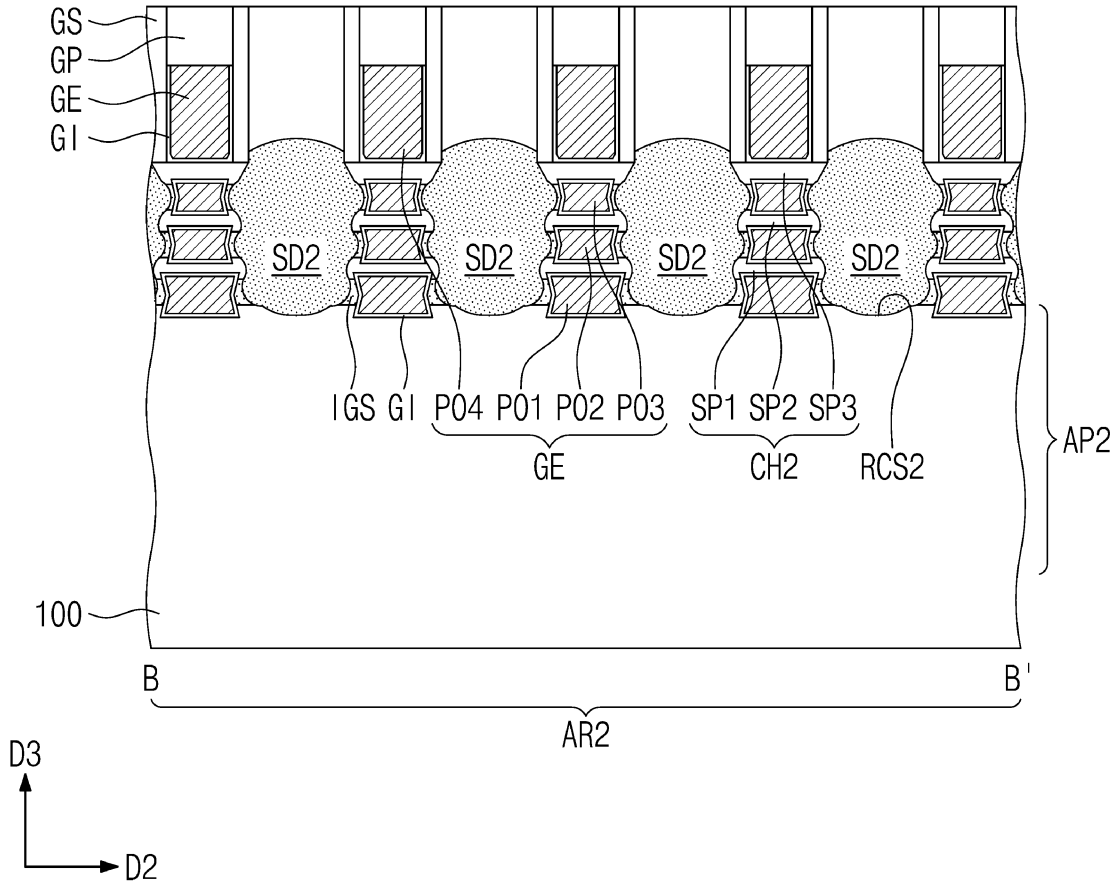

GS
GP
GE
GI
SD2
SD2
SD2
SD2
IGS GI P04 P01 P02 P03 SP1 SP2 SP3
GE
CH2
RCS2
AP2
100
B
B'
AR2
D3
D2

FIG. 12C

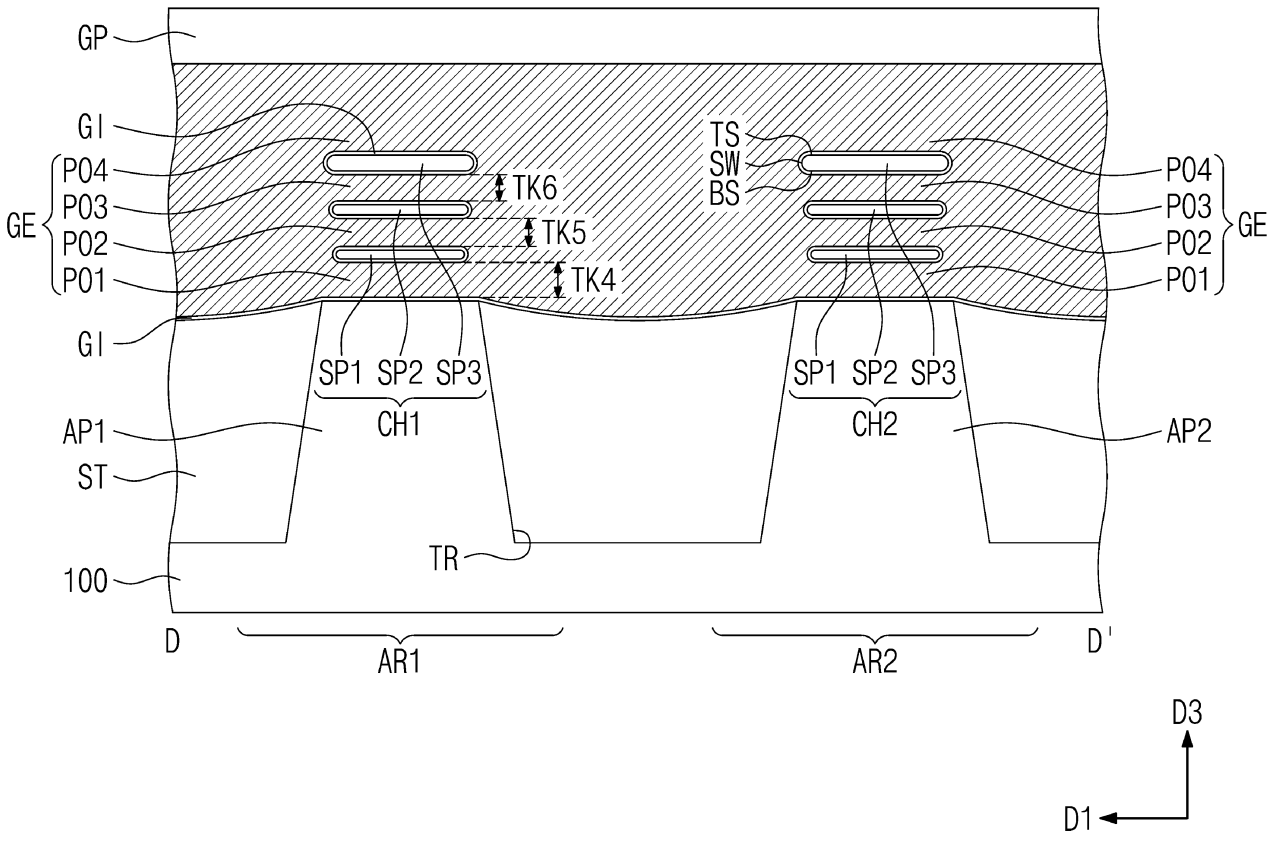

GP
GI
GE
P04
P03
P02
P01
TK6
TK5
TK4
TS
SW
BS
GI
SP1 SP2 SP3
CH1
SP1 SP2 SP3
CH2
AP1
AP2
ST
TR
100
D
AR1
AR2
D'
D3
D1

FIG. 13A

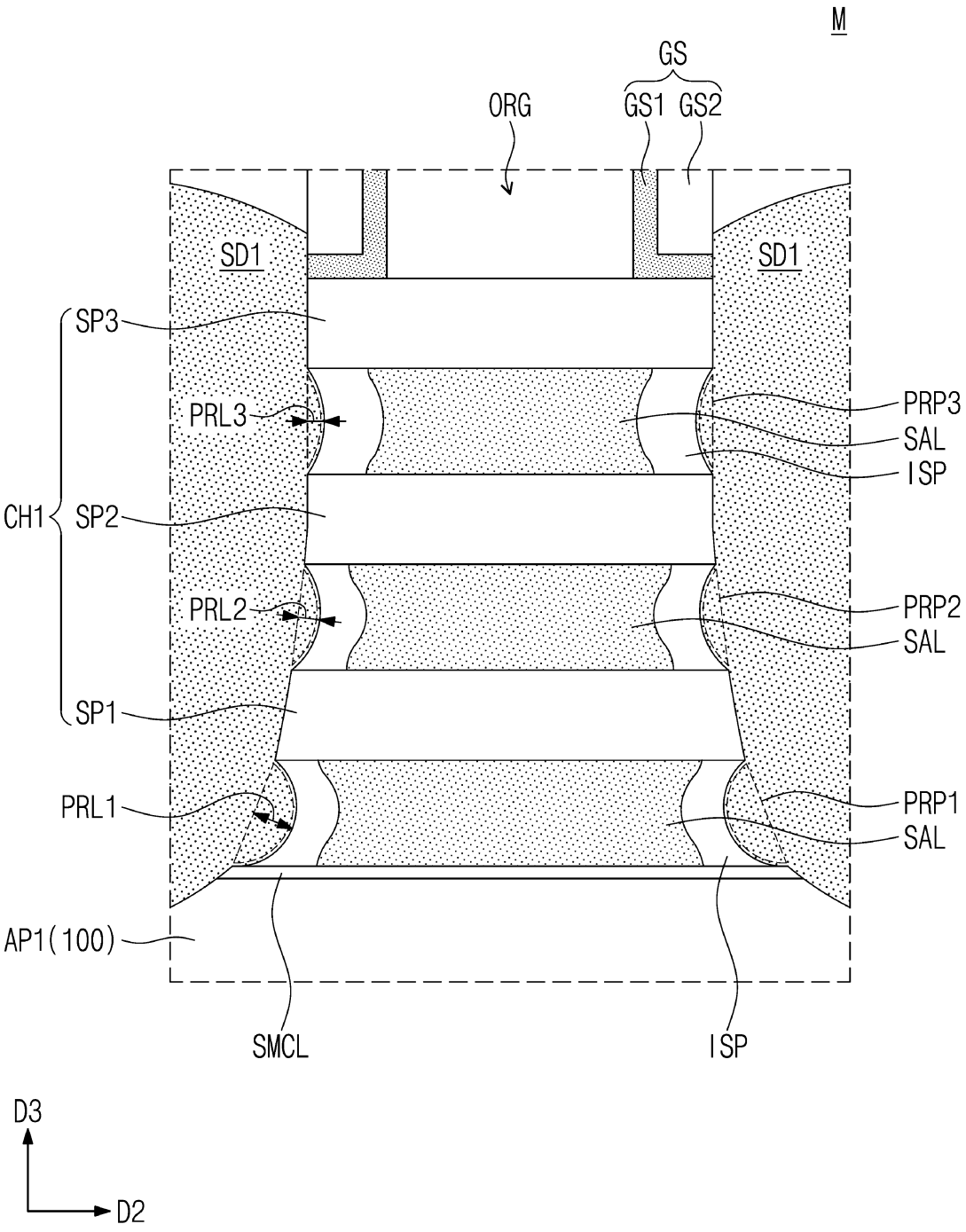

M
GS
ORG
GS1
GS2
SD1
SD1
SP3
PRL3
PRP3
SAL
ISP
CH1
SP2
PRL2
PRP2
SAL
SP1
PRL1
PRP1
SAL
AP1(100)
SMCL
ISP
D3
D2

FIG. 13B

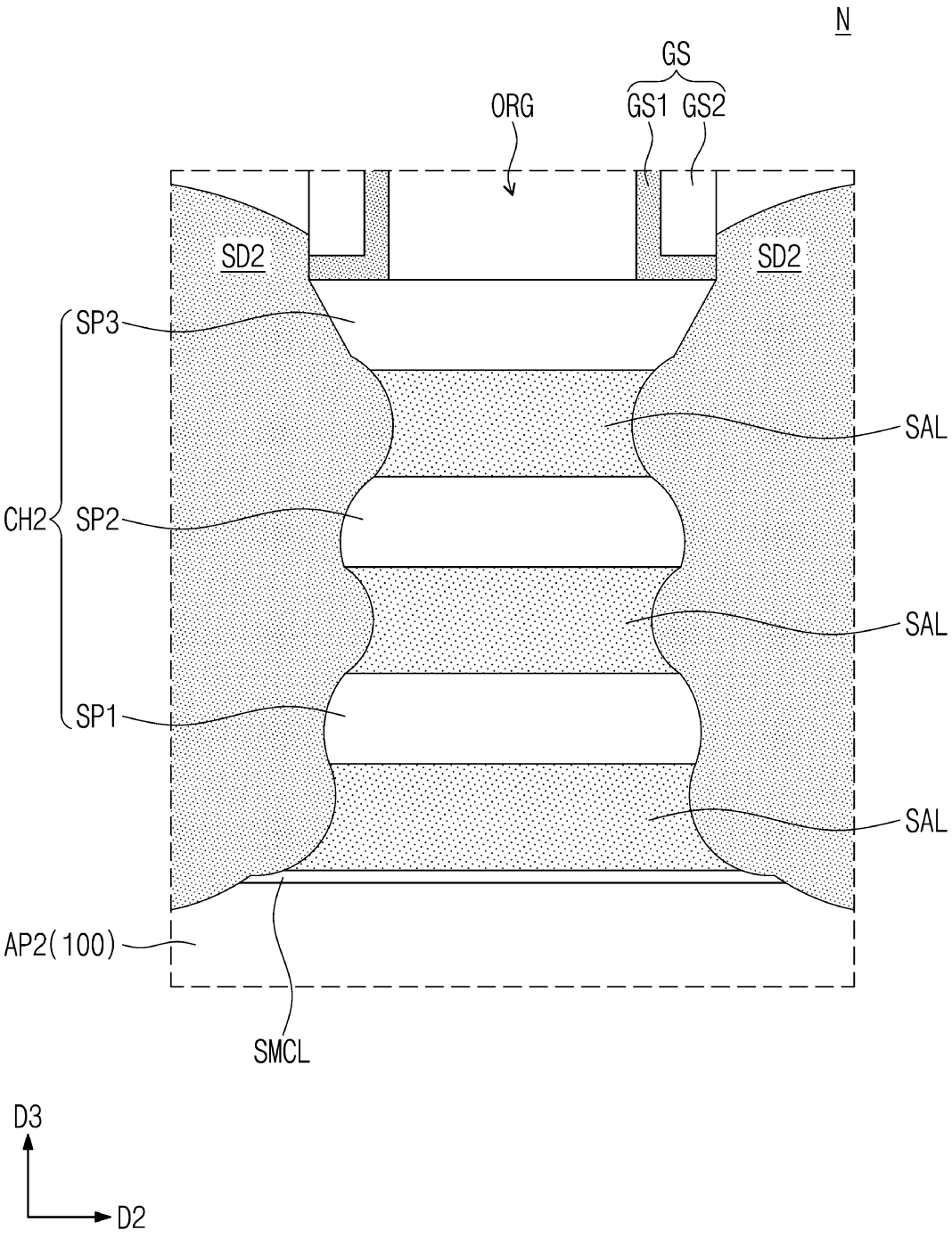

N
GS
ORG
GS1
GS2
SD2
SD2
SP3
SAL
CH2
SP2
SAL
SP1
SAL
AP2(100)
SMCL
D3
D2

FIG. 14A

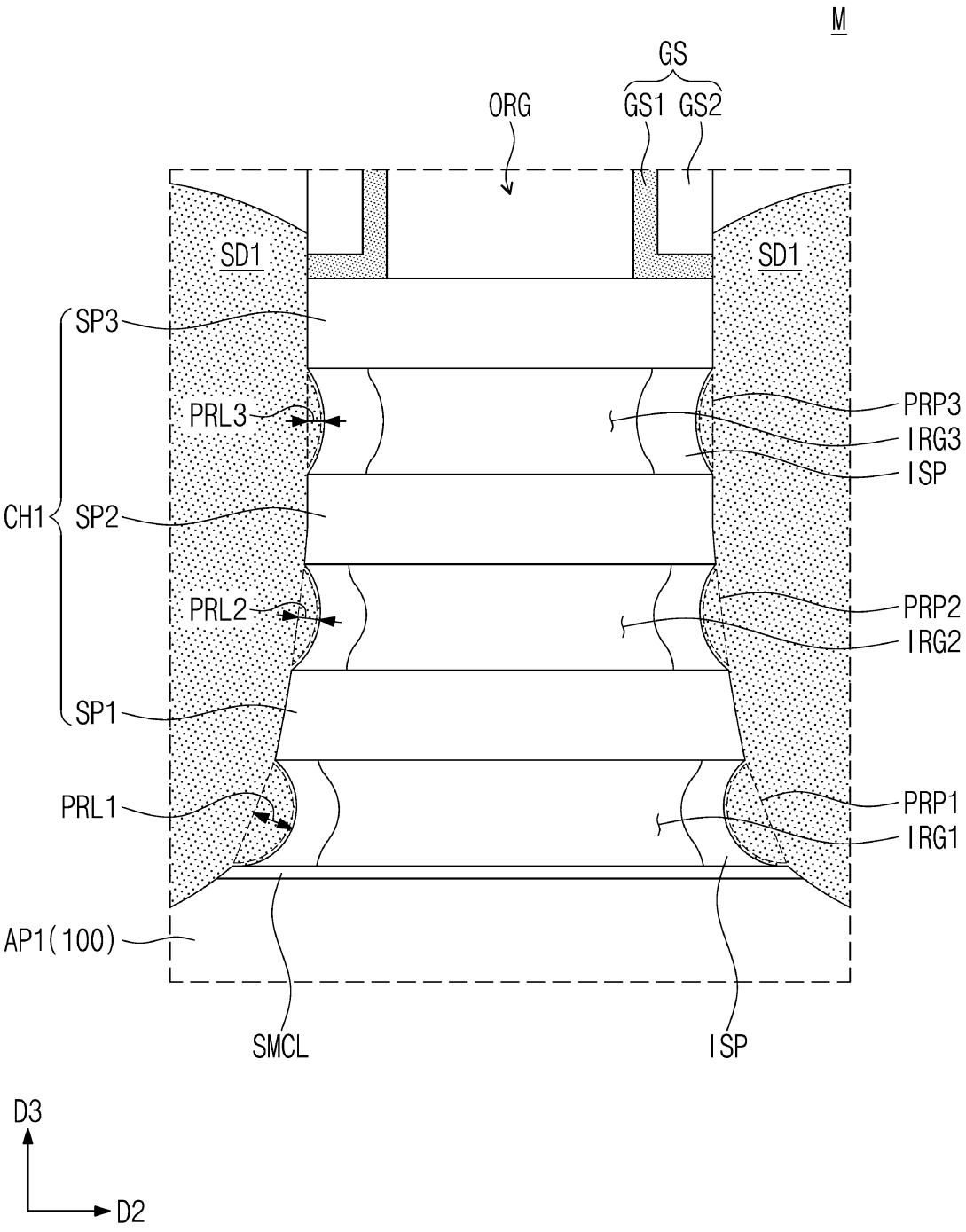

M
GS
ORG
GS1
GS2
SD1
SD1
SP3
PRL3
PRP3
IRG3
ISP
CH1
SP2
PRL2
PRP2
IRG2
SP1
PRL1
PRP1
IRG1
AP1(100)
SMCL
ISP
D3
D2

FIG. 14B

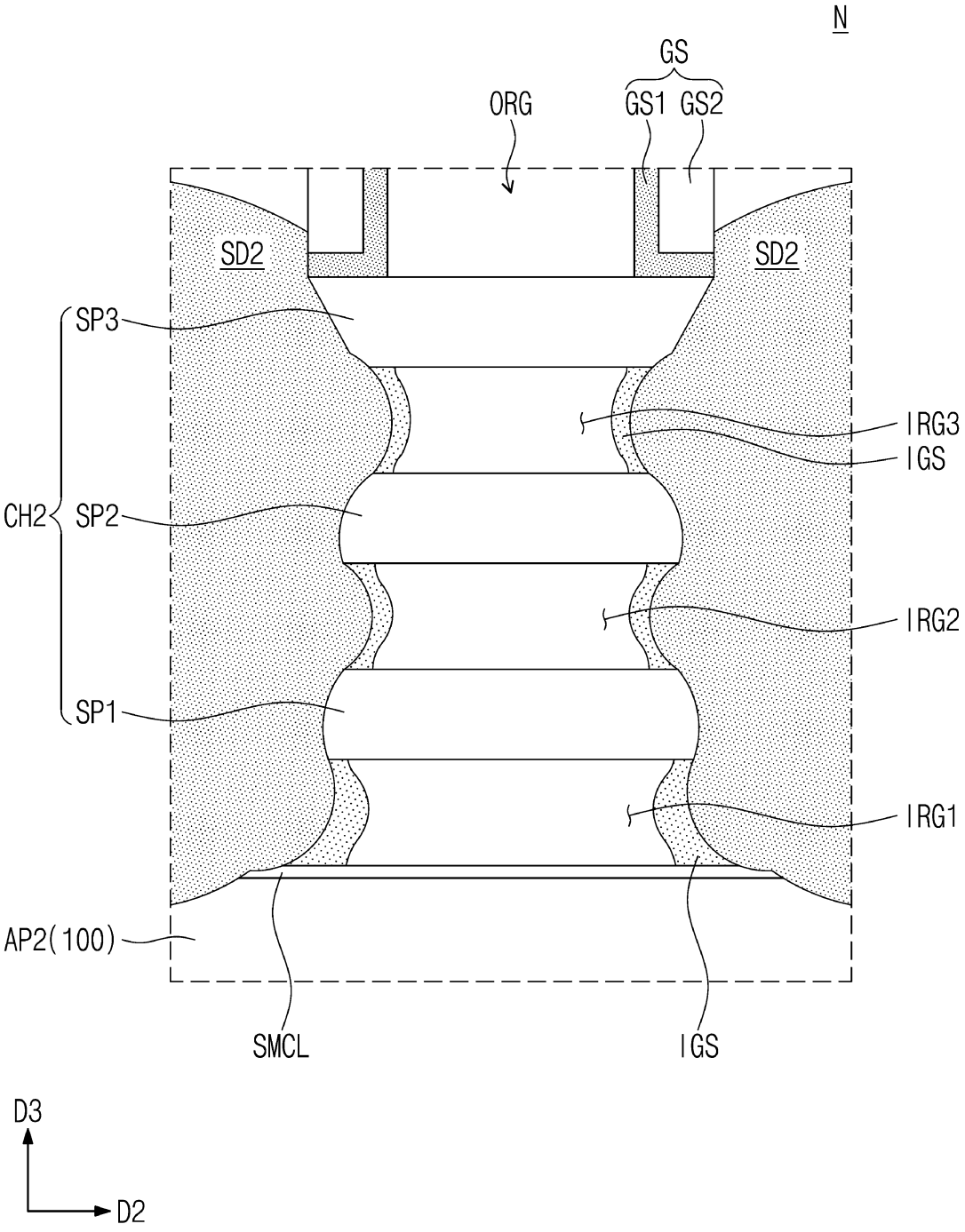

N
GS
ORG
GS1
GS2
SD2
SD2
SP3
IRG3
IGS
CH2
SP2
IRG2
SP1
IRG1
AP2(100)
SMCL
IGS
D3
D2

FIG. 15A

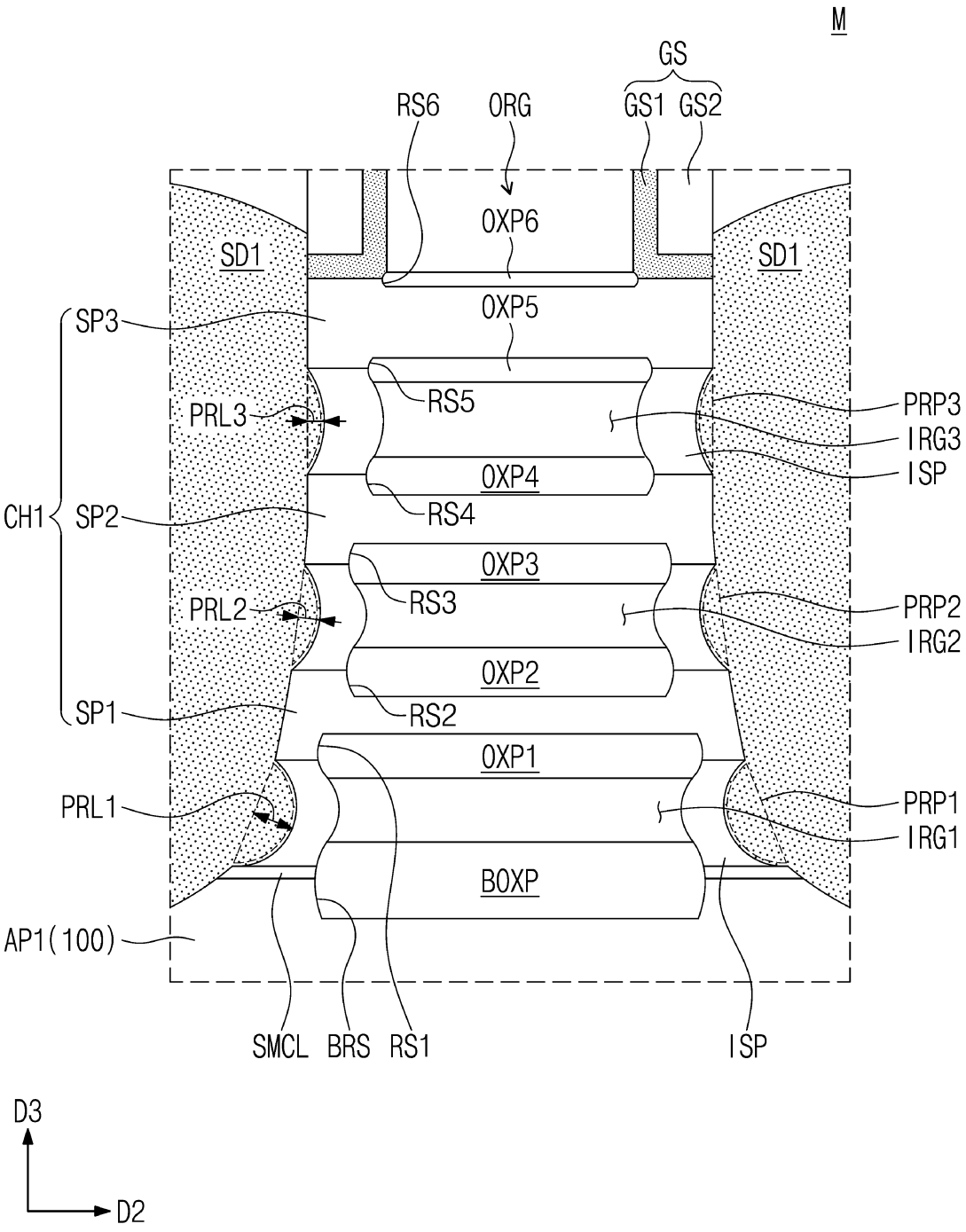

M
GS
GS1
GS2
RS6
ORG
OXP6
OXP5
OXP4
OXP3
OXP2
OXP1
BOXP
SD1
SD1
SP3
SP2
SP1
CH1
PRL3
PRL2
PRL1
RS5
RS4
RS3
RS2
PRP3
IRG3
ISP
PRP2
IRG2
PRP1
IRG1
AP1(100)
SMCL
BRS
RS1
ISP
D3
D2

FIG. 15B

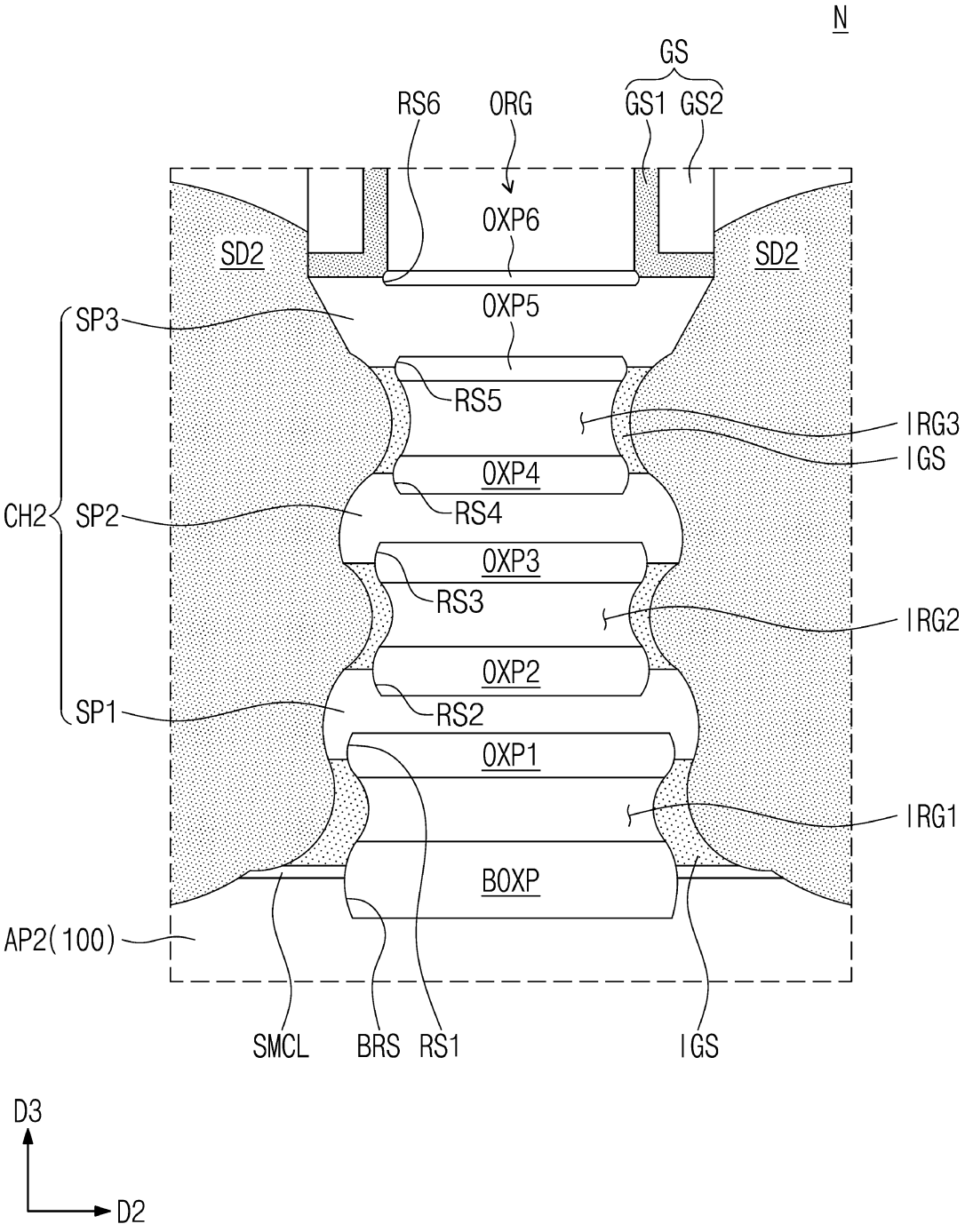

N
GS
RS6
ORG
GS1
GS2
OXP6
SD2
SD2
OXP5
SP3
RS5
IRG3
IGS
OXP4
CH2
SP2
RS4
OXP3
RS3
IRG2
OXP2
SP1
RS2
OXP1
IRG1
BOXP
AP2(100)
SMCL
BRS
RS1
IGS
D3
D2

FIG. 16A

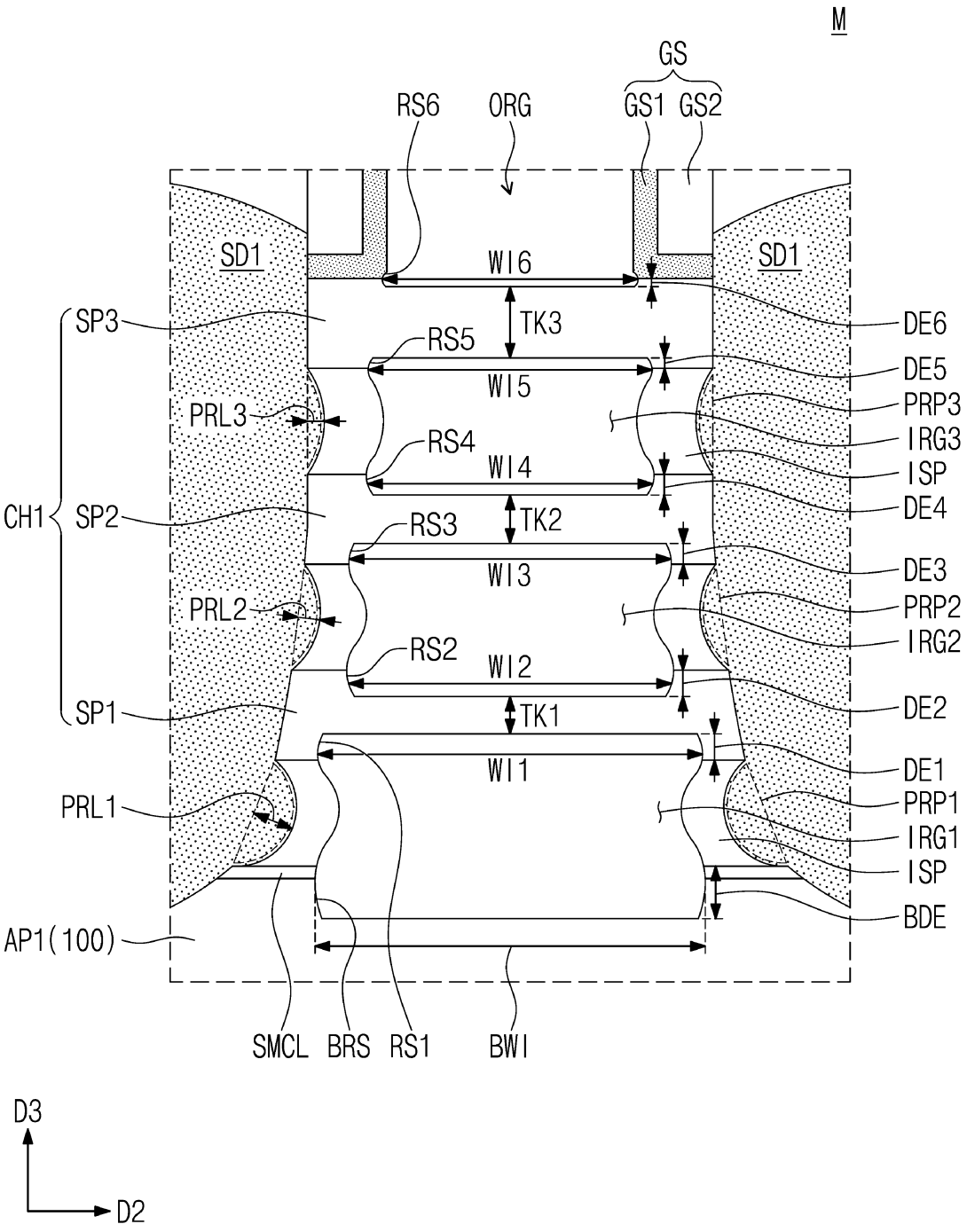

M
GS
RS6
ORG
GS1
GS2
SD1
SD1
WI6
TK3
RS5
WI5
SP3
DE6
DE5
PRL3
PRP3
IRG3
RS4
WI4
ISP
DE4
CH1
SP2
RS3
TK2
WI3
DE3
PRL2
PRP2
IRG2
RS2
WI2
SP1
TK1
DE2
WI1
DE1
PRL1
PRP1
IRG1
ISP
BDE
AP1(100)
SMCL
BRS
RS1
BWI
D3
D2

FIG. 16B

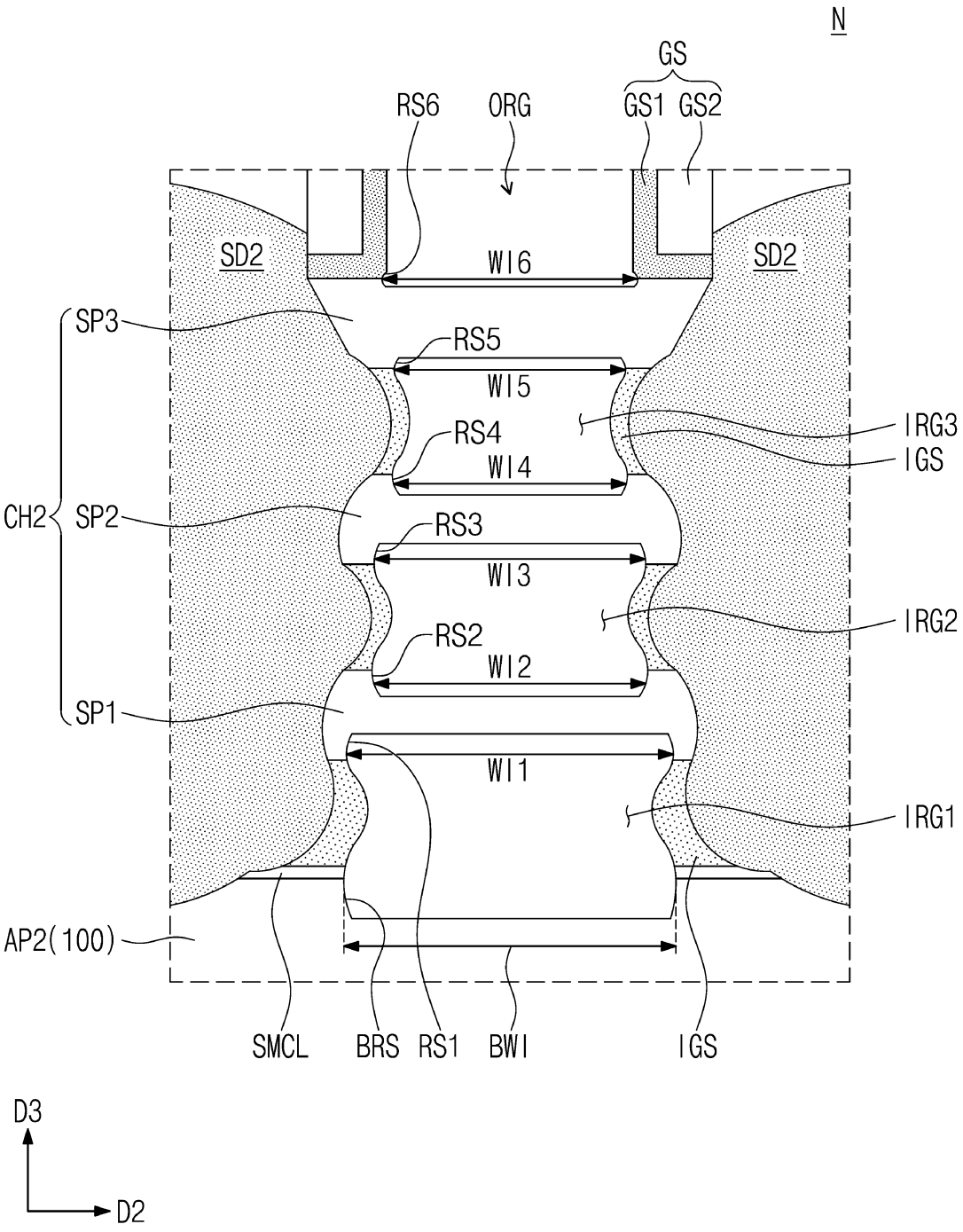

N
GS
RS6
ORG
GS1
GS2
SD2
SD2
WI6
SP3
RS5
WI5
IRG3
RS4
IGS
WI4
CH2
SP2
RS3
WI3
IRG2
RS2
WI2
SP1
WI1
IRG1
AP2(100)
SMCL
BRS
RS1
BWI
IGS
D3
D2

FIG. 17

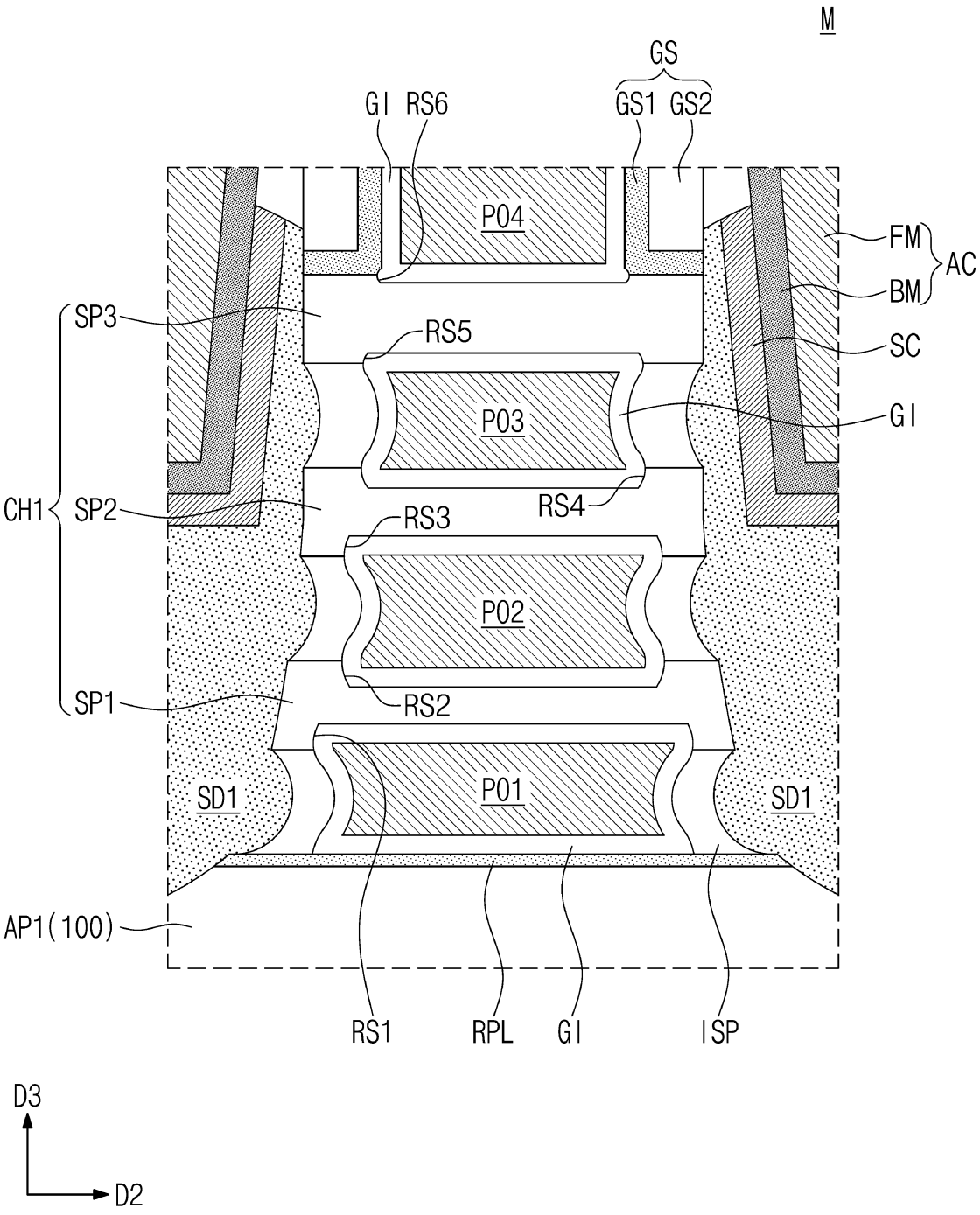

M
GS
GI
RS6
GS1
GS2
P04
FM
AC
BM
SC
SP3
RS5
P03
GI
CH1
SP2
RS4
RS3
P02
SP1
RS2
SD1
P01
SD1
AP1(100)
RS1
RPL
GI
ISP
D3
D2

FIG. 18

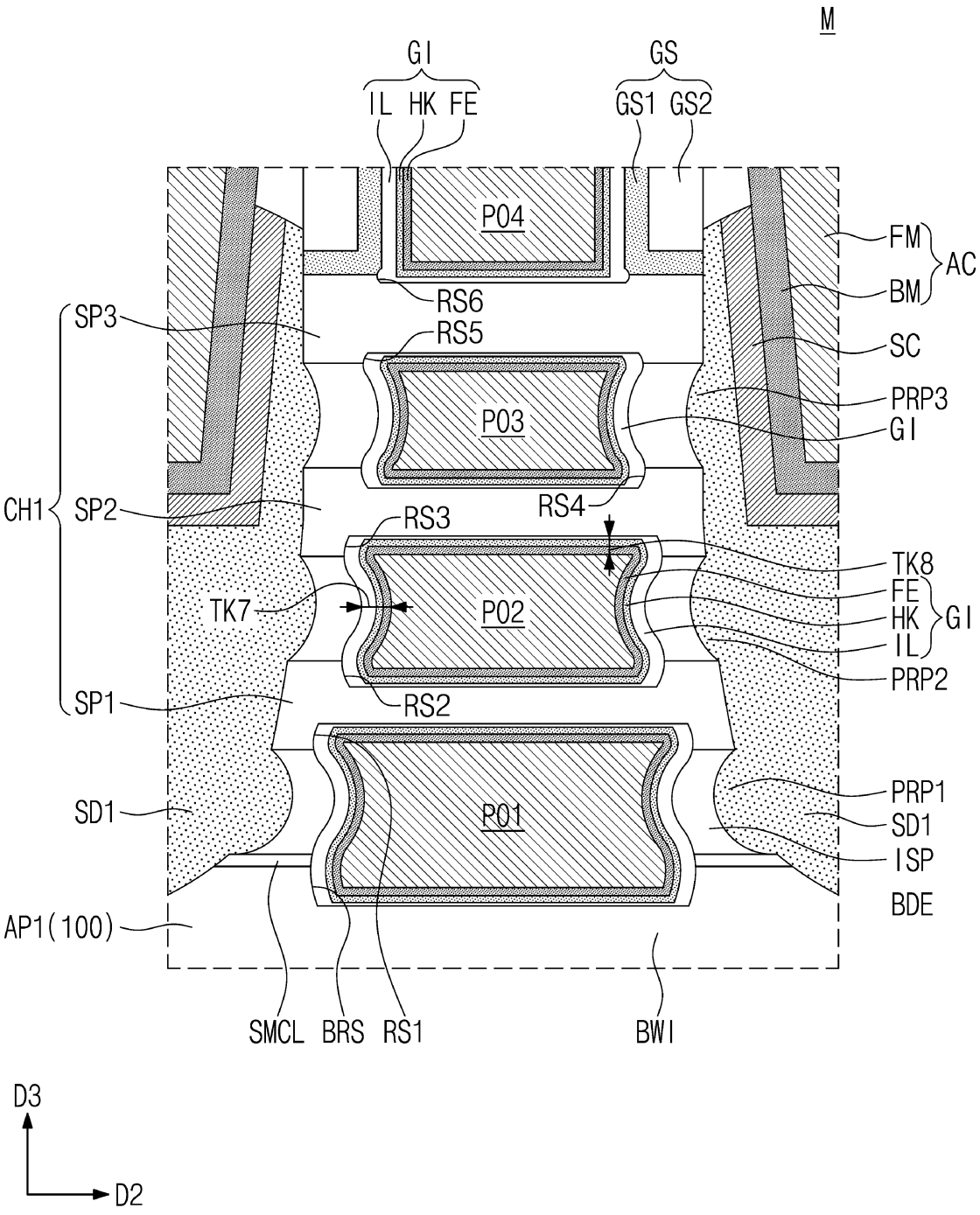

M
GI
IL HK FE
GS
GS1 GS2
P04
FM
AC
BM
RS6
SP3
RS5
SC
P03
PRP3
GI
CH1
SP2
RS4
RS3
TK8
FE
TK7
P02
HK
GI
IL
PRP2
SP1
RS2
PRP1
SD1
P01
SD1
ISP
BDE
AP1(100)
SMCL
BRS
RS1
BWI
D3
D2

FIG. 19

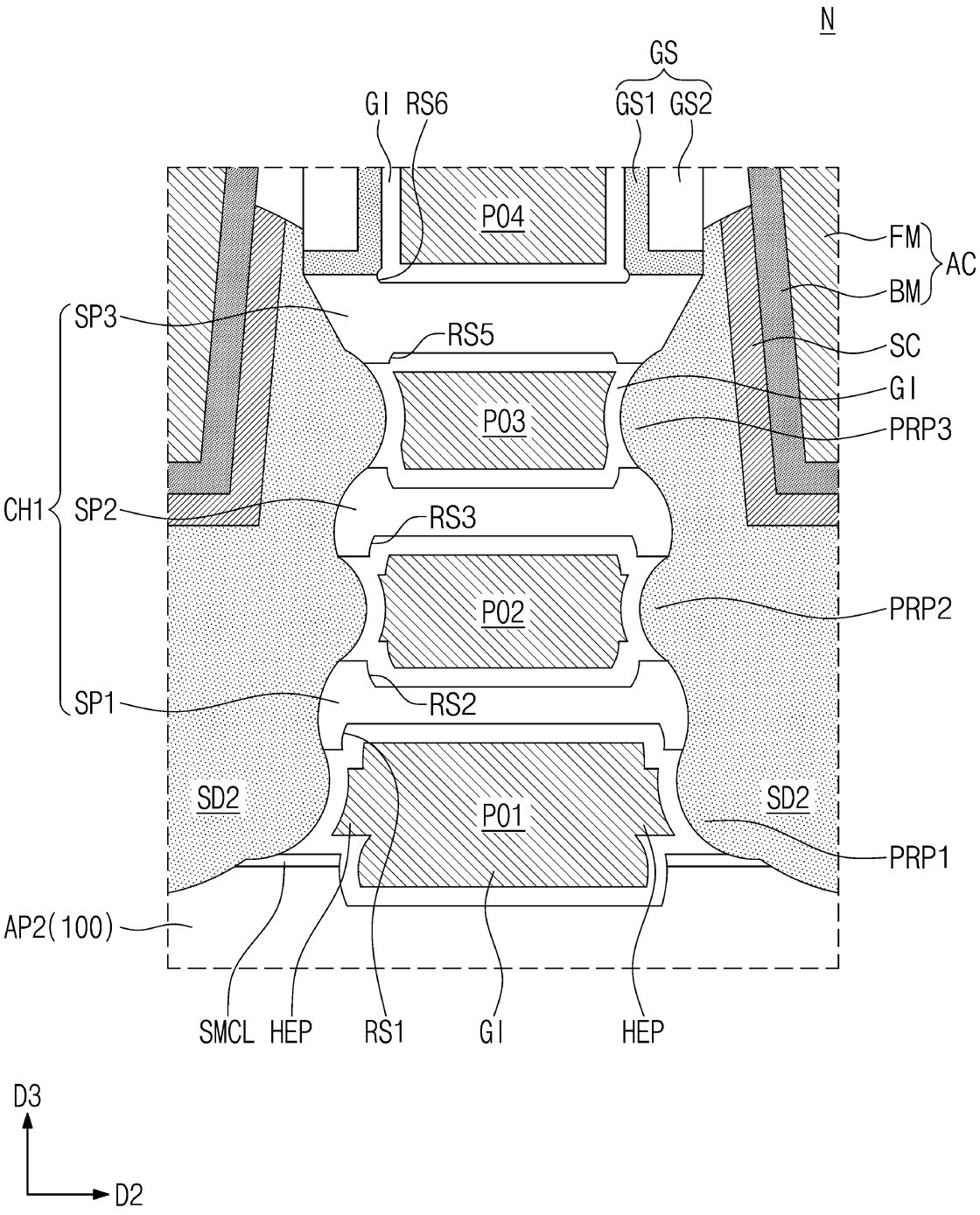

N
GS
GI
RS6
GS1
GS2
P04
FM
AC
BM
SP3
RS5
SC
GI
P03
PRP3
CH1
SP2
RS3
P02
PRP2
SP1
RS2
SD2
P01
SD2
PRP1
AP2(100)
SMCL
HEP
RS1
GI
HEP
D3
D2

FIG. 20

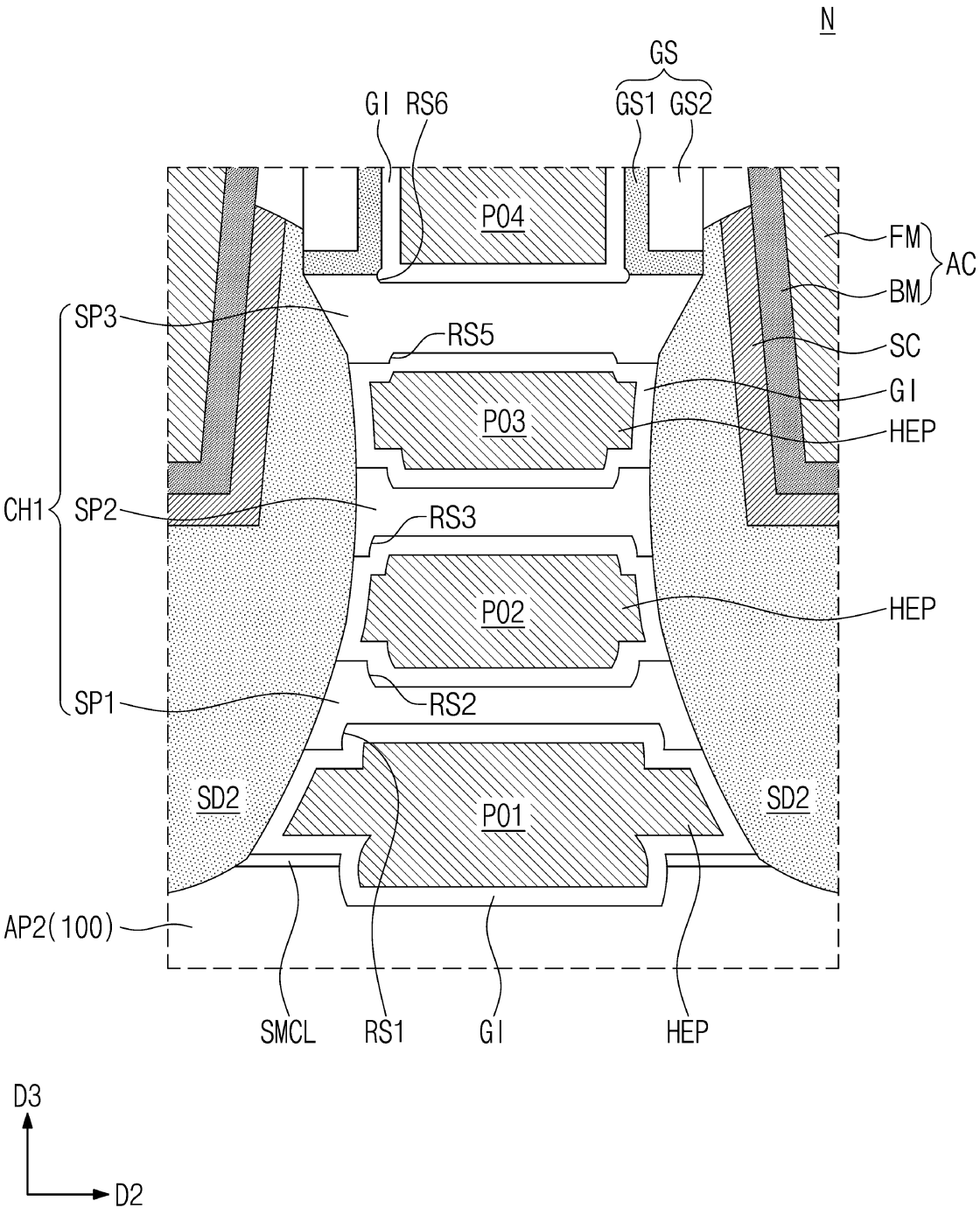

N
GS
GI
RS6
GS1
GS2
P04
FM
AC
BM
SP3
RS5
SC
GI
P03
HEP
CH1
SP2
RS3
P02
HEP
SP1
RS2
SD2
P01
SD2
AP2(100)
SMCL
RS1
GI
HEP
D3
D2

FIG. 21

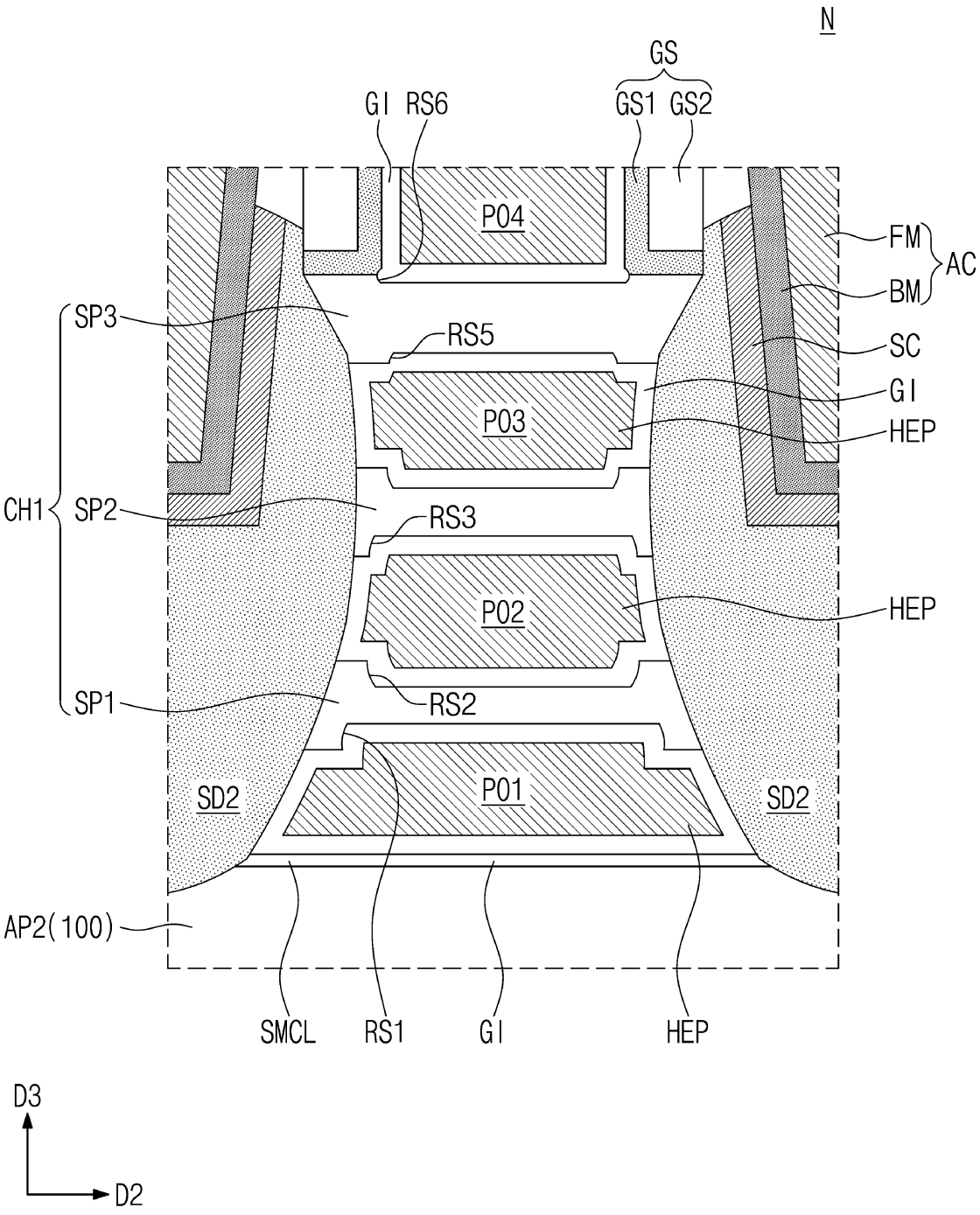

N
GS
GS1
GS2
GI
RS6
P04
FM
BM
AC
SP3
RS5
SC
GI
P03
HEP
CH1
SP2
RS3
P02
HEP
SP1
RS2
P01
SD2
SD2
AP2(100)
SMCL
RS1
GI
HEP
D3
D2

FIG. 22

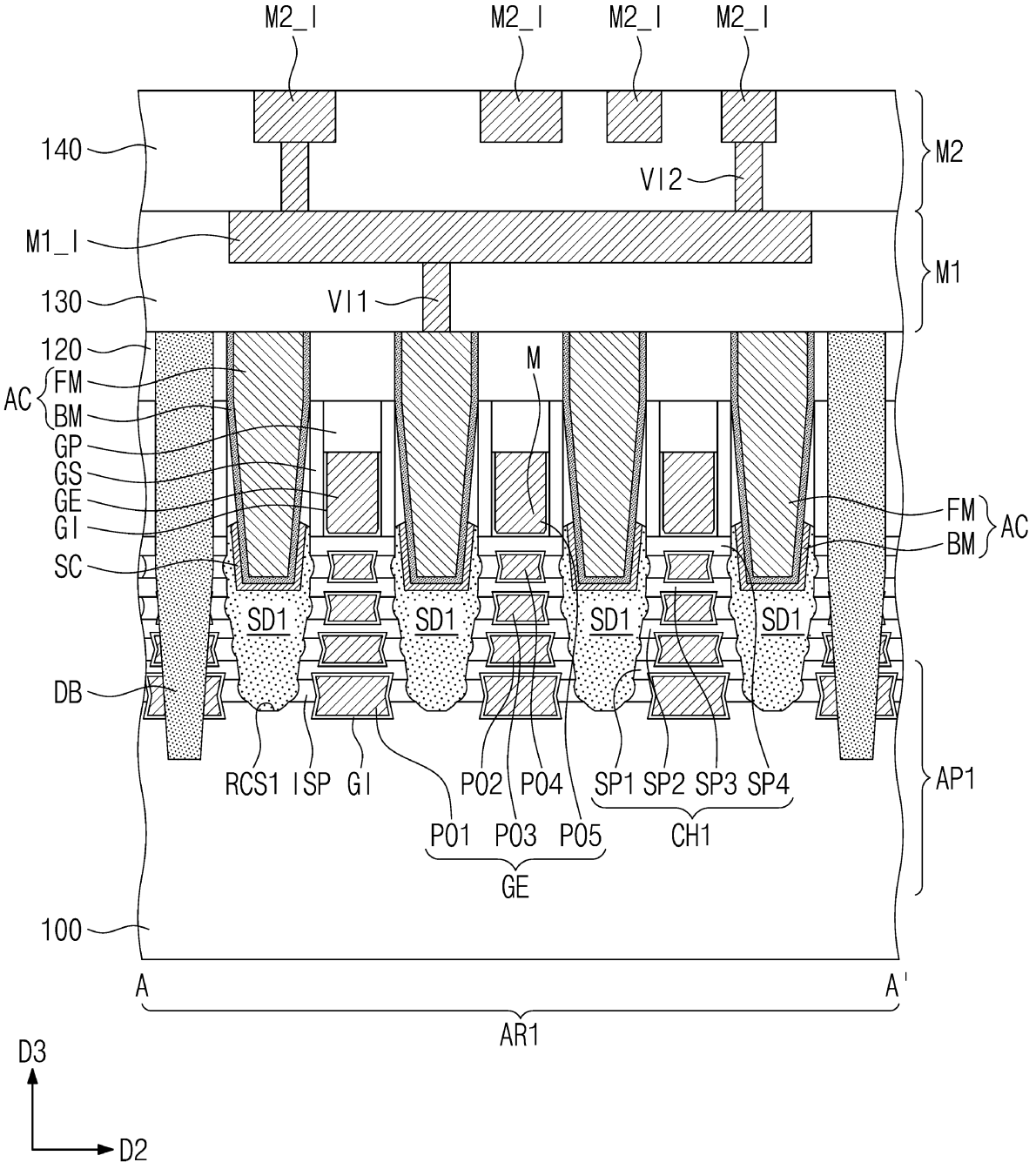

M2_I
M2_I
M2_I
M2_I
140
M2
VI2
M1_I
M1
130
VI1
120
M
AC
FM
BM
GP
GS
GE
GI
SC
FM
BM
AC
SD1
SD1
SD1
SD1
DB
AP1
RCS1
ISP
GI
P02
P04
SP1
SP2
SP3
SP4
P01
P03
P05
CH1
GE
100
A
A'
AR1
D3
D2

FIG. 23

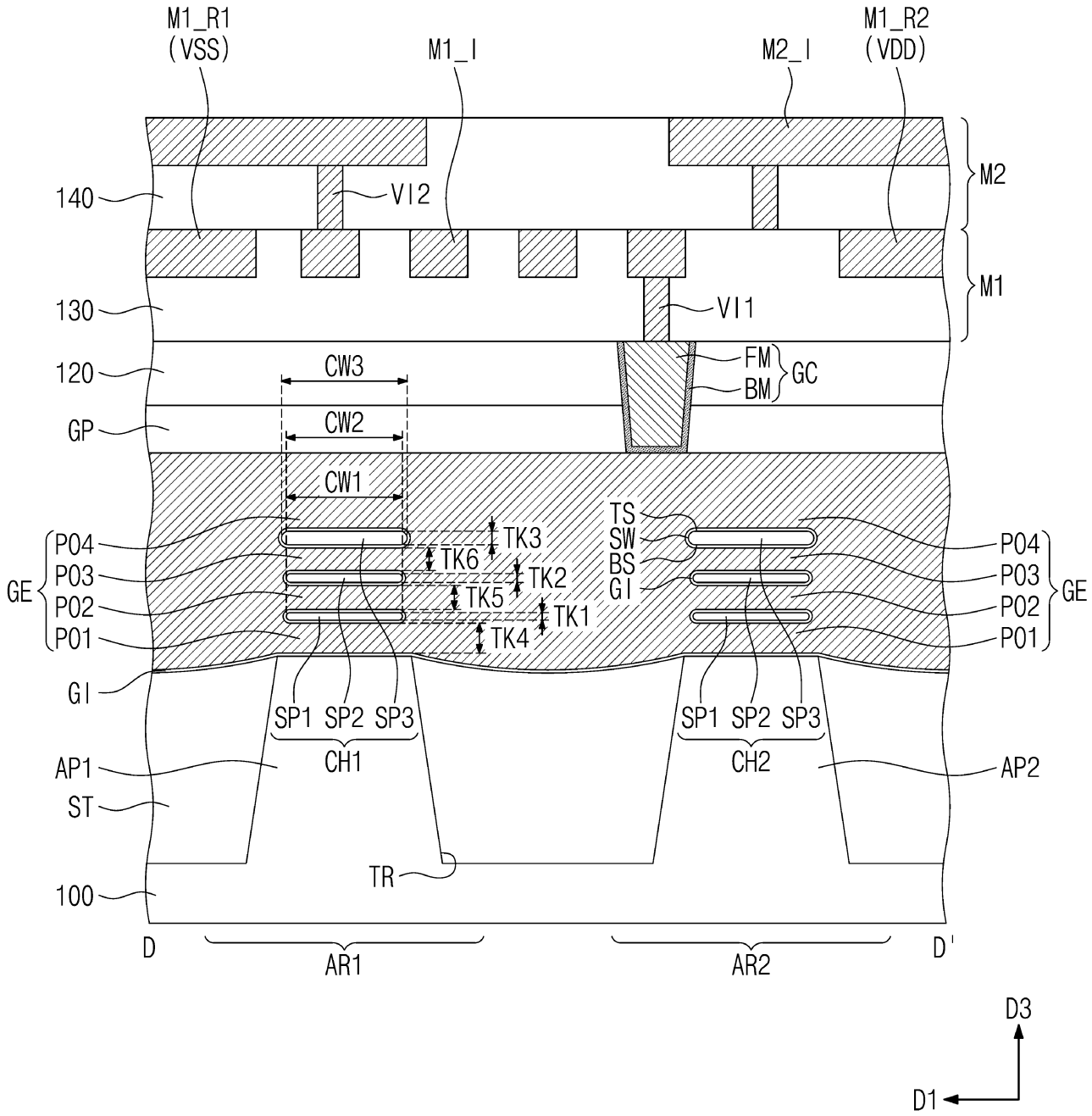

M1_R1
(VSS)
M1_I
M2_I
M1_R2
(VDD)
M2
M1
140
VI2
130
VI1
120
CW3
FM
BM
GC
GP
CW2
CW1
TS
SW
BS
GI
GE
P04
P03
P02
P01
TK3
TK6
TK2
TK5
TK1
TK4
SP1 SP2 SP3
CH1
CH2
AP1
AP2
ST
TR
100
D
D'
AR1
AR2
D3
D1

FIG. 24

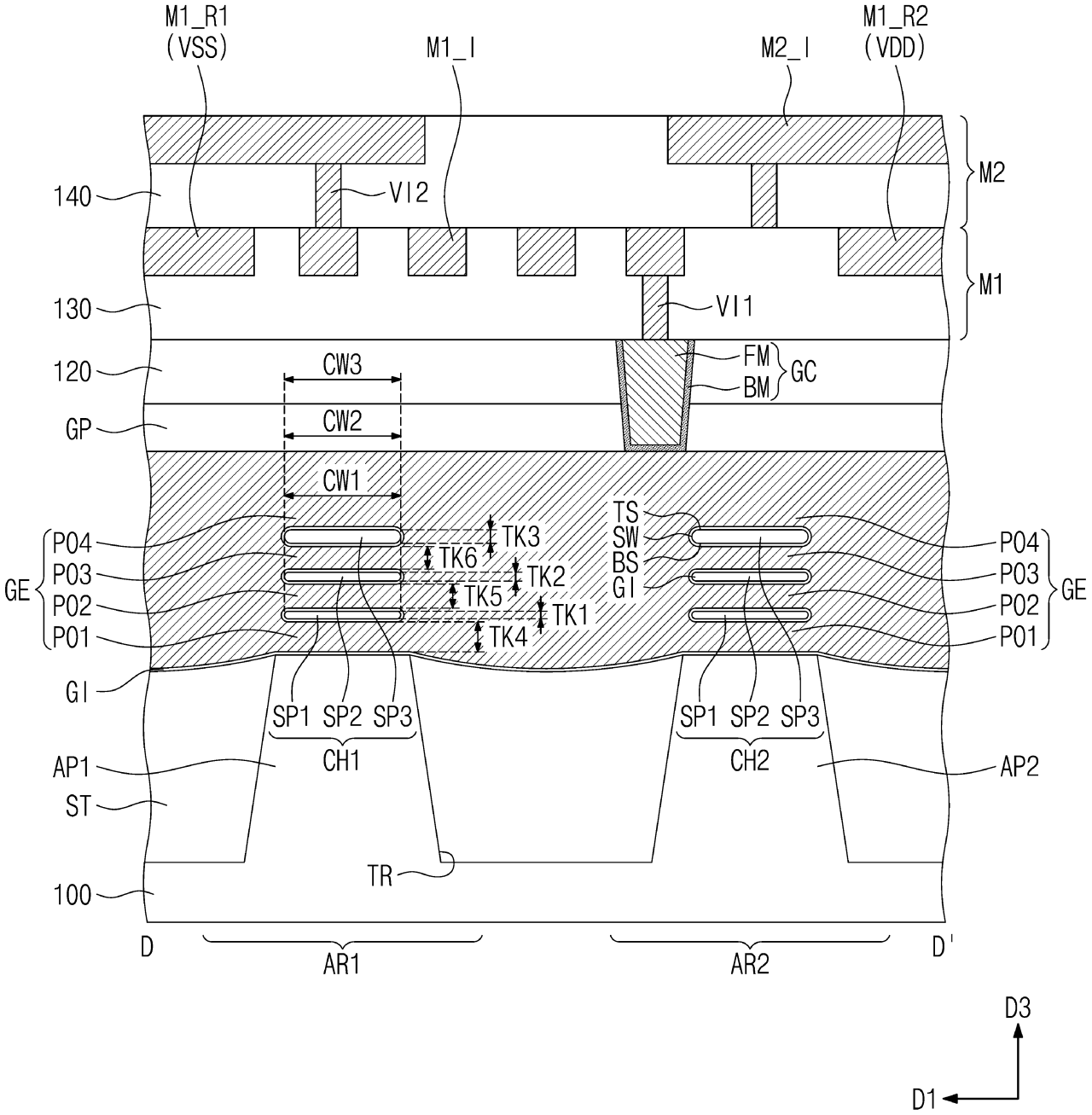
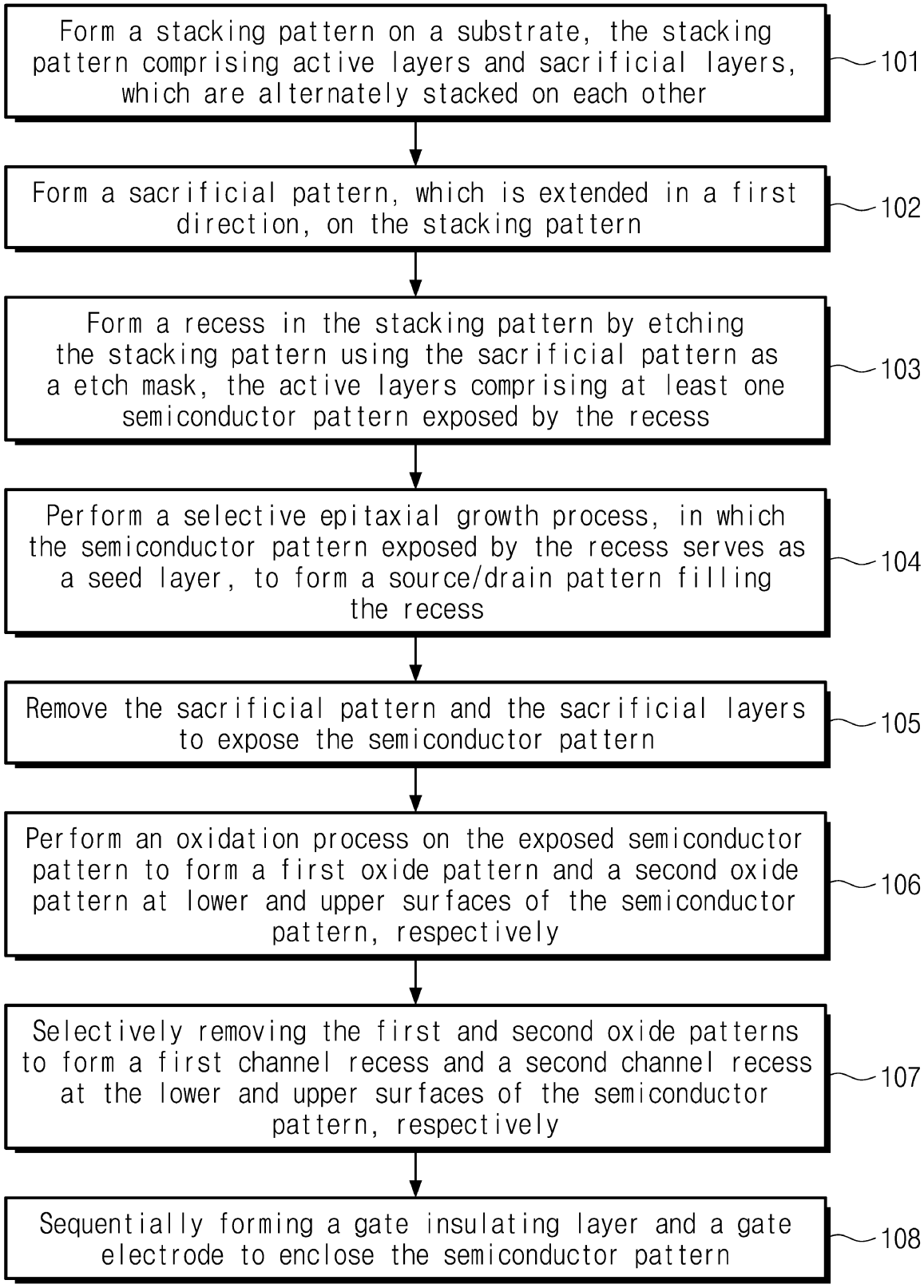

M1_R1
(VSS)
M1_I
M2_I
M1_R2
(VDD)
M2
M1
140
VI2
130
VI1
120
CW3
FM
BM
GC
GP
CW2
CW1
TS
SW
BS
GI
P04
P03
P02
P01
GE
TK3
TK6
TK2
TK5
TK1
TK4
SP1 SP2 SP3
CH1
CH2
AP1
AP2
ST
TR
100
D
D'
AR1
AR2
D3
D1

FIG. 25


Form a stacking pattern on a substrate, the stacking pattern comprising active layers and sacrificial layers, which are alternately stacked on each other
101
Form a sacrificial pattern, which is extended in a first direction, on the stacking pattern
102
Form a recess in the stacking pattern by etching the stacking pattern using the sacrificial pattern as a etch mask, the active layers comprising at least one semiconductor pattern exposed by the recess
103
Perform a selective epitaxial growth process, in which the semiconductor pattern exposed by the recess serves as a seed layer, to form a source/drain pattern filling the recess
104
Remove the sacrificial pattern and the sacrificial layers to expose the semiconductor pattern
105
Perform an oxidation process on the exposed semiconductor pattern to form a first oxide pattern and a second oxide pattern at lower and upper surfaces of the semiconductor pattern, respectively
106
Selectively removing the first and second oxide patterns to form a first channel recess and a second channel recess at the lower and upper surfaces of the semiconductor pattern, respectively
107
Sequentially forming a gate insulating layer and a gate electrode to enclose the semiconductor pattern
108