# FLIP CHIP PACKAGING USING RECESSED INTERPOSER TERMINALS

## TECHNICAL FIELD

The present invention relates to methods and apparatus for assembling and packaging single and multiple semiconductor dice with an interposer substrate. In particular, the present invention relates to methods and apparatus for assembling and packaging single and multiple semiconductor dice in a flip chip orientation with an interposer substrate.

## BACKGROUND ART

Chip-On-Board ("COB") or Board-On-Chip ("BOC") technology is used to attach a semiconductor die directly to a carrier substrate such as a printed circuit board ("PCB"), or an interposer may be employed and attachment may be effected using flip chip attachment, wire bonding, or tape automated bonding ("TAB").

Flip chip attachment generally includes electrically and mechanically attaching a semiconductor die by its active surface to an interposer or other carrier substrate using a pattern of discrete conductive elements therebetween. The discrete conductive elements are generally disposed on the active surface of the die during fabrication thereof, but may instead be disposed on the carrier substrate. The discrete conductive elements may comprise minute conductive bumps, balls or columns of various configurations. Each discrete conductive element is placed corresponding to mutually aligned locations of bond pads (or other I/O locations) on the semiconductor die and terminals on the carrier substrate when the two components are superimposed. The semiconductor die is thus electrically and mechanically connected to the carrier substrate by, for example, reflowing conductive bumps of solder or curing conductive or conductor-filled epoxy bumps. A dielectric underfill may then be disposed between the die and the carrier substrate for environmental protection and to enhance the mechanical attachment of the die to the carrier substrate.

Wire bonding and TAB attachment techniques generally begin with attaching a semiconductor die by its back side to the surface of a carrier substrate with an appropriate adhesive, such as an epoxy or silver solder. In wire bonding, a plurality of

fine wires are discretely attached to bond pads on the semiconductor die and then extended and bonded to corresponding terminal pads on the carrier substrate. A dielectric encapsulant such as a silicone or epoxy may then be applied to protect the fine wires and bond sites. In TAB, ends of metal traces carried on a flexible insulating tape such as a polyimide are attached, as by thermocompression bonding, directly to the bond pads on the semiconductor die and corresponding terminal pads on the carrier substrate.

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. As new generations of integrated circuit products are released, the number of components used to fabricate them tends to decrease due to advances in technology even though the functionality of the products increase. For example, on the average, there is approximately a ten percent decrease in components for every product generation over the previous generation having equivalent functionality.

Recent trends in packaging are moving with increasing rapidity toward flip chip attachment due to improved electrical performance and greater packaging density. However, flip chip attachment is not without problems, such as the high cost for a third metal reroute of bond pads from the middle or periphery of a die to a two-dimensional array which, in turn, may result in overlong and unequal length electrical paths. In addition, many conventional flip chip techniques exhibit a lack of consistent reliability of the interconnections between the chip and the interposer or other carrier substrate as a result of the increased miniaturization as well as difficulties in mutual alignment of the die and carrier substrate to effect such interconnections. Effective rerouting of bond pads may also be limited by die size.

Further, flip chip packages for a bumped semiconductor die employing an interposer may be undesirably thick due to the combined height of the die and interposer. This is due to the use in conventional packaging techniques of relatively costly interposers comprising dual conductive layers having a dielectric member sandwiched therebetween, the bumped semiconductor die resting on and connected to traces of the conductive layer on one side of the interposer and electrically connected to traces of the conductive layer on the opposing side, conductive vias extending therebetween. Finally, underfilling a flip chip attached semiconductor die to a carrier substrate with dielectric filler material can be a lengthy and often unreliable process, and

the presence of the underfill makes reworking of defective assemblies difficult if not impossible.

Other difficulties with conventional packages include an inability to accommodate die size reductions, or "shrinks," as a given design progresses through several generations without developing new interposer designs and tooling. As more functionality is included in dice, necessitating a greater number of inputs and outputs (I/Os), decreased spacing or pitch between the I/Os places severe limitations on the use of conventional interposers. In addition, with conventional packages, a die is not tested until package assembly is complete, resulting in excess cost since a defective die or die and interposer assembly is not detected until the package is finished.

For example, United States Patent 5,710,071 to Beddingfield et al. discloses a fairly typical flip chip attachment of a semiconductor die to a substrate and a method of underfilling a gap between the semiconductor die and substrate. In particular, the semiconductor die is attached face down to the substrate, wherein conductive bumps on the die are directly bonded to bond pads on the upper surface of the substrate, which provides the gap between the die and substrate. The underfill material flows through the gap between the semiconductor die and the substrate via capillary action toward an aperture in the substrate, thereby expelling air in the gap through the aperture in the substrate in an effort to minimize voids in the underfill material. However, such an underfilling method still is unnecessarily time consuming due to having to underfill the entire semiconductor die. Further, the flip chip attachment technique disclosed in United States Patent 5,710,071 exhibits difficulties in aligning the conductive bumps with the bond pads on the substrate and requires the expense of having a third metal reroute in the substrate.

Therefore, it would be advantageous to improve the reliability of interconnections between a chip and a carrier substrate such as an interposer by achieving accurate alignment of the interconnections, an improved underfill process, and the elimination of the necessity for a third metal reroute, while reducing total assembly height in combination with the ability to employ commercially-available, widely-practiced semiconductor device fabrication techniques and materials.

## DISCLOSURE OF INVENTION

The present invention relates to methods and apparatus for assembling and packaging individual and multiple semiconductor dice with a carrier substrate in a flip chip type arrangement. The present invention provides a flip chip semiconductor assembly substantially reduced in height or depth in comparison to conventional interposer-based flip chip assemblies and with improved mechanical and electrical reliability of the interconnections between a semiconductor die and a carrier substrate in the form of an interposer, while also improving ease of alignment for attaching the semiconductor die to the carrier substrate and eliminating the requirement for a third metal reroute as well as reducing the time for optional dielectric underfilling of the flip chip assembly.

The flip chip semiconductor device assembly of the present invention includes a conductively bumped semiconductor die assembled active surface, or face, down with an interposer substrate. The present invention includes multiple recesses formed from one surface of the interposer substrate and through the dielectric layer thereof to conductive terminals or traces on the opposing surface, the recesses configured in a predetermined recess pattern that corresponds substantially with the bond pad, and hence conductive bump, pattern or configuration of the bumped semiconductor die. Such predetermined recess patterns may include, for example, a single or double row center bond pad configuration, an I-shaped bond pad configuration and a peripheral bond pad configuration.

An adhesive element may be optionally disposed between the semiconductor die and interposer substrate to mutually secure same, in addition to any bond between the conductive bumps and terminals or traces. The adhesive element may comprise a tape having a thickness, which may be used to provide and control a vertical standoff between the active surface and the interposer substrate and to increase compliancy of the attachment of the semiconductor die and interposer substrate as well as facilitating rework. In addition, the adhesive element assists to resolve minor variances in vertical travel of die pick-and-place equipment used to place a semiconductor die on the interposer substrate, and helps maintain the die securely in position on the interposer substrate during subsequent handling, fabrication steps and transportation from one location to another.

The flip chip semiconductor device assembly is assembled so that the conductive bumps on the semiconductor die are disposed in the recesses formed in the interposer substrate, the recesses being sized and configured to receive and the bumps on the bumped semiconductor die so that they are submerged within the recesses to an extent that the active surface of the semiconductor die may sit directly against the surface of the interposer substrate onto which the recesses open. Thus, there is a reduction in the height of the flip chip semiconductor device assembly relative to conventional interposer-based flip chip assemblies due to the disposition of the conductive bumps within the recesses, which allows for the conductive bumps on the semiconductor die to be of larger size for increased reliability without increasing the overall height or depth of the flip chip semiconductor device assembly while avoiding the need for a third metal reroute on the semiconductor die. Even if an adhesive element using a tape is employed, the conductive bumps may still be substantially completely received within the recesses, but for the small vertical standoff provided by the tape.

The conductive bumps may be bonded to the conductive terminals at the bottoms of the recesses by reflowing the bumps, curing the bumps, ultrasonic bonding of the bumps to the terminals, thermal compression bonding of the bumps to the terminals, or by other techniques known in the art, depending upon the bump material selected. Further, a conductive paste or other non-solid conductive material may be provided on the bumps or within the recesses prior to disposing the bumps in the recesses. Alternatively, bumps in the form of solder balls may be disposed in the recesses prior to alignment of the semiconductor die with the interposer substrate, or higher melting point metal or alloy bumps provided in a conductive paste in the recesses or on the bumps, after which the die may be aligned with the interposer substrate and attached thereto. In addition to enhancing electrical connection reliability between the conductive bumps and the interposer terminals, a non-solid conductive material may be used to compensate for any non-coplanarity between the semiconductor die and interposer substrate due to varied bump sizes, recess depths and planarity variation in the opposing, adjacent surfaces of the semiconductor die and interposer substrate. As noted, an adhesive element on the surface of the interposer substrate facing the semiconductor die may be used in some embodiments as a height controller and may also help compensate for any

irregularities in the coplanarity between the semiconductor die and the interposer substrate.

The semiconductor device assembly of the present invention may also be configured with one or more openings extending through the interposer substrate at a location or locations from the surface facing away from the semiconductor die to provide communication between the one or more openings to each of the multiple recesses in the interposer substrate. This configuration facilitates dispensing of dielectric filler material through the opening or openings into the recesses and around the bumps. The opening or openings may be substantially coincident with the configuration of recesses and comprise gaps between conductive pad or terminal portions of conductive traces extending across the recessed or may comprise slots over or laterally offset from the recesses and in communication therewith, and if offset, a side of each recess being open to the slot. In the first and second instances, dielectric filler material may be introduced directly into the recesses through the gaps between the sides of the conductive trace extending over each recess and the periphery of the recess wall adjacent the trace. In the latter instance, dielectric filler material may be introduced into the slots to travel laterally therefrom into the recesses. Further, if a vertical standoff is employed between the interposer substrate and the semiconductor die, dielectric filler material may be introduced through a slot or other opening through the interposer substrate in the center region of the and caused to flow therefrom into the recesses through the mouths thereof, even if not in communication with the opening, and to the periphery of the semiconductor die (if desired) through the standoff. This aspect of the present invention substantially enhances underfill integrity while decreasing process time.

The flip chip semiconductor device assembly of the present invention may also include solder balls or other discrete external conductive elements attached to the conductive traces extending from the terminals over the surface of the interposer substrate facing away from the semiconductor die. The discrete external conductive elements are employed to interconnect the semiconductor device assembly with higher level packaging such as a carrier substrate, for example, in the form of a printed circuit board. The semiconductor die of the flip chip semiconductor device assembly may fully or partially encapsulated by a dielectric encapsulation material or may be left exposed.

In another aspect of the present invention, a heat transfer element may be included with the flip chip semiconductor device assembly. In particular, the heat transfer element may be included on the surface of the interposer substrate facing the semiconductor die, the active surface of the semiconductor die, or the back side of the semiconductor die. Such heat transfer element may be used to lower the operating temperature of the assembly as well as to prevent thermal fatigue.

The flip chip semiconductor device assembly of the invention may include an unencapsulated semiconductor die, a partially encapsulated semiconductor die, or a fully encapsulated semiconductor die.

The interposer substrate of the present invention may also be assembled with a plurality of semiconductor dice at a wafer or partial wafer level, wherein a wafer or partial wafer including a plurality of unsingulated semiconductor dice is attached face down to a like-sized interposer substrate with bumps on the wafer or partial wafer submerged in recesses formed in the interposer substrate. Filler material may be dispensed through openings in the interposer substrate, after which the wafer or partial wafer and interposer substrate may be diced into individual flip chip semiconductor device assemblies. Encapsulation may be performed at least partially at the wafer level and completed, if desired, after being diced into individual semiconductor assemblies.

The interposer substrate may be fabricated from a flexible material including a flexible dielectric member, a conductive member, an adhesive on the flexible dielectric member and a solder mask over the conductive member. The flexible dielectric member may comprise a polyimide layer which overlies the solder mask with the conductive member therebetween. The conductive member comprises a pattern of conductive traces formed by etching of a conductive layer carried by the flexible dielectric member or by printing traces on the flexible dielectric member using conductive ink. Trace ends may be enlarged at the intended locations of the recesses to define pads for the terminals and the traces extend therefrom to enlarged bump pads sized and placed for formation of external conductive elements thereon for connection to higher level packaging. The recesses may be formed through the flexible dielectric member from the surface thereof opposite the conductive member by etching, mechanical drilling or punching or laser ablation, wherein each of the recesses extend to a terminal of a conductive trace and is sized and configured to receive a conductive bump of the semiconductor die. The

flexible dielectric member may also optionally include another patterned conductive layer thereon over the surface of the flexible dielectric member to face the semiconductor die. The interposer substrate of the present invention may also be formed of other interposer substrate materials such as a BT resin, FR4 laminate, FR5 laminate and ceramics.

In another aspect of the present invention, the flip chip semiconductor device assembly is mounted to a circuit board in a computer or a computer system. In the computer system, the circuit board is electrically connected to a processor device which electrically communicates with an input device and an output device.

Other features and advantages of the present invention will become apparent to those of skill in the art through a consideration of the ensuing description, the accompanying drawings and the appended claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention may be ascertained from the following description of the invention when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a simplified top view of an interposer substrate having recesses therein in a center row configuration according to the present invention;

FIG. 1A is simplified bottom view of another interposer substrate design for a center row configuration according to the present invention;

FIG. 2 is a simplified cross-sectional side view taken along line 2 in FIG. 1;

FIG. 3 is a simplified cross-sectional side view take along line 3 in FIG. 1;

FIGS. 4A - 4C illustrate an interposer substrate and a method of forming recesses therein according to the present invention;

FIGS. 5A - 5D illustrate another interposer substrate and a method of forming recesses therein according to the present invention;

FIGS. 6A - 6B illustrate a first method of mounting a semiconductor die face down to an interposer substrate in a flip chip type semiconductor assembly according to the present invention;

FIGS. 7A - 7B illustrate a second method of mounting a semiconductor die face down to an interposer substrate in a flip chip semiconductor device assembly according to the present invention;

FIGS. 8A - 8D illustrate a third method of mounting a semiconductor die face down to an interposer substrate in a flip chip semiconductor device assembly according to the present invention;

FIGS. 9A - 9B illustrate a variant of the third method of mounting a semiconductor die face down to an interposer substrate in a flip chip semiconductor device assembly according to the present invention;

FIG. 10 illustrates dispensing filler material through an opening in an interposer substrate in a flip chip semiconductor device assembly according to the present invention to fill recesses therein;

FIG. 11 illustrates encapsulating a semiconductor die in a flip chip semiconductor device assembly and attaching the flip chip semiconductor device assembly according to the present invention to another substrate via solder balls;

FIG. 12 illustrates a cross-sectional side view of a flip chip semiconductor device assembly including a heat transfer element according to the present invention;

FIGS. 13A - 13B illustrate a method of assembling the flip chip semiconductor device assembly according to the present invention at a wafer level, wherein: FIG. 13A illustrates a wafer face down prior to being attached to a wafer scale interposer substrate of the present invention; and FIG. 13B illustrates the wafer attached face down to the wafer scale interposer substrate;

FIG. 14 illustrates a simplified top view of an interposer substrate having recesses therein in an I-shaped configuration according to the present invention;

FIG. 15 illustrates a simplified top view of an interposer substrate having recesses therein in a peripheral configuration according to the present invention;

FIG. 16 illustrates underfilling and encapsulating a flip chip type semiconductor assembly wherein the bumps on the semiconductor die and the recesses formed in the interposer substrate are arranged in a peripheral configuration according to the present invention;

FIG. 17 is a simplified block diagram of the flip chip type semiconductor assembly of the present invention integrated in a computer system;

FIG. 18 depicts an approach to implementation of the present invention using a non-flow dielectric filler material placement; and

FIGS. 19 through 21 depict exemplary multiple semiconductor die, folded interposer substrate embodiments of the present invention.

## BEST MODE OR MODES FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will be hereinafter described with reference to the accompanying drawings. It would be understood that these illustrations are not to be taken as actual views of any specific apparatus or method of the present invention, but are merely exemplary, idealized representations employed to more clearly and fully depict the present invention than might otherwise be possible. Additionally, elements and features common between the drawings figures retain the same numerical designation.

FIG. 1 depicts a simplified top plan view of an interposer substrate 110. The interposer substrate 110 is preferably, but not limited to, a flexible substrate, which may include a dielectric substrate member 111 and a protective solder mask 118. The dielectric substrate member 111 may define a first surface 112 of the interposer substrate 110 and the solder mask 118 may define a second surface 114 of the interposer substrate 110.

The interposer substrate 110 may be formed from any known substrate material and is preferably formed of, by way of example, a flexible laminated polymer or polyimide layer, such as UPILEX, produced by Ube Industries Ltd., or any other polymer-type layer. The interposer substrate 110 may also be made of a bismaleimide triazine (BT) resin, FR 4, FR 5 or any type of substantially non-flexible material, such as a ceramic or epoxy resin.

According to the present invention, the first surface 112 of interposer substrate 110 includes multiple recesses or vias 120 formed therein and having mouths 120m opening thereonto in a preselected pattern and of a predetermined size and shape. The multiple recesses or vias 120 each include a conductive pad or terminal 122 at a bottom thereof. The conductive pads or terminals 122 are interconnected to other conductive pads 126 on a lower surface 114 of interposer substrate 110. Such conductive pads 126 may be substantially directly below conductive

pads or terminals 122 and merely comprise an opposing surface thereof or, more typically, the conductive pads 126 may be placed at various predetermined locations laterally offset and remote from their associated conductive pads or terminals 122 and electrically connected thereto by conductive traces 124 (shown in FIG. 1 in broken lines).

The multiple recesses 120 are formed in the interposer substrate 110 in a preselected pattern to correspond with a bond pad configuration formed on an active surface of a semiconductor die intended to be attached thereto. For example, FIG. 1 depicts the multiple recesses 120 in a centrally aligned, single row configuration in interposer substrate 110. Such configuration is made to correspond and attach to a bumped semiconductor die having a centrally aligned, single row bond pad configuration which will be more fully illustrated hereafter. Other preselected patterns, by way of example, may include an I-shaped recess configuration (FIG. 14) or a peripheral recess configuration (FIG. 15); however, the present invention may be adapted to any recess configuration to match with a any particular, desired bond pad configuration. In addition, the multiple recesses 120 may be formed in any suitable shape, such as square, rectangular and circular, and may include tapered side walls so that the openings or mouths of the recesses 120 are larger than the bottoms thereof.

It will be observed in FIG. 1 that conductive traces 124 extend over recesses 120 and may optionally extend therebeyond, if desired, for enhanced adhesion of conductive traces 124 to dielectric substrate member 111. Conductive pads or terminals 122 may completely cover the bottoms of recesses 120 or, as depicted in FIG. 1, may be narrower than recesses 120 at the bottoms thereof so that gaps 121 are defined on one or both sides of conductive pads or terminals 122. As implied above, the conductive traces, which may, for example, comprise copper or a copper alloy, may be adhered to the dielectric substrate member of UPILEX, BT resin, FR 4 or, FR 5 laminate material, or other substrate materials, using adhesives as known in the art. In some instances, the material of the conductive traces may be adhesively laminated to the substrate in the form of a conductive sheet, the traces then being subtractively formed from the conductive sheet, as by etching.

Further, interposer substrate 110 may also include an opening 130 (shown in broken lines in FIG. 1) formed in thereacross, the opening 130 substantially extending

along a longitudinal extent of the centrally aligned, single row configuration of the multiple recesses 120 from one end of interposer substrate 110 to the other. Opening 130 may be formed wholly in the material of dielectric substrate member 111, or may, as shown by the broken lead line from reference numeral 130 in FIG. 2 and the broken lines and the broken lead line from reference numeral 130 in FIG. 3, be formed in solder mask 118. Of course, opening 130 may be formed partially in dielectric member 111 and partially solder mask 118, as desired. Opening 130 may be formed to align along any employed recess configuration, *i.e.*, I-shape, peripheral. To better illustrate opening 130, FIG. 2 depicts a cross-sectional view taken along lines 2-2 in FIG. 1. As illustrated, opening 130 includes multiple segments 132, each segment 132 extending between separate individual recesses 120 of the multiple recesses 120. Further, each segment 132 as shown extends along the axis of opening 130 to a side portion of each of the recesses 120; however the segments 132 may extend and be positioned from the opening 130 to the recesses 120 in any suitable manner. For example, and as depicted in FIG. 1A, opening 130 may comprise a slot laterally offset from recesses 120 which are themselves defined between fingers 111f of flexible dielectric member 111 which terminate at opening 130 in dielectric member 111. As shown, conductive traces 124 extend across opening 130, and solder mask 118 covers the end portions thereof flanking opening 130 and providing an enhanced depth and width to opening 130 for underfilling purposes.

To further illustrate opening 130, FIG. 3 is a cross-sectional view taken along lines 3-3 of FIG. 1. FIG. 3 depicts opening 130 extending directly into the recesses 120, i.e., into the plane of the drawing sheet. Such opening 130 is shown as having a lateral width smaller than the recesses 120, however, the opening may by sized substantially equal to, or larger than, the lateral width of the recesses 120. FIG. 3 also depicts conductive pads or terminals 122 at the bottom of each of the recesses 120 interconnected through conductive traces 124 with conductive pads 126 exposed at the lower surface 114 of the interposer substrate 110 through solder mask 118.

FIGS. 1 and 3 also depict an adhesive element 116 disposed on the first surface 112 of the interposer substrate 110. Such adhesive element 116 is preferably disposed on a portion of the first surface 112 of the interposer substrate 110 that is adjacent but separated from each of the multiple recesses 120. The adhesive

element 116 may be any suitable adhesive material as known in the art, such as an epoxy, acrylic, or other suitable adhesive. The adhesive element 116 may comprise, without limitation, a polyimide tape bearing adhesive on both sides thereof with the exposed surface (facing away from dielectric substrate member 111) being covered with a protective release layer until adherence to a semiconductor die is required. Such adhesive element 116 is preferably, but not limited to, of a maximum 25 $\mu$m thickness. As described in more detail later herein, adhesive element may be employed to function as a spacer between a semiconductor die and interposer substrate 110 to provide a vertical standoff therebetween or to control the degree of insertion of conductive bumps carried by the semiconductor die into recesses 120.

FIGS. 4A through 4C depict a process that may be used for forming the recesses 120 in the upper surface 112 of interposer substrate 110. FIG. 4A depicts interposer substrate 110 including a dielectric substrate member 111 having a bottom conductive layer formed on a surface thereof and a protective solder mask 118 formed over the conductive layer. The dielectric substrate member 111 is preferably a flexible material, such as the above-described flexible laminated polymer material or polyimide layer, but may also include a substantially non-flexible material. The bottom conductive layer is preferably copper, or a copper alloy, but may be any suitable electrically conductive material. The bottom conductive layer may comprise conductive traces 124 extending between conductive pads or terminals 122 and conductive pads 126 (see FIG. 3). Such conductive traces 124 may be formed by masking and etching a bottom metal or alloy conductive layer or, alternatively, the traces 124 may be formed by printing using conductive ink, or otherwise formed using any method known in the art. Once the conductive traces 124 are patterned, the protective solder mask 118 may be formed thereover.

FIG. 4B depicts dielectric substrate member 111 with one of the recesses 120 formed therein. Such recesses 120 may be formed by patterning, utilizing a chemical wet etch or dry etch, mechanical drilling or punching, laser ablation, by any method known in the art and suitable for use with the type of material employed for the dielectric substrate member 111. The recesses 120 are preferably formed to expose portions of one of the traces 124, such as conductive pads or terminals 122. At a bottom of each recess 120 and, for example, at the location of each conductive pad or

terminal 122, additional conductive material may be placed, such as gold or eutectic tin/lead solder, the material selected being compatible with the conductive material of the traces 124 and with the bumps of a semiconductor die to be mated with interposer substrate 110.. FIG. 4C illustrates that the walls of the recesses 120 may include a conductive layer 123 thereon formed, for example, by electroless plating; however, such plating is not required for practice of the present invention. Further and as shown in FIGS. 4B and 4C, recesses may be formed with large mouths 120m which taper to a smaller bottom 120b. Such tapering may be easily effected using isotropic etching techniques as known in the art.

FIGS. 5A through 5D depicts a process similar to that depicted and described in FIGS. 4A - 4C of forming recesses 120 in the first surface 112 of interposer substrate 110, with the additional of another layer, namely an second conductive layer 125, as shown in FIG. 5A. Such second conductive layer 125 is preferably a copper or copper alloy layer, but may be any suitable electrically conductive material, and may be patterned with traces depending on the needs and requirements of the particular semiconductor die to which the interposer substrate 110 is attached. FIG. 5B depicts upper conductive layer 125 patterned to expose portions of dielectric substrate member 111 where the recesses 120 are to be formed and substantially etched back from the intended lateral boundaries of the recess mouths . As shown in FIG. 5C, a recess 120 is then formed in the exposed portions of substrate member 111, by a chemical wet etch or dry etch, mechanical drilling or punching or laser ablation; however, the recess 120 may be formed utilizing any method known in the art and suitable with the type of material employed for the interposer substrate 110. The recesses 120 are preferably formed to expose conductive pads or terminals 122 of the conductive traces 124, after which additional conductive material may be placed over the exposed portion of the conductive pads or terminals 122 As before, a conductive layer 121 may be formed by electroless plating on the walls of the recesses 120 so that such conductive layer 121 contacts a portion of the conductive pads or terminals 122 of the exposed traces 124, as depicted in FIG. 5D. As shown in FIGS. 5A through 5D in solid lines, solder mask 118 may provide full coverage over the bottoms of conductive traces 124 or, as shown in broken lines, may include an aperture or apertures therethrough, for example to provide an opening 130, to expose the undersides of conductive traces 124 at the locations of

recesses 120 or otherwise, as desired, for enhanced underfill access. If a wet solder mask 118 is employed, recesses 120 in dielectric member 111 are plugged with a removable material before solder mask application; if a dry (film) solder mask 118 is employed, it may merely be laminated to dielectric member 111.

FIGS. 6A - 6B depict simplified cross-sectional views of a first method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip type semiconductor device assembly 160. FIG. 6A illustrates the first surface 112 of interposer substrate 110 aligned and facing the semiconductor die 150 prior to the assembly thereof. Semiconductor die 150 includes an active surface 152 and a back side or surface 154, wherein the active surface 152 includes a plurality of bond pads 158 bearing electrically conductive bumps 156 thereon. Such conductive bumps 156 and bond pads 158 of semiconductor die 150 are of a preselected configuration, wherein the recesses 120 in interposer substrate 110 are sized and configured to correspond with the configuration of the bond pads 158 and conductive bumps 156 of semiconductor die 150 so that the respective configurations or patterns of recesses 120 and conductive bumps 156 are substantially mirror images of each other. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder mask coverage may be provided across the bottoms of conductive traces, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Conductive bumps 156 preferably comprise, but are not limited to, conductive balls, pillars or columns. The material of conductive bumps 156 may include, but is not limited to, any known suitable metals or alloys thereof, such as lead, tin, copper, silver or gold. Conductive or conductor-filled polymers may also be employed, although gold and PbSn solder bumps are currently preferred. The conductive bumps 156 may be of uniform characteristics throughout or include, for example, a core of a first material (including a nonconductive material) having one or more conductive layers of other materials thereon. Conductive bumps 156 are preferably formed on the active surface 152 of each semiconductor die 150 at a wafer level, but such is not required. Conductive bumps 156 may be formed by metal evaporation, electroplating, stencil printing, gold stud bumping by wire bonders, or any suitable method known in the art.

FIG. 6B depicts interposer substrate 110 mounted to semiconductor die 150 to form flip chip semiconductor device assembly 160, wherein such assembly 160 provides

that each of the conductive bumps 156 are substantially inserted in a corresponding recess 120 of interposer substrate 110 and engage with the conductive pads or terminals 122 at the bottom of each of the recesses 120. Such assembly 160 may be initially attached by the adhesive 116 carried on the first surface 112 of the interposer substrate 110. The conductive bumps 156 on the semiconductor die 150 may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 by, for example, reflowing the bumps 156 (in the case of solder bumps) or curing the bumps 156 (in the case of conductive or conductor-filled polymer bumps) as known in the art. Other methods of bonding known in the art may utilized, such as ultrasonic or thermal compression.

FIGS. 7A - 7B depict simplified cross-sectional views of a second method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip semiconductor device assembly 160. FIG. 7A illustrates the first surface 112 of interposer substrate 110 aligned with and facing the semiconductor die 150 prior to the assembly thereof. FIG. 7A is similar to FIG. 6A in substantially every respect, except the conductive bumps 156 on the semiconductor die 150 carry a conductive paste 182 thereon. Such conductive paste 182 may be provided on the bumps by dipping the bumps 150 into a pool of conductive paste 182 or by depositing, dispensing or otherwise transferring the conductive paste 182 to the conductive bumps 150. The conductive paste 182 may include, but is not limited to, eutectic solder, conductive epoxy, or any non-solid conductive material known in the art. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder mask coverage may be provided across the bottoms of conductive traces, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

As depicted in FIG. 7B, the interposer substrate 110 is mounted to semiconductor die 150 to form semiconductor device assembly 160, wherein each of the conductive bumps 156 are substantially inserted into corresponding recesses 120 of interposer substrate 110 with the conductive paste 182 engaging with the conductive pads or terminals 122 in each of the recesses 120. With this arrangement, the conductive paste 182 provides contact with the conductive pads or terminals122 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are non-coplanar. Such conductive bumps 156 having the conductive paste provided

thereon may then be bonded to the conductive pads or terminals122 in the recesses 120 of interposer substrate 110 as previously described in association with FIGS. 6A and 6B.

FIGS. 8A - 8D depict simplified cross-sectional views of a third method of preparing, mounting and bonding interposer substrate 110 with a semiconductor die 150 in a flip chip type semiconductor device assembly 160. FIG. 8A depicts interposer substrate 110 having a mass of conductive paste 182 disposed over a stencil 186, patterned with openings which correspond with recesses 120. The conductive paste 182 is then spread by a spreading member 184 over the stencil 186 so that the conductive paste 182 is deposited in each of the recesses 120. The stencil 186 is then removed prior to aligning the conductive bumps 156 on the semiconductor die 150 with the recesses 120 in the interposer substrate 110, as depicted in FIG. 8B. Alternatively, conductive paste 182 may be disposed into recesses 120 without using a stencil 186, using the surface of dielectric member 111 itself as a stencil.

With the conductive paste 182 in the recesses 120, FIG. 8C depicts the interposer substrate 110 mounted to semiconductor die 150 to form semiconductor device assembly 160, wherein each of the conductive bumps 156 are substantially inserted into the conductive paste 182 in the corresponding recesses 120 of interposer substrate 110. As previously described in FIG. 7B, the conductive paste 182 provides electrical and mechanical interconnection between the bond pads 122 or trace ends and the conductive bumps 150 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are non-coplanar. The semiconductor die 150 may then be bonded with the interposer substrate 110 as previously described in association with FIGS. 6A and 6B. It will be understood, as noted above, that stencil 186 may not be required if the mass of conductive paste 182 is disposed and spread into recesses 120 prior to disposition of an adhesive element 116 over first surface 112. Moreover, it will be understood that conductive paste 182, if eutectic solder, may be disposed in recesses 120 and then reflowed and solidified prior to attachment of semiconductor die 150 to interposer substrate 110 using a second reflow to provide an indefinite shelf life for interposer substrate 110. Alternatively, semiconductor die 150 may be aligned with interposer substrate 110 after conductive paste disposition and a single reflow employed. FIG. 8D is an enlarged view of a single conductive bump 156 carried by a semiconductor die 150 in initial contact with a mass of conductive paste 182 disposed in

a recess 120 in dielectric member 111 of interposer substrate 110 over conductive pad or terminal 122 of a conductive trace 124.

As a further alternative, a conductive bump 156, to be used either in cooperation with or in lieu of a conductive bump 156 carried by semiconductor die 150 may be formed in each of recesses 120 through plating of conductive pads or terminals 120 with a conductive material such as a suitable metal. Such plating may be effected electrolytically, using a bus line connected to each conductive trace 124, or by electroless plating, both techniques being well known in the art.

FIGS. 9A - 9B depict simplified cross-sectional views of a variant of the above-described third method comprising a fourth method of preparing, mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip semiconductor device assembly 160. Such variant is similar to the third method as described in FIGS. 8A - 8C of providing conductive paste in each of the recesses 120, except the conductive bumps 156 are initially unattached to the bond pads 158 of the semiconductor die 150. As depicted in FIG. 9A, the conductive bumps 156 in the form of balls, such as metal balls, are embedded into the conductive paste 182 which was previously spread into the recesses 120 of the interposer substrate 110. The bond pads 158 in the semiconductor die 150 are aligned with the conductive bumps 156 in the recesses 120 in the interposer substrate 110 and then mounted thereto, as depicted in FIGS. 9A - 9B. The conductive paste 182 may comprise a solder wettable to both bond pads 158 and conductive pads or terminals 122 or a conductive or conductor-filled adhesive. It will also be understood and appreciated that conductive bumps 156 may themselves comprise solder, such as a PbSn solder, and conductive paste 182 eliminated or also comprising a compatible solder.

As a further alternative and as previously described with respect to FIGS. 8A and 8B, a conductive bump 156 to be used in lieu of a conductive bump 156 carried by semiconductor die 150 may be formed in each of recesses 120 through plating of conductive pads or terminals 120 with a conductive material such as a suitable metal.

It will be well appreciated by one of ordinary skill in the art that, since the bumps are bonded within the recesses 120 of the interposer substrate 110 itself, the height of the flip chip semiconductor device assembly 160 is minimized. Therefore, conductive bumps 156 may be formed larger in size than those of conventional flip chip assemblies

without increasing, or even while decreasing, the height of the flip chip semiconductor device assembly 160, resulting in the increase in electrical and mechanical reliability and performance of the interconnections between the interposer substrate 110 and the semiconductor die 150. Further, the recesses 120 in the interposer substrate 110 provide an inherent alignment aspect absent in a conventional flip chip semiconductor device assembly because the conductive bumps 156 easily slide into their respective corresponding recesses 120 to ensure proper alignment and proper attachment thereof. In addition, the adhesive element 116 on the first surface 112 of the interposer substrate 110 as well as the conductive paste 182 in the recesses 120 may act as a height controller for reliable attachment of the semiconductor die 150 to the interposer substrate 110, wherein the adhesive element 116 and/or the conductive paste 182 may be used to compensate for any irregularities due to varied conductive bump sizes, recess depths and planarity variation in the surfaces of the interposer substrate 110 and semiconductor die 150.

As shown in FIG. 10, a dielectric filler material 166 (commonly termed an "underfill" material) may be optionally applied through opening 130. The method employed to apply the filler material 166 is preferably by dispensing under pressure from dispenser head 164, but may include any method known in the art, such as gravity and vacuum injecting. In this manner, the dielectric filler material 166 may be applied into the opening 130, move as a flow front through the multiple passages 132 and into each of the recesses 120 to fill a space around the conductive bumps 156, bond pads158 and conductive pads or terminals 122. The dielectric filler material 166 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means in order to form at least a semisolid mass in the recesses 120. Such dielectric filler material 166 provides enhanced securement of the components of flip chip semiconductor device assembly 160 as well as precluding shorting between conductive elements and protecting the conductive elements from environmental concerns, such as moisture. As such, compared to the conventional underfilling of the entire semiconductor die, the semiconductor assembly 160 of the present invention requires less time since the filler material may only be directed to fill the recesses 120 or, rather, any left over space within in the recesses 122 proximate the interconnections, *i.e.*, bumps 156.

Turning back to the third and fourth methods depicted in FIGS. 8A - 8C and 9A - 9B, the interposer substrate 110 described for use in such methods may not include an opening for applying filler material to the recesses 120 because the recesses 120 are substantially filled with conductive paste 182. Therefore, it is contemplated that applying filler material through an opening 130 in the interposer substrate 110 described in the third and fourth methods may not be necessary.

FIG. 10 also depicts conductive balls 162, such as solder balls or any suitable conductive material 162, provided at the conductive pads 126 exposed at the second surface 114 of the interposer substrate 110. Such conductive balls 162 may be provided prior to or subsequent to dispensing the filler material 166, and formation thereof, if formed of solder, is facilitated by solder mask 118 (see FIG. 2) and apertures therethrough placed over locations of conductive pads 126. Of course, conductive balls 162 may comprise other materials, such as conductive epoxies or conductor-filled epoxies, and may comprise other shapes, such as bumps, columns and pillars. Once the conductive balls 162 are formed on or attached to the interposer substrate 110 and the dielectric filler material 166 has been provided (if desired or necessitated), the semiconductor die 150 may then be either partially or fully encapsulated by an encapsulation apparatus 178 with a dielectric encapsulation material 168 as depicted in FIG. 11. In the case of partially encapsulating the semiconductor die 150, encapsulation material 168 may be dispensed by dispenser head 164 about the periphery of the die 150 so that the back side or surface 154 of the die is left exposed. In the case of fully encapsulating the semiconductor die 150, encapsulation material 168 may be provided by dispensing, spin-coating, glob-top, pot molding, transfer molding, or any suitable method known in the art. It is currently preferred that such encapsulation material 168 be applied to the back side or surface 154 of the semiconductor die 150 (which may include at the wafer level, as by spin-coating) prior to dispensing additional encapsulation material 168 about the periphery of the semiconductor die 150 in order to facilitate fully encapsulating the die 150.

FIG. 11 also depicts flip chip semiconductor device assembly 160 attached to another carrier substrate 170, such as a printed circuit board or mother board. The carrier substrate 170 includes a substrate upper surface 172 and a substrate lower surface 174, upper surface 172 bearing substrate terminal pads 176 arranged to

correspond and attach with conductive balls 162 on the bottom surface 114 of interposer substrate 110. As such, the flip chip semiconductor device assembly 160 may be mechanically and electrically connected to substrate 170 by reflowing the conductive (solder) balls 162 to the substrate pads 176. A dielectric filler material (not shown) as known in the art may then be applied between the flip chip semiconductor device assembly 160 and the carrier substrate 170 for securing and protecting the interconnections, *i.e.*, conductive balls 162, therebetween.

FIG. 12 depicts a flip chip semiconductor device assembly 160 including a heat transfer element 180. The heat transfer element 180 may be provided over the first surface 112 of the interposer substrate 110 and under the adhesive 116 as a thin, thermally conductive material. The heat transfer element 180 may also be provided on the active surface 152 of the semiconductor die 150 to abut the first surface 112 of the interposer substrate 110. Another option is to provide the heat transfer element 180 on the back surface 154 of the semiconductor die 150 as shown in broken lines. Such heat transfer device element 180 is configured and located to thermally conduct heat formed and generated from the electrical components of the semiconductor die 150 and to remove such heat from the flip chip semiconductor device assembly 160, to reduce the incidence of thermal fatigue in the interconnections and circuitry of the assembly160 and, specifically, the semiconductor die 150 as well as reducing operating temperatures.

The heat transfer element 180 may be formed of any thermally conductive material, such as copper and silver, but may also comprise a thermally conductive material that is non-electrically conductive, such as a thin diamond material and/or diamond composite deposited as a thin film or layer.

As depicted in FIGS. 13A and 13B, the interposer substrate 110 of the present invention may also be formed initially on a wafer scale corresponding to a semiconductor wafer carrying a plurality of unsingulated semiconductor dice 150 and then singulated or separated after assembly by a dicing process into the individual flip chip semiconductor device assemblies 160. As used herein, the term "wafer" not limited to conventional substantially circular semiconductor wafers but extends to any large scale substrate including a layer of semiconductor material of sufficient size for formation of multiple dice thereon and encompasses portions of such large scale substrates bearing multiple semiconductor dice. In particular, FIG. 13A depicts a

simplified cross-sectional view of a semiconductor wafer 250 facing a wafer scale interposer substrate 210 prior to mutual attachment thereof. The semiconductor wafer 250 collectively includes multiple semiconductor dice 251 in columns and rows separable along borders 253 as shown in broken lines, wherein the wafer 250 includes a back side or surface 254 and an active surface 252 and each semiconductor die 250 includes conductive bumps 256 in a configuration dictated by the bond pads 258 on which they are formed.

The interposer substrate 210 includes a first surface 212 and a second surface 214 with multiple recesses 220 formed in the first surface 212 and openings 230 having passages (not shown) formed in the second surface 214. The recesses 220 formed in the interposer substrate 210 are made to correspond in substantially a mirror image with the bump configuration on each of the dice 251 of the wafer 250. In this manner, the interposer substrate 210 may be attached to the wafer 250 via an adhesive element 216 on the first surface 212 of the interposer substrate 210 so that the bumps 256 on the wafer 250 are inserted into and substantially received within the multiple recesses 220 formed in the interposer substrate 210 to form a wafer scale assembly 260, as depicted in FIG. 13B. The wafer assembly 260 may then be singulated or "diced" along the borders 253 of the wafer 250 via a dicing member such as a wafer saw 280 to form individual flip chip semiconductor device assemblies that each include one or more semiconductor die 251 having the separated interposer substrate 210 of the present invention mounted thereon.

Also at the wafer level and as previously described in association with FIGS. 6A-6B, 7A-7B, 8A-8C, 9A-9B, the conductive bumps 256 may be bonded to the conductive pads or terminals in the recesses 220 to, therefore, mechanically bond and electrically connect the semiconductor wafer 250 to the wafer scale interposer substrate 210. In addition, dielectric filler material may be applied through the openings 230 and conductive balls 262 may be provided on the bond posts on the second surface 214 of the interposer substrate 210, either prior to dicing the wafer scale assembly 260 or subsequent thereto.

FIG. 14 depicts a top plan view of an interposer substrate 310 having an alternative recess configuration made for corresponding to a substantial "mirror image" bond pad configuration on the active surface of a semiconductor die. In particular, in

this first alternative, there is an I-shaped bond pad configuration, wherein multiple recesses 320 are formed over the upper surface 312 of interposer substrate 310 that are aligned in the shape of an "I" with adhesive elements 316 disposed on either side of the body of the "I" and between the ends thereof. In another alternative recess configuration, the recesses may be formed in an interposer substrate around a periphery thereof. Such alternative is depicted in FIG. 15 of a top plan view of an interposer substrate 410 with an adhesive element 416 at a center portion of interposer substrate 410 and recesses 420 formed thereabout and proximate a periphery of interposer substrate 410. As in the previous recess configurations, the periphery recess configuration in interposer substrate 410 is made to correspond with a substantial "mirror image" bond pad configuration on an active surface of a semiconductor die.

As previously described with respect to the center row recess configuration, both the I-shaped and the periphery configurations depicted in FIGS. 14 and 15 may include one or more openings in a surface of the interposer substrate opposing that through which the recesses are formed with passages extending therefrom to each of the recesses. As such, subsequent to mounting a bumped semiconductor die to the interposer substrate, dielectric filler material may be applied through the opening and passages to fill the recesses and protect the conductive bumps disposed therein.

FIG. 16 depicts a cross-sectional view of a semiconductor assembly 460 including a semiconductor die 450 mounted face down to an interposer substrate 410 having a peripheral recess configuration and an alternative method of applying dielectric filler material 462 to the assembly 460. In particular, dielectric filler material 162 may be applied by dispenser 164 around the periphery of the semiconductor die 450 so that the dielectric filler material 162 flows under the die 450 and around the conductive bumps 456 adjacent the die periphery. As such, the dielectric filler material 162 is only needed proximate the conductive bumps 456 and not under the entire die as done conventionally. The semiconductor die 450 may be left exposed or be encapsulated by encapsulation member 178, which may provide encapsulation material 168 to the assembly 460 via dispensing, spin-coating, glob-top, depositing or transfer molding, or any suitable method known in the art. It is preferred that such encapsulation material 168 be applied to the back surface 454 of the semiconductor die 450 at the

wafer level or prior to dispensing the filler material 162 about the periphery, to facilitate fully encapsulating the die 450.

Further, in this alternative, it is preferred that the semiconductor die 450 is assembled and bonded to the interposer substrate 410 with the conductive bumps 456 disposed in the conductive paste 182 as described in FIGS. 8A-8C and 9A-9B; however, this alternative may also employ the methods described in FIGS. 6A-6B and 7A-7B for assembling and bonding the die 450 to the interposer substrate 410.

As illustrated in block diagram form in drawing FIG. 17, flip chip semiconductor device assembly 160 of the present invention is mounted to a circuit board 570, such as previously-discussed carrier substrate 170, in a computer system 500. In the computer system 500, the circuit board 570 is connected to a processor device 572 which communicates with an input device 574 and an output device 576. The input device 574 may be a keyboard, mouse, joystick or any other computer input device. The output device 576 may be a monitor, printer or storage device, such as a disk drive, or any other output device. The processor device 572 may be, but is not limited to, a microprocessor or a circuit card including hardware for processing computer instructions. Additional structure for the computer system 500 is readily apparent to those of ordinary skill in the art.

As a further approach to implementing the present invention and as depicted in FIG. 18, an interposer substrate 110 may be provided having conductive traces 124 laminated thereto, the bottoms thereof being fully covered or, optionally, uncovered, by solder mask 118, and a conductive bump 156a formed by reflow (if solder) or curing (if an epoxy) of a mass of conductive paste 182 at the bottom of each recess 120. A dielectric filler material 166 in then disposed over conductive bumps 156a in each recess 120 as shown. A semiconductor die 150 carrying a like plurality of conductive bumps 156b arranged for superimposed contact with conductive bumps 156a when semiconductor die 150 is aligned with interposer substrate 110, is then aligned over interposer substrate 110 and vertically pressed thereagainst as depicted by arrow M, the die placement motion squeezing the non-dielectric filler material laterally outward so that conductive bumps 156a and 156b meet and make conductive contact. Adhesive elements 116 may, as shown, be used, or may be omitted, as desired.

In a variation of the approach of FIG. 18, it is also contemplated that, in lieu of using dielectric filler 166 and to provide an interposer substrate-to-die adhesive instead of using a separate adhesive element 116, a nonconductive film NCF as shown in broken lines in FIG. 18 be disposed over interposer substrate 110 after formation of conductive bumps 156a thereon and prior to assembly with a semiconductor die 150 carrying conductive bumps 156b. When the semiconductor die 150 and interposer substrate 110 are pressed together, bumps 156a and 156b will penetrate the nonconductive film to initiate mutual electrical contact therebetween. Suitable nonconductive films include the UF511 and UF527 films offered by Hitachi Chemical, Semiconductor Material Division, Japan.

It is further contemplated that an approach to the present invention, comprising a flexible interposer substrate using at least one conductive layer laminated to at least one dielectric member or interposed between two dielectric members, may be employed to implement a folded interposer substrate package according to the present invention. Several exemplary embodiments of folded interposer substrate packages are respectively disclosed in FIGS. 19 through 21. Of course, more than one conductive layer may be employed, separated by a dielectric layer and interconnected as desired or required using conductive vias, the use of a single conductive layer being merely illustrative of the invention and not limiting thereof. However, the addition of a second conductive layer, of necessity, increases package depth or thickness, which may be undesirable in some instances.

FIG. 19 depicts an interposer substrate 110, which may comprise either a dual conductive layer or single conductive layer interposer substrate according to the present invention, folded over upon itself in two portions 110a and 110b, with back-to-back semiconductor dice 150a and 150b therebetween to form folded interposer substrate package 600a. The semiconductor dice 150a and 150b are flip-chip configured with conductive bumps 156 projecting therefrom into recesses (not shown for clarity) in interposer substrate 110 as discussed with respect to previous embodiments. The standoff areas between each semiconductor die 150 and its adjacent portion of interposer substrate 110 may be filled with dielectric filler material 166, as may the peripheries and back sides of the semiconductor dice 150a and 150b, and the bight area 190 of the fold between interposer substrate portions 110a and 110b. Enlarged

conductive elements 192 may be employed to connect the interposer substrate 110 to higher-level packaging, such as a carrier substrate in the form of a printed circuit board. Exemplary folded interposer substrate package 600a results. Folded interposer substrate package 600a may be formed by respectively connecting semiconductor dice 150a and 150b to the same side of interposer substrate 110 in unfolded form over then-laterally-adjacent portions 110a and 110b, introducing dielectric filler material 166 between active surfaces of the dice and about the lateral peripheries thereof and the then folding the substrate 110 and adhering semiconductor dice 150a and 150b back-to-back. Encapsulation of bight portion 190 with the same or different dielectric filler material 166 may then be effected and bumping with enlarged conductive elements 192 for connection to higher level packaging may be completed. Insulation of the exterior surface of interposer substrate 110 may be provided with a covering dielectric member such as a film having apertures therethrough by which enlarged conductive elements 192 communicate with a conductive layer (not shown) of interposer substrate 110.

FIG. 20 depicts another folded interposer substrate package 600b implementing two folds to provide three mutually superimposed substrate portions 110a, 110b and 110c. Three semiconductor dice 150a-c are also employed in this embodiment, but the third portion 110c of interposer substrate 110 lies over semiconductor die 150c, which is inverted. Again, standoff areas and bight areas 190 may be filled with dielectric filler material 166. Exemplary folded interposer substrate package 600b results. Folded interposer substrate package 600b may be formed by respectively connecting semiconductor dice 150a, 150b and 150c to the same side of interposer substrate 110 in unfolded form over then-laterally-adjacent portions 110a, 110b and 110c, introducing a dielectric filler material 166 between the active surfaces of each die 150a-c and interposer substrate 110 and about the peripheries thereof, then folding the substrate 110 and adhering semiconductor dice 150a and 150b back-to-back and semiconductor die 150c to an exterior surface of portion 110a, after which bight portions 190 may be dielectrically filled with the same or different dielectric material 166 and bumping with enlarged conductive elements 192 for connection to higher level packaging may be completed.

FIG. 21 depicts yet another folded interposer substrate package 600c implementing three folds to provide four mutually superimposed substrate

portions 110a, 110b, 110c and 110d. Four semiconductor dice 150a-d are employed in this embodiment, 150a and 150b being placed back-to-back and 150c and 150d being placed back-to-back. Again, standoff areas and bight areas 190 may be filled with an dielectric filler material 166. Folded interposer substrate package 600c results. Folded interposer substrate package 600c may be formed by respectively connecting semiconductor dice 150a-d to the same side of interposer substrate 110 in unfolded form over then-laterally-adjacent portions 110a, 110b, 110c and 110d, after which a dielectric filler material 166 may be introduced between the active surface of each die 150a-d and its associated portion 110a-d of interposer substrate 110 and about the die peripheries. Substrate portions 110a and 110d may then be folded over substrate portions 110b and 110c. Semiconductor dice 150a and 150b are adhered back-to-back and semiconductor dice 150c and 150d are adhered back-to-back. The assembly is then refolded between substrate portions 110b and 110c, which are then mutually adhered so that all four semiconductor dice 150a-d and all four substrate portions 110a-d are in substantial superimposition. Encapsulation of bight portions 190 with the same or a different dielectric material 166 and bumping with enlarged conductive elements 192 for connection to higher level packaging may then be completed.

Thus it will be apparent that the flip chip semiconductor device assembly of the present invention provides a compact, robust package at a reduced cost in comparison to conventional bumped semiconductor die assemblies employing dual conductive layer interposers. For example, a package height reduction of about 90 $\mu$m may be effected using a 100 $\mu$m thick dielectric member and eliminating a second 12 $\mu$m thick conductive layer adjacent the semiconductor die, even with a 25 $\mu$m thick adhesive element comprising a tape disposed between the semiconductor die and interposer substrate, since the discrete conductive elements or conductive bumps of the die may be substantially completely received within the recesses of the dielectric member, but for any vertical standoff provided by the tape. Electrical connection reliability is improved, since the conductive bumps are in contact with the terminals at the recess bottoms, either directly or through an interposed conductive material within the recesses, eliminating the need for conductive vias and an electrical connection between a first conductive layer adjacent the semiconductor die contacted by a conductive bump and a via and another electrical connection between the via and a second conductive layer on

the opposite side of the interposer substrate. Moreover, due to the straightforward design, even large semiconductor dice carrying a large number of conductive bumps may be rerouted for external connection using the present invention as all rerouting is carried out on the side of the interposer substrate facing away from the semiconductor die.

The present invention may employ a recess lateral dimension or diameter which is far in excess of the lateral dimension or diameter of an associated conductive bump, thus greatly facilitating bump and recess alignment by loosening required dimensional tolerances. For example, a 75$\mu$m bump may be employed with a 120 $\mu$m recess using a 175 $\mu$m pitch

It is anticipated, as previously noted, that various types of conductive bumping may be used to implement the present invention. However, it is currently believed that gold stud bumps used in combination with a solder paste disposed in the recesses are particularly suitable as for prototyping and low volume production due to its advanced state of development, low cost, flexibility in accommodating different bond pad layouts and fine pitch capability.

In addition, the use of a flexible interposer substrate easily accommodates minor variations between heights of various conductive bumps and lack of absolute planarity of the semiconductor die active surface as well as that of the terminals. Further, encapsulation, if desired, of some or all portions of the periphery and back surface of the semiconductor die by a variety of methods is greatly facilitated, as is incorporation of a thermally conductive heat transfer element such as a heat sink without adding complexity to the package. If an adhesive element employing a tape is used to secure the semiconductor die and interposer substrate together, different bond pad arrangements are easily accommodated without the use of a liquid or gel adhesive and attendant complexity of disposition. Further, tape may be used to resolve lack of coplanarity of the conductive bumps on a semiconductor die or at wafer level and to provide cushioning during die attach to the interposer substrate, as force may be applied sufficient to ensure contact of the conductive bumps with terminals without damage to the assembly. More specifically, during semiconductor die placement, the tape may act as a stopper or barrier, and as a cushion. If a conductive paste is deposited in a via, the tape acts as a barrier to prevent paste contamination of the surface of the semiconductor die. If, on the other hand, solidified conductive bumps, when heat is used to soften the

bump material, the tape acts as a stopper as well as a cushion when the bump material relaxes. In addition, tape accommodates the "spring back" effect exhibited when force used to assemble a semiconductor die and interposer substrate is released, helping to keep the interconnection or joint together. These advantages are applicable to both rigid or flexible interposer substrates.

Further, use of tape facilitates handling of the assembly prior to reflow of solder-type conductive bumps in the recesses as well as rework, as the assemblies may be electrically tested before reflow and before a dielectric filler is applied and/or the semiconductor die encapsulated and a defective die removed and replaced. The presence of the tape also reduces the volume of dielectric filler material (if employed) required between the interposer substrate and semiconductor die and its compliant characteristics reduce the potential incidence of stress-induced defects due to thermal cycling of the assembly during operation.

While the present invention has been disclosed in terms of a certain preferred embodiments and alternatives thereof, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited. Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from one embodiment may be combined with those of another while remaining within the scope of the invention. For example, the opening 130 and segments 132 described in association with the centrally aligned recess configuration in interposer substrate 110 in FIGS. 1-3, may also be provided and adapted to the I-shaped recess configuration of interposer substrate 310 and the periphery recess configuration of interposer substrate 410 in FIGS. 14 and 15, respectively. In addition, the present invention is contemplated as affording advantages to assemblies using rigid as well as flexible interposer substrates although, of course, some features and embodiments may offer greater utility to flexible interposer substrates.

CLAIMS

What is claimed is:

1. A semiconductor device assembly comprising:

a semiconductor die having an active surface and a back surface, said active surface having a plurality of spaced conductive bumps extending transversely therefrom; and

an interposer substrate having first surface facing the semiconductor die and a second, opposing surface, said interposer substrate comprising a dielectric member having a plurality of spaced recesses opening onto said first surface and extending through said dielectric member to a plurality of conductive terminals extending transversely across each of the plurality of spaced recesses and proximate said second surface;

wherein at least one of said spaced conductive bumps is substantially completely received in each recess of said plurality of spaced recesses in conductive contact with a conductive terminal of the plurality of conductive terminals.

2. The assembly of claim 1, wherein said dielectric member comprises at least a portion of one of at least one polyimide layer, a ceramic, a BT resin, an FR4 substrate and an FR5 substrate.

3. The assembly of claim 1, wherein said interposer substrate comprises a flexible tape.

4. The assembly of claim 1, wherein said plurality of spaced conductive bumps exhibit heights substantially equal to depths of said plurality of spaced recesses and end portions of each of said plurality of spaced conductive bumps substantially abut each of said plurality of conductive terminals, respectively.

5. The assembly of claim 1, wherein said active surface of said semiconductor die abuts with said first surface of said interposer substrate.

6. The assembly of claim 1, wherein at least some recesses of said plurality of spaced recesses communicate with at least one opening through said second surface of said interposer substrate.

7. The assembly of claim 6, wherein said at least one opening extends a length in a plane of said interposer substrate and is in communication with at least some recesses of said plurality of spaced recesses.

8. The assembly of claim 1, wherein said plurality of conductive terminals comprise portions of a plurality of conductive traces extending over bottoms of at least some recesses of said plurality.

9. The assembly of claim 1, wherein each of said plurality of spaced recesses include electroless plating on at least walls thereof.

10. The assembly of claim 1, wherein said interposer substrate includes conductive balls electrically connected to said plurality of conductive terminals, respectively, and protruding transversely from said second surface.

11. The assembly of claim 1, wherein said plurality of spaced conductive bumps on said active surface of said semiconductor die are aligned along a single central row or a double central row.

12. The assembly of claim 11, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of conductive bumps.

13. The assembly of claim 1, wherein said plurality of spaced conductive bumps on said active surface of said semiconductor die are located adjacent at least a portion of a periphery of said semiconductor die.

14. The assembly of claim 13, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps.

15. The assembly of claim 1, wherein said plurality of spaced conductive bumps on said active surface of said semiconductor die are arranged in an I-shaped configuration.

16. The assembly of claim 15, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of conductive bumps.

17. The assembly of claim 1, further comprising an encapsulation material encapsulating at least a portion of said semiconductor die.

18. The assembly of claim 1, further comprising a thermally conductive element in thermal communication with said semiconductor die.

19. The assembly of claim 1, further comprising a dielectric filler material in at least some recesses of said plurality of spaced recesses.

20. The assembly of claim 19, wherein the dielectric filler material extends between at least a portion of said active surface of said semiconductor die and said first surface of said interposer substrate.

21. The assembly of claim 1, further comprising an adhesive element disposed between said first surface of said interposer substrate and said active surface of said semiconductor die.

22. The assembly of claim 21, wherein the adhesive element comprises a tape having a thickness.

23. The assembly of claim 1, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of the plurality of spaced conductive bumps.

24. The assembly of claim 23, wherein at least some of said spaced conductive bumps are suspended over a conductive terminal of said plurality of conductive terminals in a recess of said plurality of spaced recesses and in conductive contact therewith through an interposed conductive material within said recess.

25. A semiconductor device assembly comprising:

a wafer having an active surface and a back surface and including a plurality of unsingulated semiconductor dice, each of said unsingulated semiconductor dice having a plurality of spaced conductive bumps on said active surface; and

a wafer scale interposer superimposed on said wafer, having a first surface facing said wafer and a second, opposing surface, and comprising a dielectric member, said wafer scale interposer including a plurality of unsingulated interposer substrates each sized and aligned with one of said plurality of semiconductor dice of said wafer, each of said interposer substrates having a plurality of spaced recesses opening onto said first surface and extending through said dielectric member to a plurality of conductive terminals extending across each of said plurality of spaced recesses, respectively and proximate said second surface;

wherein at least one of said spaced conductive bumps is substantially completely received in each recess of said plurality of spaced recesses in conductive contact with a conductive terminal of said plurality of conductive terminals.

26. The assembly of claim 25, further including at least one adhesive element disposed between each of said unsingulated semiconductor dice and an aligned unsingulated interposer substrate.

27. The assembly of claim 26, wherein said at least one adhesive element comprises a tape having a thickness.

28. The assembly of claim 25, wherein said dielectric member comprises at least a portion of one of at least one polyimide layer, a ceramic, a BT resin, an FR4 substrate and an FR5 substrate.

29. The assembly of claim 25, wherein said wafer scale interposer comprises a flexible tape.

30. The assembly of claim 25, wherein said plurality of spaced conductive bumps exhibit heights substantially equal to depths of said plurality of spaced recesses and end portions of said spaced conductive bumps substantially abut said terminals.

31. The assembly of claim 25, wherein said active surface of said wafer abuts with said first surface of said wafer scale interposer.

32. The assembly of claim 25, wherein at least some recesses of said plurality of spaced recesses communicate with at least one opening through said second surface of said wafer scale interposer.

33. The assembly of claim 32, wherein said at least one opening extends a length in a plane of said wafer scale interposer and is in communication with at least some recesses of said plurality of spaced recesses.

34. The assembly of claim 25, wherein said plurality of conductive terminals comprise portions of a plurality of conductive traces extending over bottoms of at least some recesses of each said plurality of spaced recesses.

35. The assembly of claim 25, wherein each of said plurality of spaced recesses include electroless plating on at least walls thereof.

36. The assembly of claim 25, wherein said interposer includes conductive balls electrically connected to said plurality of conductive terminals and protruding transversely from said second surface.

37. The assembly of claim 25, wherein said plurality of spaced conductive bumps on said active surface of each said unsingulated semiconductor die are aligned along a single central row or a double central row.

38. The assembly of claim 37, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps of an aligned unsingulated semiconductor die.

39. The assembly of claim 25, wherein said plurality of spaced conductive bumps on said active surface of each said unsingulated semiconductor die are located adjacent at least a portion of a periphery of each said unsingulated semiconductor die.

40. The assembly of claim 39, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps of an aligned unsingulated semiconductor die.

41. The assembly of claim 25, wherein said plurality of spaced conductive bumps on said active surface of each said unsingulated semiconductor die are arranged in an I-shaped configuration of each said semiconductor die.

42. The assembly of claim 41, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps of an aligned unsingulated semiconductor die.

43. The assembly of claim 25, further comprising an encapsulation material encapsulating at least a portion of each said unsingulated semiconductor die.

44. The assembly of claim 43, wherein the encapsulation material extends over at least the back surface of said wafer.

45. The assembly of claim 25, further comprising a thermally conductive element in thermal communication with each said unsingulated semiconductor die.

46. The assembly of claim 25, further comprising a dielectric filler material in at least some recesses of each said plurality of spaced recesses.

47. The assembly of claim 46, wherein said dielectric filler material extends between at least a portion of said active surface of said wafer and said first surface of said wafer scale interposer.

48. The assembly of claim 25, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps.

49. The assembly of claim 48, wherein at least some of said spaced conductive bumps are suspended over a conductive terminal of said plurality of conductive terminals in a recess of said plurality of spaced recesses and in conductive contact therewith through an interposed conductive material within said recess.

50. An electronic system comprising:

a processor device coupled to an input device and an output device; and

a semiconductor assembly coupled to at least one of said processor device, said input device and said output device, said semiconductor assembly comprising:

a semiconductor die having an active surface and a back surface, said active surface having a plurality of spaced conductive bumps extending transversely therefrom; and

an interposer substrate having first surface facing said semiconductor die and a second, opposing surface, said interposer substrate comprising a dielectric member having a plurality of spaced recesses opening onto said first surface and extending through said dielectric member to a plurality of conductive terminals extending transversely across each of said plurality of spaced recesses, respectively, and proximate said second surface;

wherein at least one of said spaced conductive bumps is substantially completely received in each recess of said plurality of spaced recesses in conductive

contact with a conductive terminal of said plurality of spaced conductive terminals.

51. The system of claim 50, wherein said dielectric member comprises at least a portion of one of at least one polyimide layer, a ceramic, a BT resin, an FR4 substrate and an FR5 substrate.

52. The system of claim 50, wherein said interposer substrate comprises a flexible tape.

53. The system of claim 50, wherein said plurality of spaced conductive bumps exhibit heights substantially equal to depths of said plurality of spaced recesses end portions of each of said plurality of spaced conductive bumps substantially abut each of said plurality of conductive terminals, respectively.

54. The system of claim 50, wherein said active surface of said semiconductor die abuts with said first surface of said interposer substrate.

55. The system of claim 50, wherein at least some recesses of said plurality of spaced recesses communicate with at least one opening through said second surface of said interposer substrate.

56. The system of claim 55, wherein said at least one opening extends a length in a plane of said interposer substrate and is in communication with at least some recesses of said plurality.

57. The system of claim 50, wherein said plurality of conductive terminals comprise portions of a plurality of conductive traces extending over bottoms of at least some recesses of said plurality.

58. The system of claim 50, wherein each of said plurality of spaced recesses include electroless plating on at least walls thereof.

59. The system of claim 50, wherein said interposer substrate includes conductive balls electrically connected to said plurality of conductive terminals and protruding transversely from said second surface.

60. The system of claim 50, wherein said plurality of spaced conductive bumps on said active surface of said semiconductor die are aligned along a single central row or a double central row.

61. The system of claim 60, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps.

62. The system of claim 50, wherein said plurality of spaced conductive bumps on said active surface of said semiconductor die are located adjacent at least a portion of a periphery of said semiconductor die.

63. The system of claim 62, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps.

64. The system of claim 50, wherein said plurality of spaced conductive bumps on said active surface of said semiconductor die are arranged in an I-shaped configuration.

65. The system of claim 64, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps.

66. The system of claim 50, further comprising an encapsulation material encapsulating at least a portion of said semiconductor die.

67. The system of claim 66, further comprising a thermally conductive element in thermal communication with said semiconductor die.

68. The system of claim 50, further comprising a dielectric filler material in at least some recesses of said plurality of spaced recesses.

69. The assembly of claim 68, wherein said dielectric filler material extends between at least a portion of said active surface of said semiconductor die and said first surface of said interposer substrate.

70. The system of claim 50, further comprising an adhesive element disposed between said first surface of said interposer substrate and said active surface of said semiconductor die.

71. The assembly of claim 70, wherein the adhesive element comprises a tape having a thickness.

72. The system of claim 50, wherein each recess of said plurality of spaced recesses receives therein one conductive bump of said plurality of spaced conductive bumps.

73. The system of claim 50, wherein at least some of said spaced conductive bumps are suspended over a conductive terminal of the plurality of conductive terminals in a recess of the plurality of spaced recesses and in conductive contact therewith through an interposed conductive material within said recess.