

CIRCUIT ARRANGEMENT AND RECEIVER INCLUDING THE CIRCUIT ARRANGEMENT

ABSTRACT

5 According to embodiments of the present invention, a circuit arrangement is provided. The circuit arrangement includes a first input terminal and a second input terminal, a first transistor and a second transistor, each of the first transistor and the second transistor having a first controlled terminal, a second controlled terminal and a control terminal, the first controlled terminal of the first transistor being coupled to the first controlled terminal
10 of the second transistor, the control terminal of the first transistor being coupled to the first input terminal, the control terminal of the second transistor being coupled to the second input terminal, and the second controlled terminal of the first transistor being coupled to the second controlled terminal of the second transistor, an input matching circuit coupled to the first input terminal, the second input terminal, the first transistor
15 and the second transistor, a first resistive element coupled between the control terminal of the first transistor and the second controlled terminal of the first transistor, a second resistive element coupled between the control terminal of the second transistor and the second controlled terminal of the second transistor, and an output terminal coupled to the second controlled terminal of the first transistor and the second controlled terminal of the
20 second transistor, wherein the input matching circuit includes a first inductor, a second inductor, a third inductor, a first capacitor and a second capacitor, wherein the first inductor is coupled between the first input terminal and the control terminal of the first transistor, wherein the second inductor is coupled between the first controlled terminal of the first transistor and the first controlled terminal of the second transistor, wherein the
25 third inductor is coupled between the second input terminal and the control terminal of the second transistor, wherein the first capacitor is coupled between the control terminal of the first transistor and the first controlled terminal of the first transistor, and wherein the second capacitor is coupled between the control terminal of the second transistor and the first controlled terminal of the second transistor. According to further embodiments of
30 the present invention, a receiver including the circuit arrangement is provided.

Figure 4