Claims

1. A non-volatile semiconductor memory device including a plurality of floating gates electrically insulated and a first bit line and a second bit line, a cell being configured for each of the floating gates, wherein

each of cells includes a read transistor for reading out a voltage depending on the presence or absence of charge in the floating gate, a program transistor that injects charge into the floating gate, an erase transistor that ejects charge from the floating gate, and a control capacitor that adjusts a potential at the floating gate, the floating gate extending on respective active regions of the read transistor, the program transistor, the erase transistor, and the control capacitor,

one cell of the cells has a configuration in which the first bit line is connected to the read transistor via a switch transistor, and the second bit line is directly connected to the program transistor, and

the other cell paired with the one cell has a configuration in which the second bit line is connected to the read transistor via a switch transistor, and the first bit line is directly connected to the program transistor.

2. The non-volatile semiconductor memory device according to claim 1, wherein in each of the cells,

the erase transistor is formed in an N-type well or a P-type well, and the control capacitor is formed in an N-type well or a P-type well having the same conductivity type as that of the erase transistor and different from the N-type well or the P-type well of the erase transistor, and

the read transistor, the switch transistor, and the program transistor are formed in a P-type well or an N-type well having a different conductivity type from those of the erase transistor and the control capacitor.

3. The non-volatile semiconductor memory device according to claim 1 or 2, further comprising

an erase gate line that uniformly applies a common voltage to the erase transistors respectively provided for the floating gates, and

a source line that uniformly applies a common voltage to the read transistors respectively provided for the floating gates.

4. The non-volatile semiconductor memory device according to any one of claims 1 to 3, wherein

the one cell and the other cell constitute one bit, and

a gate line is individually connected to the switch transistors respectively provided for the cells and independently controlled to be turned on or off.

5. The non-volatile semiconductor memory device according to any one of claims 1 to 4, wherein

the first bit line is connected to one storage node in an SRAM cell, and the second bit line is connected to the other storage node complementary with the one storage node in the SRAM cell, and

the SRAM cell and the one cell and the other cell constitute one bit.

Claims

1. A non-volatile semiconductor memory device including:

a plurality of floating gates electrically insulated;

a first bit line;

a second bit line; and

a cell being configured for each of the floating gates, wherein

each of the cells includes a read transistor for reading out a voltage depending on the presence or absence of charge in the floating gate, a program transistor that injects charge into the floating gate, an erase transistor that ejects charge from the floating gate, and a control capacitor that adjusts a potential at the floating gate, the floating gate extending on respective active regions of the read transistor, the program transistor, the erase transistor, and the control capacitor,

one cell of the cells has a configuration in which the first bit line is connected to the read transistor in the one cell via a switch transistor in the one cell, and the second bit line is directly connected to the program transistor in the one cell, and

the other cell paired with the one cell has a configuration in which the second bit line is connected to the read transistor in the other cell via a switch transistor in the other cell, and the first bit line is directly connected to the program transistor in the other cell, wherein

the second bit line is used for data programming in the one cell and for reading in the other cell, and the first bit line is used for data programming in the other cell and for reading in the one cell.

2. The non-volatile semiconductor memory device according to claim 1, wherein in each of the cells,

the erase transistor is formed in an N-type well or a P-type well, and the control capacitor is formed in another N-type well or another P-type well having the same conductivity type as that of the erase transistor, and

the read transistor, the switch transistor, and the program transistor are formed in a P-type well or an N-type well having a different conductivity type from that of the erase transistor and the control capacitor.

3. The non-volatile semiconductor memory device according to claim 1 or 2, further comprising

an erase gate line that uniformly applies a common voltage to the erase transistors respectively provided for the floating gates, and

a source line that uniformly applies a common voltage to the read transistors respectively provided for the floating gates.

4. The non-volatile semiconductor memory device according to any one of claims 1 to 3, wherein

the one cell and the other cell constitute one bit, and

gate lines are separately connected to the switch transistors provided for the cells, respectively, and independently controlled to be turned on or off.

5. The non-volatile semiconductor memory device according to any one of claims 1 to 4, wherein

the first bit line is connected to one storage node in an SRAM cell, and the second bit line is connected to the other storage node complementary with the one storage node in the SRAM cell, and

the SRAM cell and the one cell and the other cell constitute one bit.

6. The non-volatile semiconductor memory device according to any one of claims 1 and 3 to 5, wherein

the one cell and the other cell are formed in parallel over a first active region, a second active region, a third active region, and a fourth active region, the first to fourth active regions being electrically insulated from each other.

7. The non-volatile semiconductor memory device according to claim 6, wherein

the switch transistor and the read transistor in the one cell and the program transistor in the other cell are formed in the second active region, and

the switch transistor and the read transistor in the other cell and the program transistor in the one cell are formed in the third active region.