

WHAT IS CLAIMED IS:

1. A memory device, comprising:
 - a substrate;
 - a first layer stack above the substrate and having alternating conductor and insulator layers;
 - a second layer stack, disposed over the first layer stack and having alternating conductor and insulator layers;
 - one or more first vertical structures extending through the first layer stack;
 - a conductive material disposed on a top surface of the one or more first vertical structures;
 - and
 - one or more second vertical structures extending through the second layer stack and through a portion of the conductive material.
2. The memory device of claim 1, wherein the one or more first vertical structures comprises one or more first NAND strings and the one or more second vertical structures comprises one or more second NAND strings.
3. The memory device of claim 2, wherein each of the one or more first NAND strings and the one or more second NAND strings includes a plurality of memory layers surrounding a core insulating material.
4. The memory device of claim 3, wherein the plurality of memory layers includes a stack consisting of a blocking layer, a storage layer, a tunneling layer, and a channel layer.
5. The memory device of claim 4, wherein dopants originating from the conductive material are present in portions of the channel layer adjacent to the conductive material.
6. The memory device of claim 1, wherein the conductive material comprises doped polysilicon.
7. The memory device of claim 1, wherein a portion of the conductive material surrounds a lower end of the one or more second vertical structures.
8. The memory device of claim 1, wherein a width of the conductive material is greater than a width of the one or more first vertical structures and the one or more second vertical structures, such that the conductive material projects outward from the one or more first vertical structures and the one or more second vertical structures.
9. A memory device, comprising:

a substrate;
a first layer stack above the substrate and having alternating conductor and insulator layers;
a second layer stack, disposed over the first layer stack and having alternating conductor and insulator layers;
one or more first vertical structures extending through the first layer stack;
a conductive material disposed on a top surface of the one or more first vertical structures;
and
one or more second vertical structures extending through the second layer stack and abutting a top surface of the conductive material.

10. The memory device of claim 9, wherein the one or more first vertical structures comprise one or more first NAND strings and the one or more second vertical structures comprise one or more second NAND strings.
11. The memory device of claim 10, wherein each of the one or more first NAND strings and the one or more second NAND strings includes a plurality of memory layers surrounding a core insulating material.
12. The memory device of claim 11, wherein the plurality of memory layers includes a stack consisting of a blocking layer, a storage layer, a tunneling layer, and a channel layer.
13. The memory device of claim 12, wherein dopants originating from the conductive material are present in portions of the channel layer adjacent to the conductive material.
14. The memory device of claim 9, wherein the conductive material comprises doped polysilicon.
15. The memory device of claim 9, wherein a width of the conductive material is greater than a width of the one or more first vertical structures and the one or more second vertical structures, such that the conductive material projects outward from the one or more first vertical structures and the one or more second vertical structures.

16. A memory device, comprising:

a substrate;
a first layer stack above the substrate and having alternating conductor and insulator layers;
one or more first vertical structures extending through the first layer stack;
a conductive material disposed on a top surface of the one or more first vertical structures;

an insulating layer disposed over the first layer stack and over the conductive material;
a second layer stack, disposed over the insulating layer and having alternating conductor and insulator layers; and
one or more second vertical structures extending through the second layer stack and through the insulating layer, and abutting a top surface of the conductive material.

17. The memory device of claim 16, wherein the one or more first vertical structures comprise one or more first NAND strings and the one or more second vertical structures comprise one or more second NAND strings.
18. The memory device of claim 17, wherein each of the one or more first NAND strings and the one or more second NAND strings includes a plurality of memory layers surrounding a core insulating material.
19. The memory device of claim 18, wherein the plurality of memory layers includes a stack consisting of a blocking layer, a storage layer, a tunneling layer, and a channel layer.
20. The memory device of claim 19, wherein dopants originating from the conductive material are present in portions of the channel layer adjacent to the conductive material.
21. The memory device of claim 16, wherein the conductive material comprises doped polysilicon.
22. The memory device of claim 16, wherein the insulating layer comprises aluminum oxide.
23. The memory device of claim 16, wherein the insulating layer surrounds a lower end of the one or more second vertical structures.
24. The memory device of claim 16, wherein a width of the conductive material is greater than a width of the one or more first vertical structures and the one or more second vertical structures, such that the conductive material projects outward from the one or more first vertical structures and the one or more second vertical structures.
25. An electronic system, comprising the memory device of any one of claims 1-24.
26. A method for forming a memory device, comprising:
 - forming a first layer stack over a substrate, the first layer stack having alternating sacrificial and dielectric layers;
 - forming one or more first openings through the first layer stack;
 - forming one or more first vertical structures in the one or more first openings;

removing a top portion of the one or more first vertical structures to form one or more first recesses;

depositing a conductive material within the one or more first recesses;

forming a second layer stack over the first layer stack, the second layer stack having alternating sacrificial and dielectric layers;

forming one or more second openings through the second layer stack and through a portion of the conductive material; and

forming one or more second vertical structures in the one or more second openings.

27. The method of claim 26, wherein forming the one or more first vertical structures comprises:

depositing a plurality of memory layers comprising a blocking layer, a storage layer, a tunneling layer, and a channel layer; and

depositing a core insulator material.

28. The method of claim 27, wherein the removing comprises:

etching back a portion of the core insulator material using a first etching process;

etching back a portion of the channel layer using a second etching process; and

etching back a portion of the blocking layer, the storage layer, and the tunneling layer using one or more other etching processes.

29. The method of claim 27, further comprising annealing the memory device such that dopants from the conductive material diffuse into the channel layer adjacent to the conductive material.

30. The method of claim 26, wherein depositing the conductive material comprises depositing polysilicon.

31. The method of claim 26, further comprising:

removing the sacrificial layers of the first layer stack and the second layer stack; and

replacing the removed sacrificial layers of the first layer stack and the second layer stack with conductive layers.

32. A method for forming a memory device, comprising:

forming a first layer stack over a substrate, the first layer stack having alternating sacrificial and dielectric layers;
forming one or more first openings through the first layer stack;
forming one or more first vertical structures in the one or more first openings;
removing a top portion of the one or more first vertical structures to form one or more first recesses;
depositing a conductive material within the one or more first recesses;
removing a top portion of the conductive material to form one or more second recesses;
depositing an insulating material in the one or more second recesses;
forming a second layer stack over the first layer stack, the second layer stack having alternating sacrificial and dielectric layers;
forming one or more second openings through the second layer stack and through a portion of the insulating material;
removing the insulating material; and
forming one or more second vertical structures in the one or more second openings.

33. The method of claim 32, wherein forming the one or more first vertical structures comprises:

depositing a plurality of memory layers comprising a blocking layer, a storage layer, a tunneling layer, and a channel layer; and
depositing a core insulator material.

34. The method of claim 33, wherein removing the top portion of the one or more first vertical structures comprises:

etching back a portion of the core insulator material using a first etching process;
etching back a portion of the channel layer using a second etching process; and
etching back a portion of the blocking layer, the storage layer, and the tunneling layer using one or more other etching processes.

35. The method of claim 33, further comprising annealing the memory device such that dopants from the conductive material diffuse into the channel layer adjacent to the conductive material.

36. The method of claim 32, wherein depositing the conductive material comprises depositing polysilicon.
37. The method of claim 32, wherein depositing the insulating material comprises depositing aluminum oxide.
38. The method of claim 32, further comprising:
- removing the sacrificial layers of the first layer stack and the second layer stack; and
 - replacing the removed sacrificial layers of the first layer stack and the second layer stack with conductive layers.
39. A method for forming a memory device, comprising:
- forming a first layer stack over a substrate, the first layer stack having alternating sacrificial and dielectric layers;
 - forming one or more first openings through the first layer stack;
 - forming one or more first vertical structures in the one or more first openings;
 - removing a top portion of the one or more first vertical structures to form one or more first recesses;
 - depositing a conductive material within the one or more first recesses;
 - depositing an insulating layer over the first layer stack and over the conductive material;
 - forming a second layer stack over the insulating layer, the second layer stack having alternating sacrificial and dielectric layers;
 - forming one or more second openings through the second layer stack and through a portion of the insulating layer;
 - removing additional portions of the insulating layer at a bottom of the one or more second openings; and
 - forming one or more second vertical structures in the one or more second openings.
40. The method of claim 39, wherein forming the one or more first vertical structures comprises:
- depositing a plurality of memory layers comprising a blocking layer, a storage layer, a tunneling layer, and a channel layer; and
 - depositing a core insulator material.

41. The method of claim 40, wherein removing the top portion of the one or more first vertical structures comprises:
- etching back a portion of the core insulator material using a first etching process;
 - etching back a portion of the channel layer using a second etching process; and
 - etching back a portion of the blocking layer, the storage layer, and the tunneling layer using one or more other etching processes.
42. The method of claim 40, further comprising annealing the memory device such that dopants from the conductive material diffuse into the channel layer adjacent to the conductive material.
43. The method of claim 39, wherein depositing the conductive material comprises depositing polysilicon.
44. The method of claim 39, wherein depositing the insulating layer comprises depositing aluminum oxide.
45. The method of claim 39, further comprising:
- removing the sacrificial layers of the first layer stack and the second layer stack; and
 - replacing the removed sacrificial layers of the first layer stack and the second layer stack with conductive layers.