

Description

Method for producing wiring arrangements with electrically conductive cross connections between the top side and underside of a substrate, and wiring arrangements having cross connections of this type

The number of connections on integrated circuits is becoming ever greater, while said integrated circuits are at the same time becoming miniaturized to an ever greater extent. The difficulties expected in the course of this increase in miniaturization in the application of solder paste and component mounting are intended to be overcome by new housing forms, where emphasis may be given here in particular to single-chip, few-chip or multi-chip modules in the ball grid array package (DE-Z productronic 5, 1994, pages 54, 55). These modules are based on a plated-through substrate, on which contact is made with the chips for example via bonding wires or by means of flip-chip mounting. The ball grid array (BGA) is situated on the underside of the substrate, and is often also referred to as a solder grid array or solder bump array. The ball grid array comprises solder studs arranged over the area on the underside of the substrate, which allow surface mounting on the printed circuit boards or assemblies. The arrangement of the solder studs over an area allows large numbers of connections to be realized, in a coarse grid of 1.27 mm, for example.

In the case of so-called MID technology (MID = Molded Interconnection Devices), injection-molded parts with integrated conductor runs are used instead of conventional printed circuits. High-quality thermoplastics suitable for the injection molding of three-dimensional substrates form the basis of this technology. By comparison with conventional substrate materials for printed circuits, such thermoplastics are distinguished by better mechanical, chemical,

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electrical and environmental properties. In the case of one specific direction of MID technology, so-called SIL technology (SIL = Spitzgießteile mit integrierten Leiterzügen [injection-molded parts with integrated conductor runs]), a metal layer applied to the

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injection-molded parts is structured without using the mask technique that is otherwise customary, by means of a special laser structuring method. In this case, a plurality of mechanical and electrical functions can be integrated in the three-dimensional injection-molded parts with structured metalization layer. The housing support function is simultaneously taken over by guides and snap-connections while the metalization layer, in addition to the wiring and connection function, also serves as electromagnetic shielding and provides for good heat dissipation. In order to produce electrically conductive cross connections between two wiring installations on mutually opposite surfaces of the injection-molded parts, corresponding plated-through holes are produced as early as during the injection-molding process. The inner walls of these plated-through holes are then likewise coated with a metal layer during the metalization of the injection-molded parts. Further details relating to the production of three-dimensional injection-molded parts with integrated conductor runs are revealed for example in DE-A-37 32 249 or EP-A-0 361 192.

According to a variant of MID technology which is disclosed in EP-A-0 645 953, a substrate is produced by injection molding and provided with a well and then a first conductor plane, a dielectric layer and a second conductor plane are successively produced on said substrate, whereupon an electronic component is incorporated in the well, the connections of the component are electrically conductively connected to assigned connection areas on the substrate, preferably by bonding, and then an encapsulation is formed for the component by the well being filled with plastic. A compact, thin structure with a high wiring density is produced. The recessed mounting and encapsulation of components in wells of the injection-molded substrate not only results in a thickness reduction but also attains optimum protection of the component and the connection wiring thereof.

WO-A-96 096 46 has disclosed a so-called polymer stud grid array (PSGA), which combines the advantages of a ball grid array (BGA) with the advantages of MID technology. The new design was called

5 a polymer stud grid array (PSGA) on the basis of the ball grid array (BGA), the term "polymer stud" being intended to refer to polymer studs which are concomitantly formed during the injection molding of the substrate. The new design is suitable for single-

10 chip, few-chip or multi-chip modules and comprises

- an injection-molded three-dimensional substrate made of an electrically insulating polymer,
- polymer studs which are arranged over the area on the underside of the substrate and are concomitantly
- 15 formed during the injection-molding process,
- external connections which are formed on the polymer studs by a solderable end surface,
- conductor runs which are formed at least on the underside of the substrate and connect the external
- 20 connections to internal connections, and
- at least one chip which is arranged on the substrate and whose connections are electrically conductively connected to the internal connections.

In addition to the simple and cost-effective

25 production of the polymer studs during the injection molding of the substrate, the production of the external connections on the polymer studs can also be carried out with minimal effort together with the production of the conductor runs, which is normal for

30 MID technology and SIL technology. The fine laser structuring which is preferred in SIL technology enables the external connections to be realized on the polymer studs with large numbers of connections in a very fine grid. It should be emphasized, furthermore,

35 that the thermal expansion of the polymer studs corresponds to the thermal expansions of the substrate and to that of the printed circuit board accommodating the module. Should any mechanical stresses occur, then the elastic properties of the polymer studs allow at

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least partial compensation. The dimensional stability
of the external connections formed on the polymer studs

also allows the reliability for repair and replacement to be considerably enhanced by comparison with ball grid arrays, whose connections are formed by solder studs. In the case of the polymer stud grid array, the polymer studs and the chip or the chips are usually arranged on the same side of the substrate. In the case of a substrate provided with plated-through holes, the polymer studs and the chip or the chips may perfectly well be arranged on different sides of the substrate as well. Such an arrangement of polymer studs and chips on opposite sides of the substrate is of interest particularly for large chips, which require a multiplicity of assigned external connections.

WO-A-89 00346 discloses single-chip modules which are suitable for surface mounting and are based on an injection-molded three-dimensional substrate with plated-through holes. In addition to these plated-through holes, during the injection-molding process, the substrate acquires a well, arranged centrally on the top side, and a multiplicity of polymer studs arranged in one or else in two peripheral rows on the underside. The chip arranged in the well on the top side is connected to assigned conductor tracks, which lead to the outside in the form of strips, via fine contact-making wires. These conductor tracks are then electrically conductively connected to the assigned, surface-metalized polymer studs over plated-through holes arranged in the outer region. If the edge regions of the substrate are then separated with cutting lines which pass centrally through the plated-through holes, then electrically conductive cross connections with a semicircular cross section are produced, which electrically conductively connect the outer ends of the conductor tracks arranged on the surface of the substrate to the assigned polymer studs arranged on the underside of the substrate.

The invention specified in claims 1 and 9 is based on the problem, in the context of MID technology,

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of simplifying the production of electrically
conductive cross connections between conductor

structures on the top side and underside of a substrate. In this case, the cross connections are intended to be suitable, in particular, also for the polymer stud grid arrays explained above.

5 The invention is based on the insight that cross connections can be produced at the same time as the laser structuring of the conductor structures provided that the cross connections are produced at edges with an oblique, roof-shaped or convex contour.

10 In this case, the cross connections can be produced both at ends of the substrate and at the inner walls of cutouts of the substrate. In the latter case, in contrast to conventional plated-through holes, it is possible to realize a plurality of conductor track-type

15 cross connections per cutout. In this case, however, the term cutout is also intended to be understood to mean appropriately formed plated-through holes for a single cross connection between the top side and underside. The structuring of the cross connections

20 according to the invention can be carried out with minimal outlay since no additional work operation is necessary.

Advantageous refinements of the method according to the invention are specified in claims 2 to

25 8.

Advantageous refinements of the wiring arrangement according to the invention are specified in claims 10 to 12.

The refinement according to claim 2 enables the

30 substrate to be produced simply and in a manner suitable for mass production, in particular, by means of injection molding.

In contrast to a convex contour, the contours specified in claims 3 and 10 facilitate the laser

35 structuring of the cross connections by virtue of their pronounced edges. In accordance with claims 4 and 11, effective laser structuring of the cross connections is ensured in this case

through angles of inclination of at least 110° with respect to the horizontal and/or at least 20° with respect to the vertical.

The refinement according to claim 5 enables the
5 cross connections according to the invention to be realized in polymer stud grid arrays.

The development according to claim 6 has the advantage that, for the application of the metallization layer, it is possible to resort to
10 technologies which have long proven their worth in the production of printed circuits.

Although the method according to the invention can, in principle, also be carried out using the semiadditive technique, the subtractive technique in
15 accordance with claim 7 affords quite a few advantages. In addition to the simple and economical production of the desired conductor patterns, emphasis may be given here in particular to the simple laser structuring of an etching resist. In accordance with claim 8, the
20 etching resist can in this case be applied in a particularly simple manner by chemical deposition or electrodeposition of tin or tin-lead.

In accordance with claim 12, the cross connections according to the invention can preferably
25 be used in a polymer stud grid array with a chip arranged on the top side of the substrate. The arrangement of the chip on the top side of the substrate and the arrangement of the polymer studs on the underside of the substrate in this case result in
30 ideal preconditions for realizing so-called chip scale packages, in the case of which the dimensions of the array essentially correspond to the dimensions of the chip.

Exemplary embodiments of the invention are
35 illustrated in the drawing and are described in more detail below.

In the figures:

- Figure 1 shows a cross section through a substrate with a roof-shaped contour of the edges relevant to cross connections,
- 5 Figure 2 shows a cross section through a substrate with an oblique contour of the edges relevant to cross connections,
- Figure 3 shows a cross section through a substrate with a convex contour of the edges relevant to cross connections,
- 10 Figure 4 shows the substrate as shown in Figure 1 after the application of a metallization layer,
- Figure 5 shows the substrate as shown in Figure 4 after the application of an etching resist,
- 15 Figure 6 shows a cross section through a roof-shaped contour of the substrate in accordance with the line VI-VI in Figure 5,
- Figure 7 shows the laser structuring of the etching resist layer in the case of the cross section of the roof-shaped contour as shown in Figure 6,
- 20 Figure 8 shows the formation of the cross connections in the case of the cross section of the roof-shaped contour as shown in Figure 6,
- 25 Figure 9 shows a partial plan view of the top side of the substrate with conductor tracks and cross connections,
- Figure 10 shows a partial plan view of the underside of the substrate with conductor tracks and cross connections, and
- 30 Figure 11 shows a side view of the substrate formed as a polymer stud grid array.

Figure 1 shows a truncated cross section through a substrate S1, whose discernible end has a roof-shaped contour K1. In the region of a cutout A1 of the substrate S1, which cutout may have a circular, oval, rectangular or square shape, the inner wall likewise has a roof-shaped contour K1. The top side and underside of the substrate S1 are designated by O and U, respectively. The roof-shaped contour K1 illustrated is provided for the production of cross connections that is yet to be explained with reference to Figures 4 to 10. The angle of inclination between the roof-shaped contour K1 and the top side O and/or underside U is designated by α , where α is greater than 90° .

The substrate 1, including the cutout A1 and the roof-shaped contours K1, is produced by injection molding, suitable substrate materials being thermoplastics which are resistant to high temperatures, such as polyetherimide, polyether sulfone or polyamide.

Figure 2 shows a truncated cross section through a substrate S2, which, in contrast to the substrate illustrated in Figure 1, has an oblique contour K2 in the region of an end and in the region of a cutout A2. The angle of inclination between the oblique contour K2 and the top side O of the substrate S2 is again designated by α , where α is greater than 90° in this case as well.

Figure 3 shows a truncated cross section through a substrate S3, which, in contrast to the substrates illustrated in Figures 1 and 2, has a convex contour K3 in the region of an end and in the region of a cutout A3.

By virtue of their special contours K1, K2 and K3, the substrates S1, S2 and S3 illustrated in Figures 1 and 3 enable laser structuring of metallization layers applied there. In the case of the contours K1 and K3, this laser structuring

is carried out in order to form cross connections from the top side O and from the underside U. In the case of the contour K2, the laser structuring of cross connections is carried out only from the top side O. In
5 a departure from the exemplary embodiment illustrated in Figure 1, the roof-shaped contour K1 can also have an asymmetrical roof shape.

The substrate S1 illustrated in Figure 1 is firstly subjected to a series of customary
10 pretreatments, in particular pickling, cleaning, seeding and activation of the seeding. Afterwards, in accordance with Figure 4, a metallization layer M is applied to the substrate S1 over the whole area by means of the electroless deposition of copper and
15 subsequent electrodeposition of copper.

In accordance with Figure 5, an etching resist AR is subsequently applied to the metallization layer M by electroless- or by electrodeposition of tin.

Figure 6 shows a truncated cross section
20 through the roof-shaped contour K1 of the substrate S1 in accordance with the line VI-VI in Figure 5.

In accordance with Figure 7, the etching resist AR is removed again by structuring by means of a laser beam LS in those regions of the roof-shaped contour K1
25 (cf. Figure 5) which do not correspond to the later cross connections. In this case, the laser beam LS is not oriented perpendicularly to the surface of the roof-shaped contour K1 but perpendicularly to the surface O of the substrate S1 (cf. Figure 5). Those
30 regions of the metallization layer M which are uncovered by the laser structuring of the etching resist AR are then etched away down to the surface of the substrate S1 as shown in Figure 8, conductor track-type cross connections Q being produced.

35 Figure 9 shows a partial plan view of the top side O of the substrate S1 and the conductor tracks L

formed thereon, which merge in an aligned manner with the assigned cross connections Q in the region of the roof-shaped contour K1. The production of the conductor tracks L on the top side O of the substrate S1 takes place at the same time as the production (which can be seen from Figure 7) of the adjoining cross connections Q by laser structuring of the etching resist AR and subsequent etching away of the uncovered regions of the metallization layer M.

10 In a manner corresponding to Figure 9, Figure 10 shows a partial plan view of the underside U of the substrate S1 and the conductor tracks L formed thereon, which merge in an aligned manner with the assigned cross connections Q in the region of the roof-shaped contour K1. The production of the conductor tracks L on the underside U of the substrate S1 takes place at the same time as the production of the adjoining connections Q by laser structuring of the etching resist AR and subsequent etching away of the uncovered regions of the metallization layer M. The laser structuring is thereby performed by a laser beam LS oriented perpendicularly to the underside U of the substrate S1 (cf. Figure 7).

25 Figure 11 shows a side view of the substrate S1 with conductor tracks L, cross connections Q in the region of the roof-shaped contour K1 and with the already mentioned polymer studs H arranged over the area on the underside U. A chip C is applied to the top side O of the substrate S1, contact being made with said chip either using the wire-bonding technology with bonding wires B as illustrated on the left or using the flip-chip technology with connections AS as illustrated on the right.

35 In the case of wire-bonding technology, the chip C is joined to the top side O of the substrate S by means of an adhesive layer KL.

Figure 11 clearly shows that the individual connections of the chip C are electrically conductively connected to assigned polymer studs H via conductor tracks L on the top side O, via cross connections Q at
5 the ends in the region of the roof-shaped contour K1,

and via conductor tracks L on the underside U. A solderable end surface is applied to the underside of the metallized polymer studs H, said end surface being formed for example by a layer sequence of nickel and
5 gold.

The structure illustrated in Figure 11 is a polymer stud grid array, which is designated altogether by PSGA. Further details of such polymer stud grid arrays are revealed in WO-A 96 09 646, for example.

10 In the case of the polymer stud grid array PSGA as shown in Figure 11, the external dimensions of the chip C and substrate S1 are approximately the same size. Consequently, a form of housing is involved which is usually referred to as a chip scale package. It can
15 also clearly be discerned that the cross connections Q at the ends in the region of the roof-shaped contour K1, being structured extremely finely, enable the entire polymer stud grid array PSGA to be configured extremely compactly, and thus make a crucial
20 contribution to the realization of the chip scale package.

Patent claims



1. A method for producing wiring arrangements with electrically conductive cross connections (Q) between
5 conductor structures on the top side (O) and on the underside (U) of a substrate (S1; S2; S3), having the following steps:
- a) Production of the substrate (S1; S2; S3) from an electrically insulating plastic by injection
10 molding, transfer molding or compression molding, at least one end of the substrate (S1; S2; S3) and/or at least one inner wall of a cutout (A1; A2; A3) of the substrate (S1; S2; S3) acquiring an oblique, roof-shaped or convex contour (K1; K2; K3);
- 15 b) application of a metallization layer (M) to the substrate (S1; S2; S3);
- c) partial removal of the metallization layer (M) by structuring by means of a laser beam (LS) for the
20 purpose of forming the conductor structures on the top side (O) and on the underside (U) of the substrate (S1; S2; S3) and for the purpose of forming conductor track-type cross connections (Q) in the region of at least one end of the substrate
25 (S1; S2; S3) and/or at least one inner wall of a cutout (A1; A2; A3) of the substrate (S1; S2; S3).
2. The method as claimed in claim 1, characterized in that the substrate (S1; S2; S3) is produced by injection molding.
- 30 3. The method as claimed in claim 1 or 2, characterized in that at least one end of the substrate (S1; S2) and/or at least one inner wall of a cutout (A1; A2) of the substrate (S1; S2) acquires an oblique or roof-shaped contour (K1; K2).
- 35 4. The method as claimed in claim 3, characterized in that the end or the inner wall is inclined



by an angle (α) of at least 110° with respect to the top side (O) or the underside (U) of the substrate (S1; S2).

5. The method as claimed in one of the preceding
5 claims,

characterized in that, in step a), polymer studs (H) which are arranged over the area on the underside (U) of the substrate (S1) are concomitantly formed during the production of said substrate, and in that, after
10 the application of the metallization layer (M), a solderable end surface (E) is applied to the polymer studs (H).

6. The method as claimed in one of the preceding claims,
15 characterized in that the metallization layer (M) is applied to the substrate (S1) by electroless- and electrodeposition of copper.

7. The method as claimed in one of the preceding claims,
20 characterized in that, after step b), an etching resist (AR) is applied to the metallization layer (M), in that the etching resist (AR) is removed again by structuring by means of a laser beam (LS) in regions not corresponding to the desired conductor pattern, and in
25 that the uncovered regions of the metallization layer (M) are then etched away down to the surface of the substrate (S1).

8. The method as claimed in claim 7,
characterized in that the etching resist (AR) is
30 applied by the electrodeposition of tin or tin-lead.

9. A wiring arrangement with electrically conductive cross connections (Q) between conductor structures on the top side (O) and on the underside (U) of a substrate (S1; S2; S3), where

35 - at least one end of the substrate (S1; S2; S3) and/or at least one inner wall of a cutout (A1; A2; A3) of the substrate (S1; S2; S3) has an

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oblique, roof-shaped or convex contour (K1; K2;
K3), and where



- 5 the cross connections (Q) are in the form of conductor tracks and arranged in the region of at least one end of the substrate (S1; S2; S3) and/or at least one inner wall of a cutout (A1; A2; A3) of the substrate (S1; S2; S3).
- 10 The wiring arrangement as claimed in claim 9, characterized in that at least one end of the substrate (S1; S2) and/or at least one inner wall of a cutout (A1; A2) of the substrate (S1; S2) has an oblique or roof-shaped contour (K1; K2).
- 15 The method arrangement as claimed in claim 9, characterized in that the end or the inner wall is inclined by an angle (α) of at least 110° with respect to the top side (O) or the underside (U) of the substrate (S1; S2).
- 20 The wiring arrangement as claimed in claim 9 or 10, having
- polymer studs (H) which are formed integrally and arranged over the area on the underside (U) of the substrate (S1),
 - a chip (C) arranged on the top side (O) of the substrate (S1) using wire bonding technology or using flip-chip technology, and having
 - a solderable end surface (E) applied to the polymer studs (H), where
 - the solderable end surface (E) of a polymer stud (H) is electrically conductively connected to an assigned connection (AS) of the chip (C) in each case via a conductor track (L) on the underside (U) of the substrate (S1), a cross connection (Q) and a conductor track (L) on the top side (O) of the substrate (S1).