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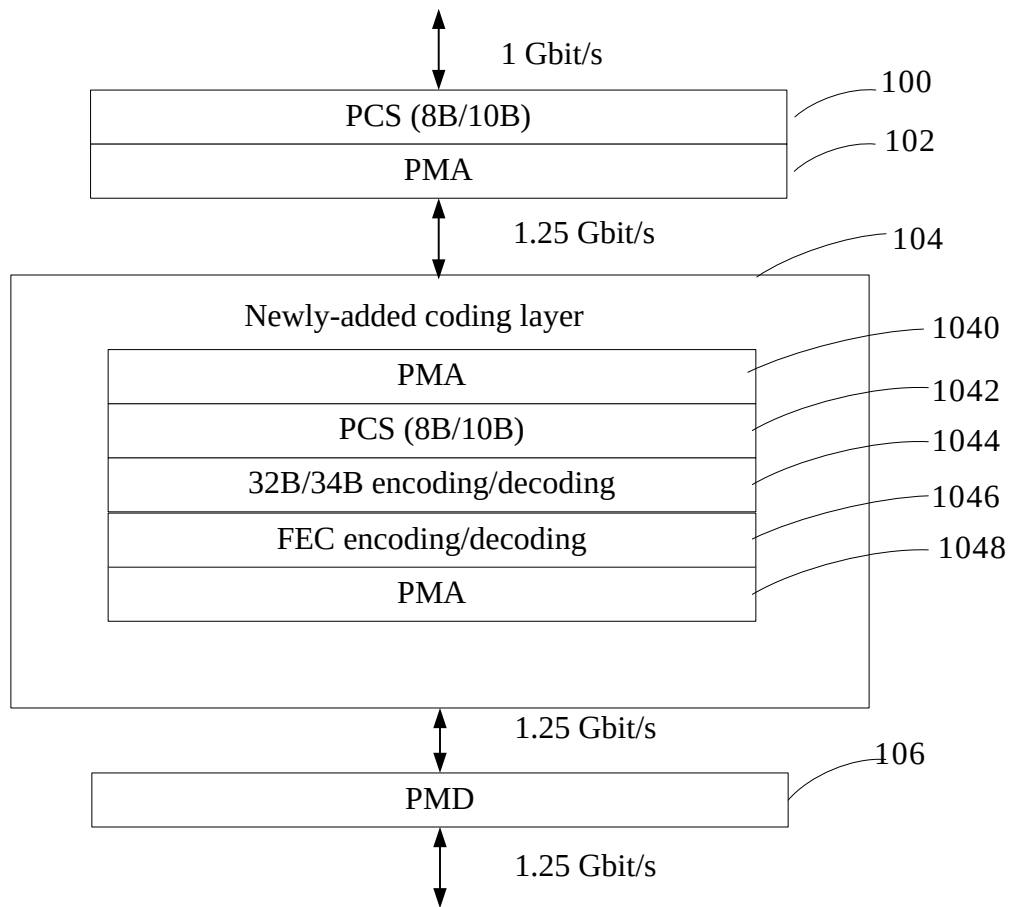


FIG. 1

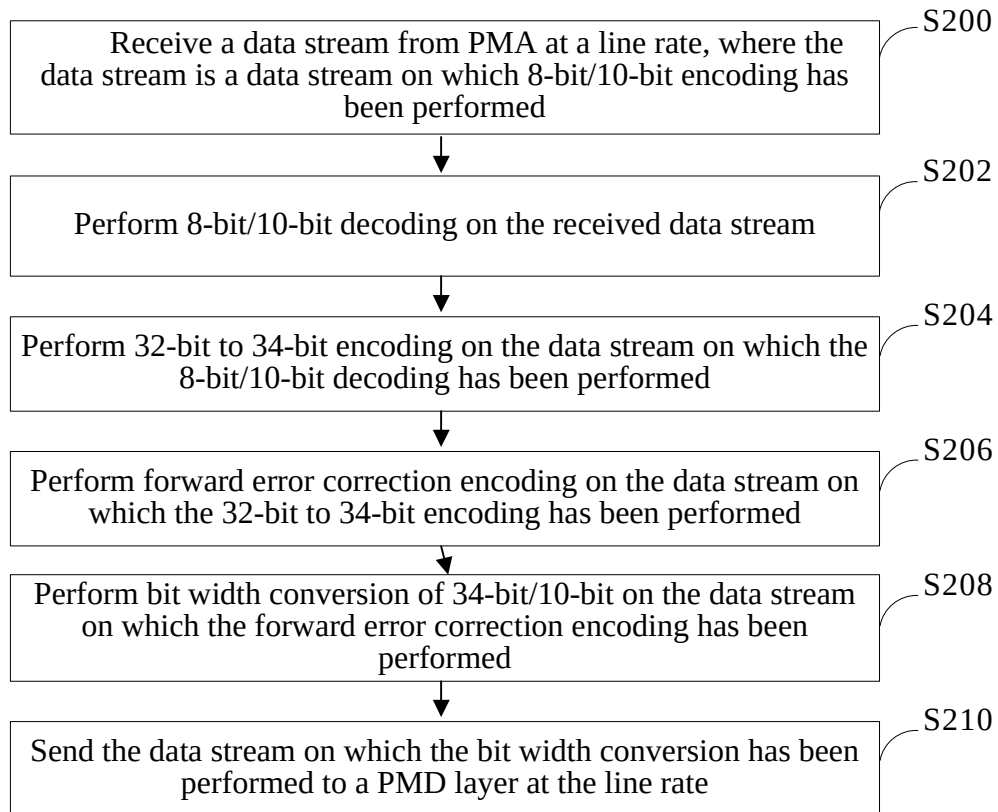


FIG. 2

32 bits	34 bits								
Input data	First synchr onizati on head	Data							
	0 1	2 ... 5	6 ... 9	10...13	14...17	18...21	22...25	26...29	30...33
D0D1D2 D3	01	D0		D1		D2		D3	
Input data	Second synchr onizati on head	Mapping code	Code						
C0D1D2 D3	10	1000	K0	D1		D2		D3	
D0C1D2 D3	10	0100	D0		K1	D2		D3	
D0D1C2 D3	10	0010	D0		D1		K2	D3	
D0D1D2 C3	10	0001	D0		D1		D2		K3
C0D1C2 D3	10	1010	K0	K1	D2		D3		Rsvd
.....	...								
C0C1C2 C3	10	1111	K0	K1	K2	K3	Rsvd (0x555)		

FIG. 3

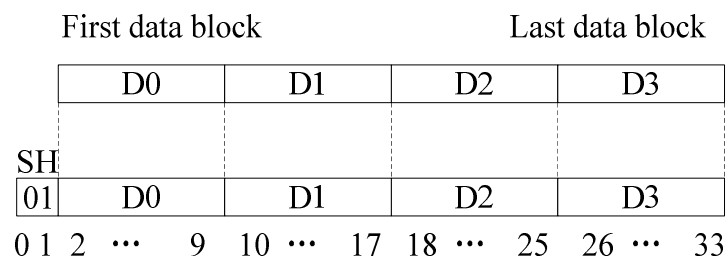


FIG. 4

First control character block(Binary)	Second control character block (Binary)
000 11100	0000
001 11100	0001
010 11100	0010
011 11100	0011
100 11100	0100
101 11100	0101
110 11100	0110
111 11100	0111
111 10111	1000
111 11011	1001
111 11101	1010
111 11110	1011

FIG. 5

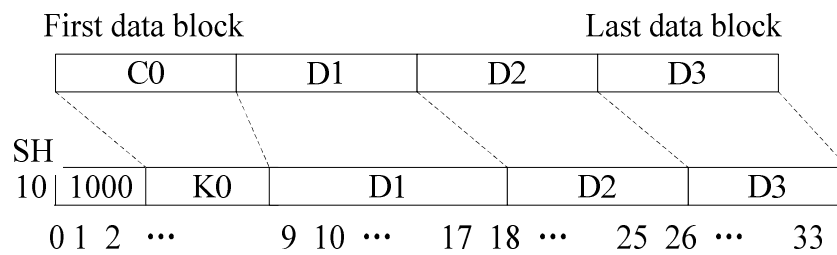


FIG. 6

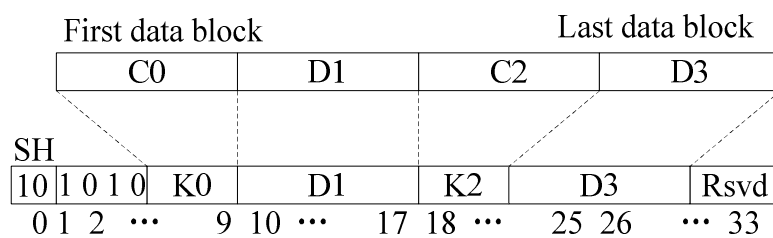


FIG. 7

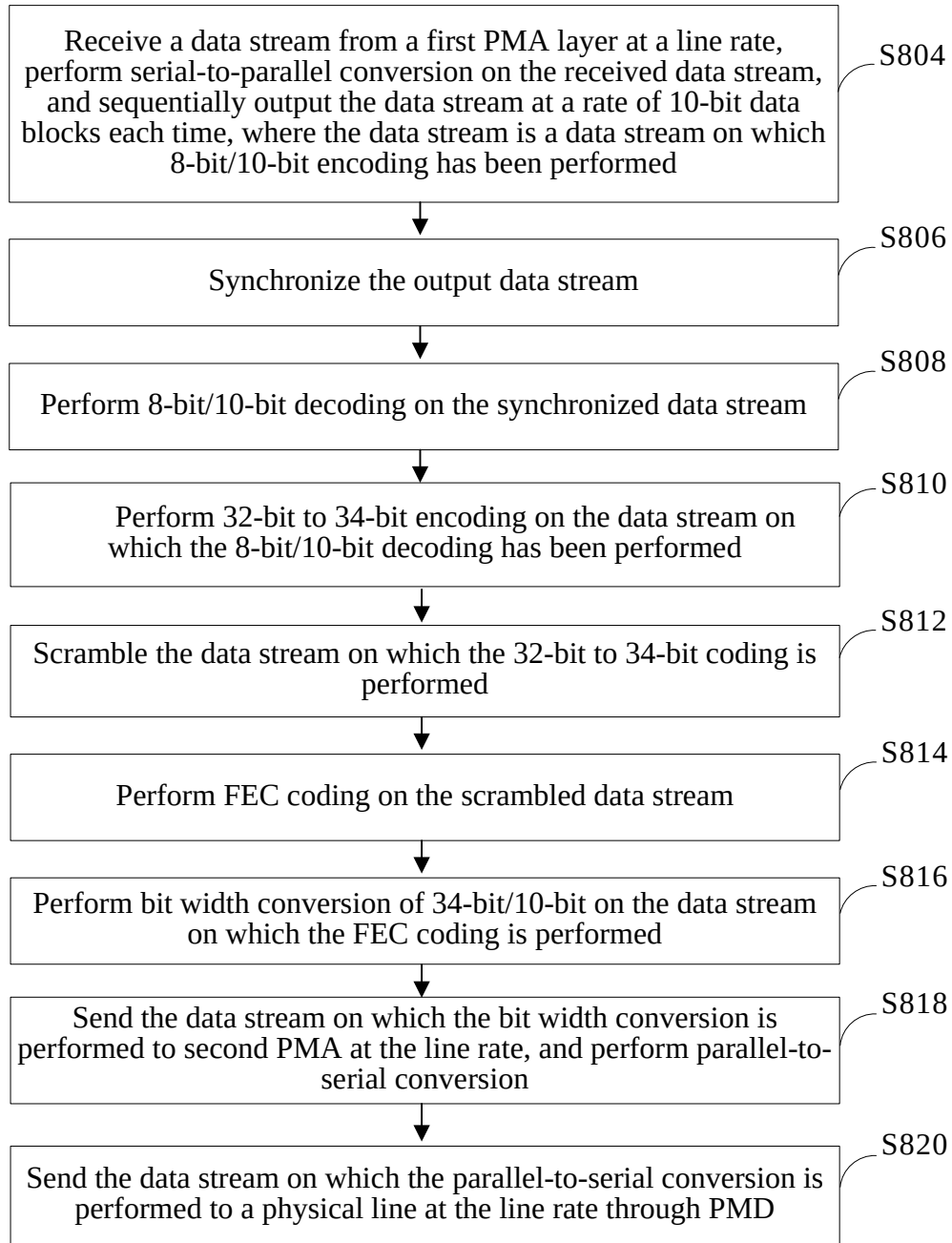


FIG. 8

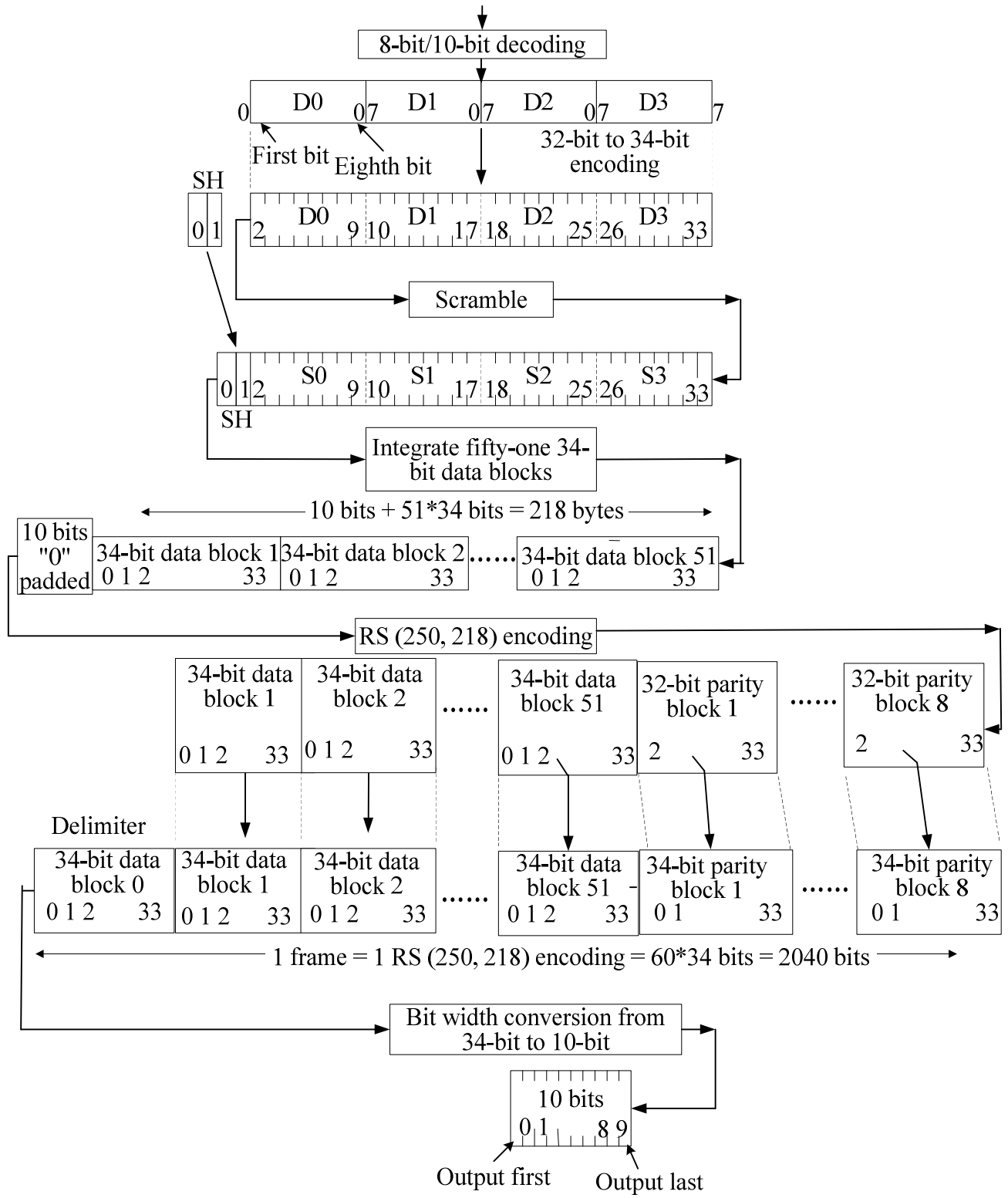


FIG. 9

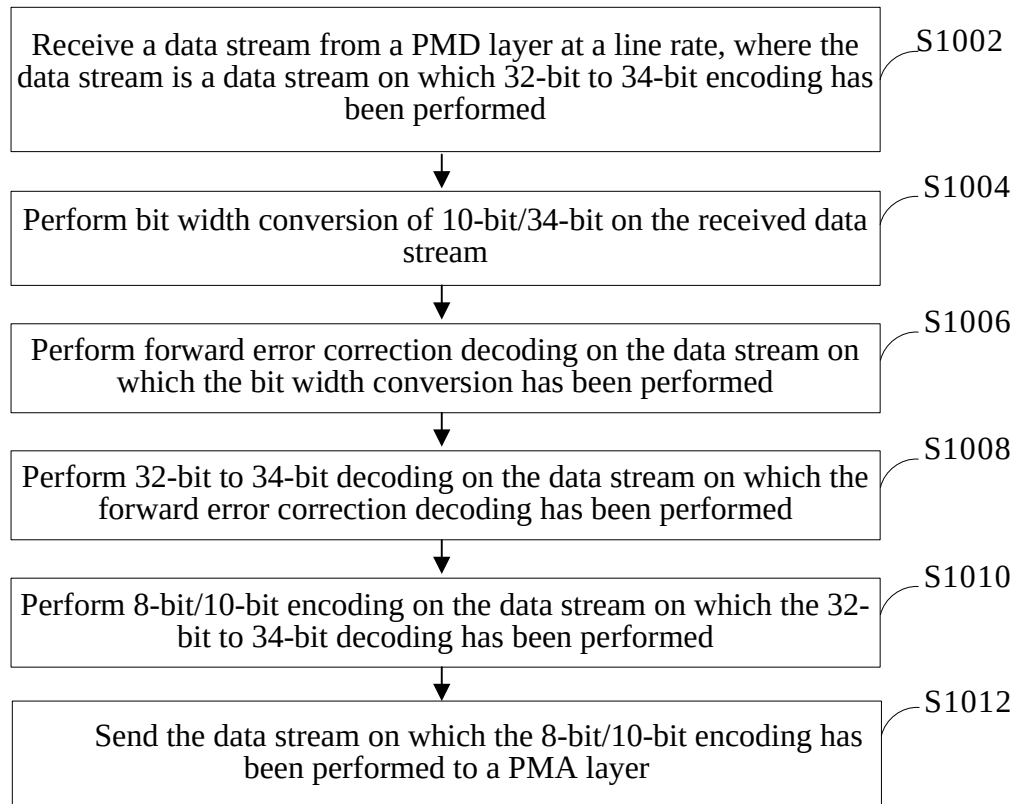


FIG. 10

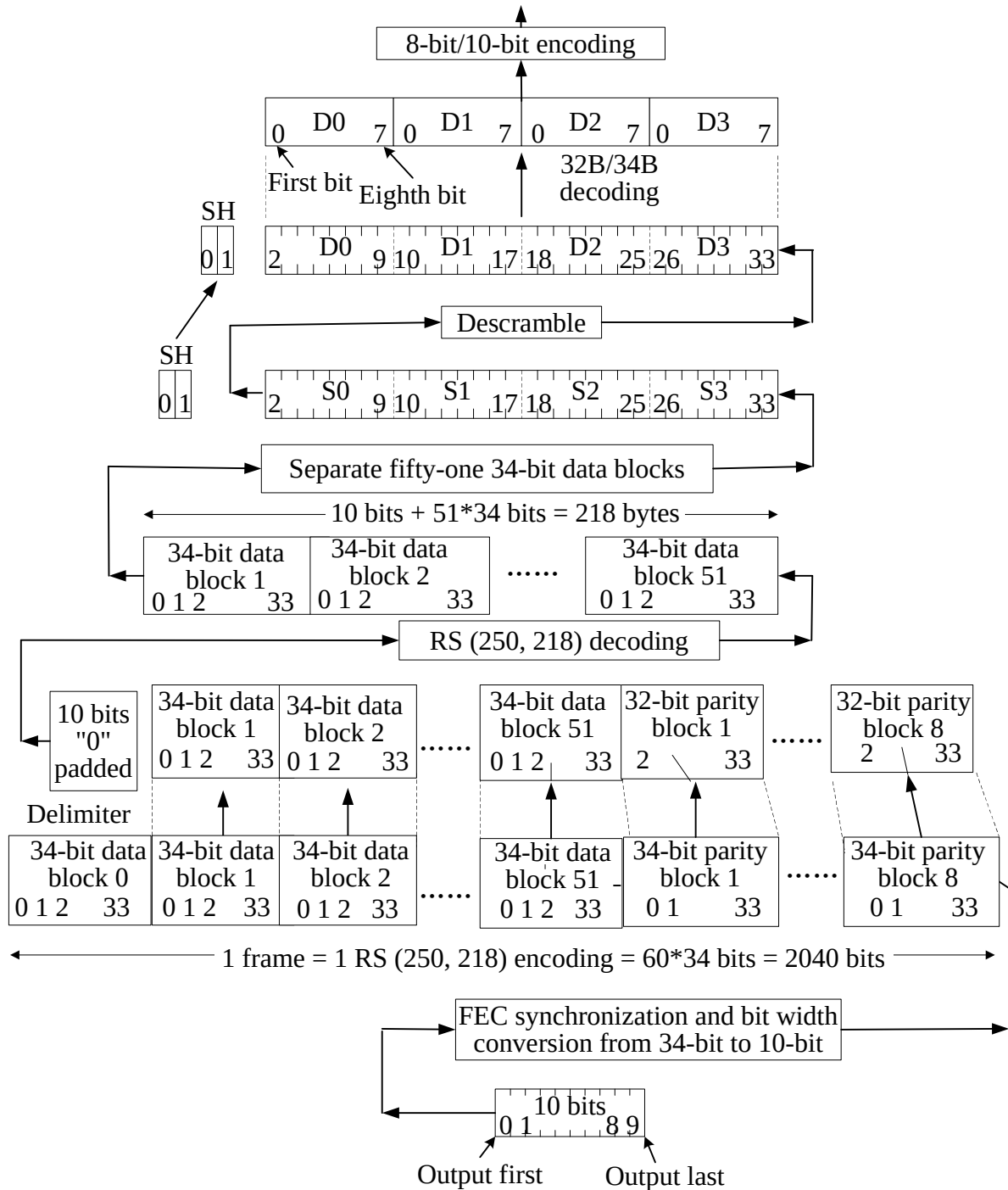


FIG. 11

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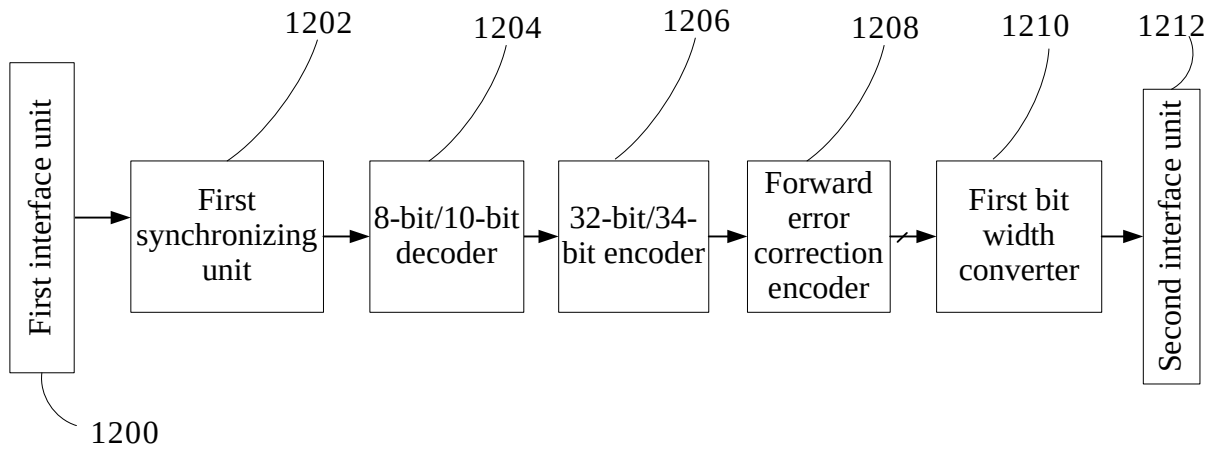


FIG. 12

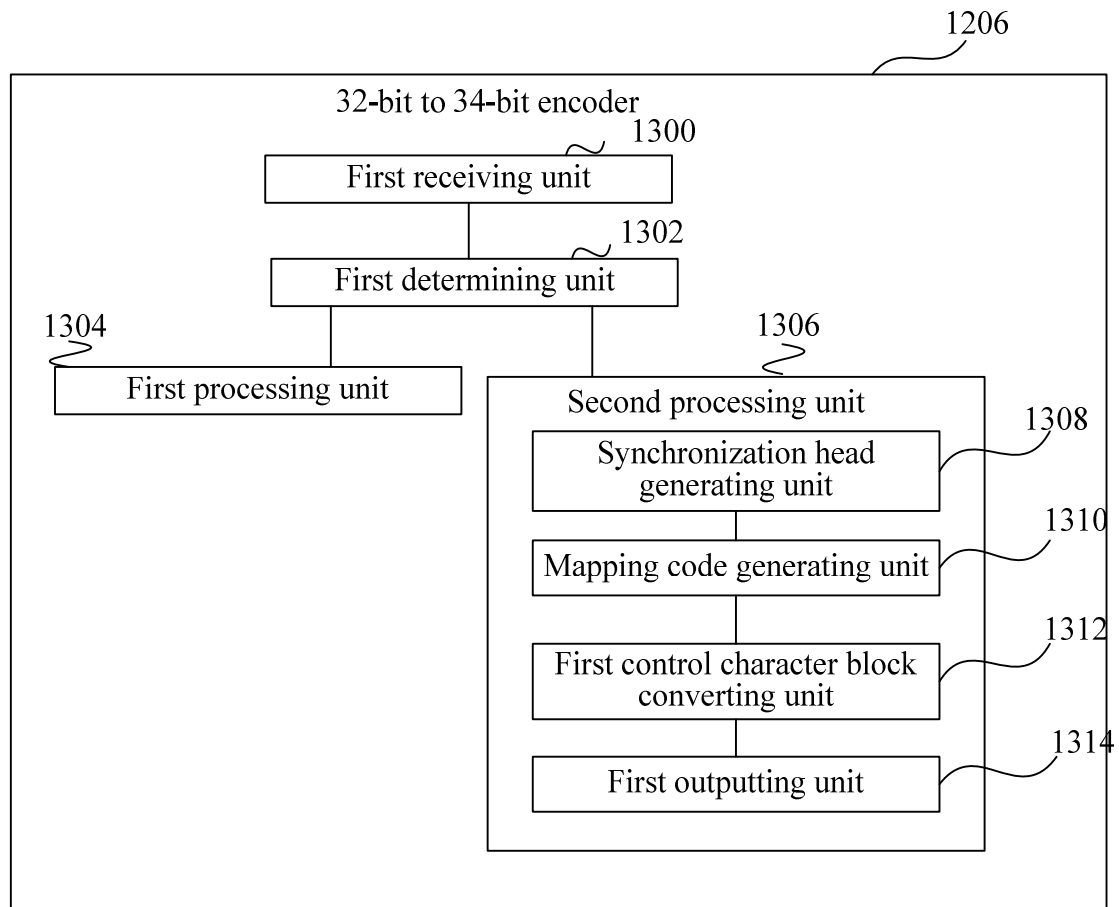


FIG. 13

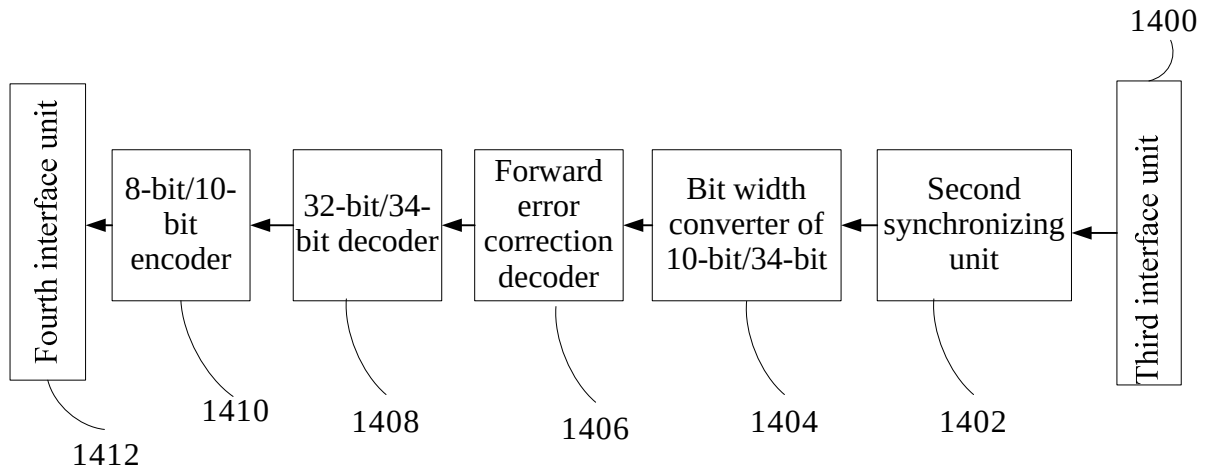


FIG. 14

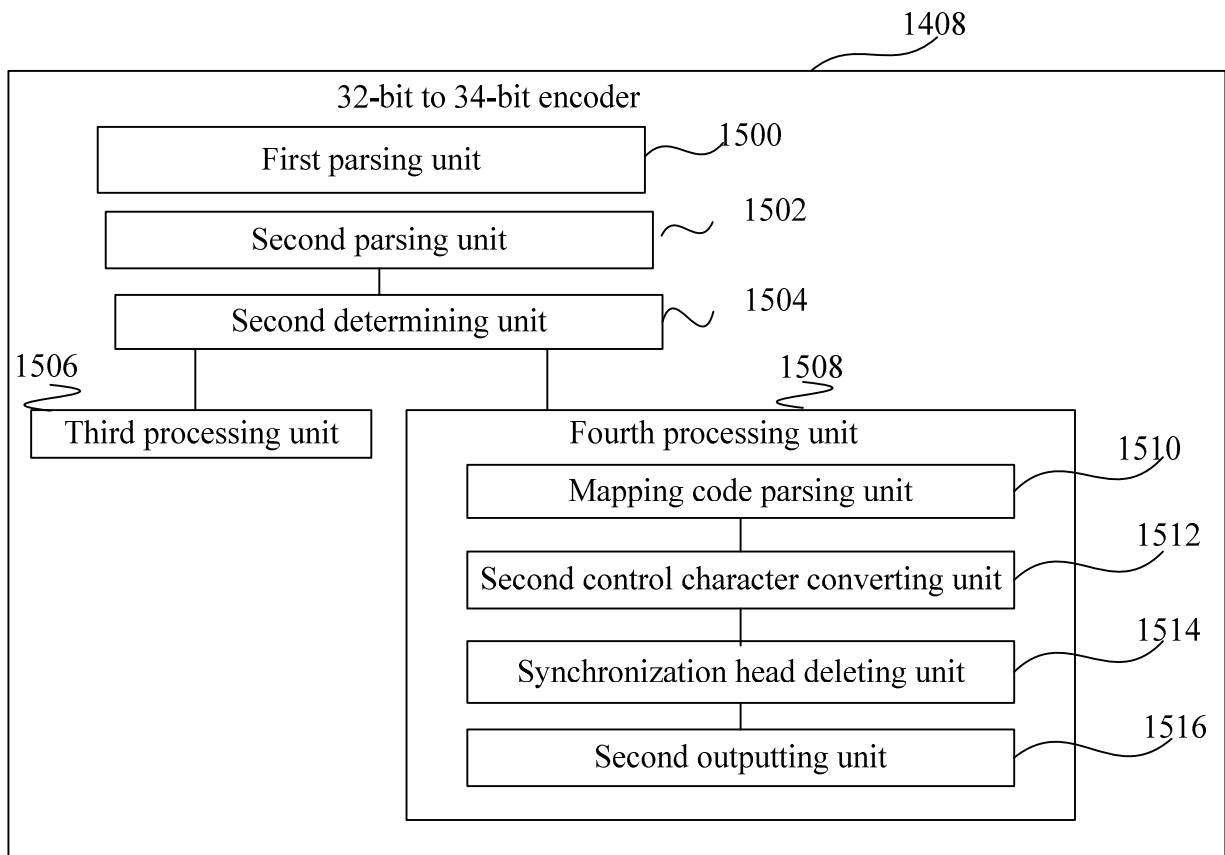


FIG. 15

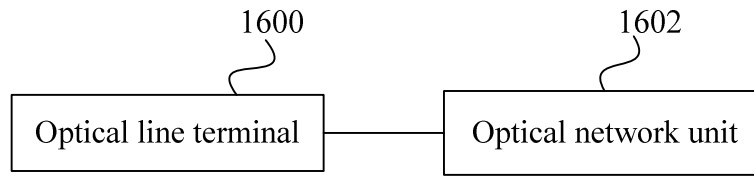


FIG. 16

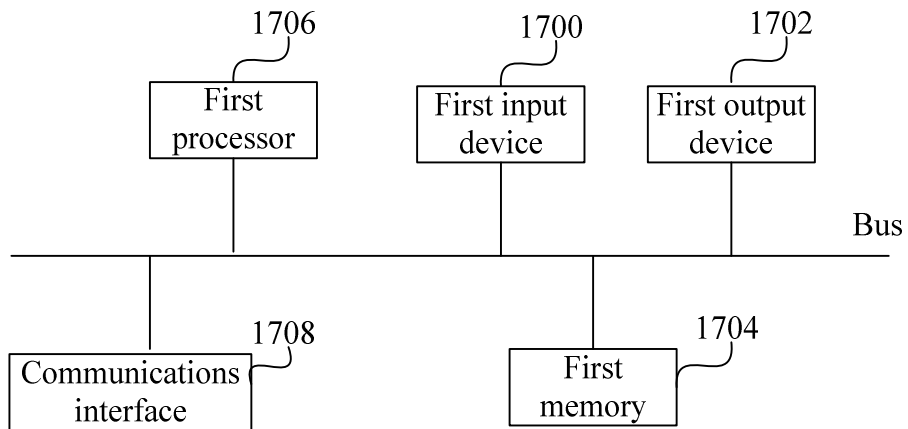


FIG. 17

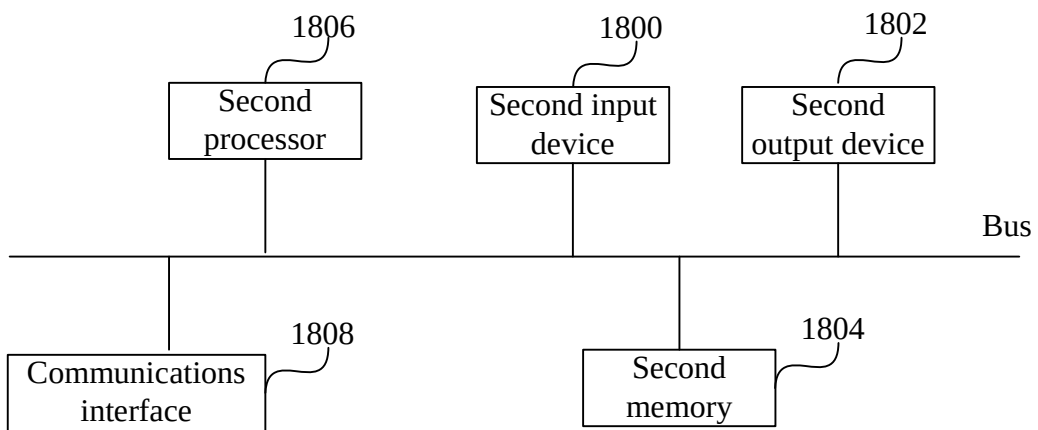


FIG. 18