WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor memory device, comprising:

etching a substrate wherein a trench is formed that crosses active regions of the substrate;

forming a gate insulating layer on bottom and side surfaces of the trench;

forming a first gate electrode on the gate insulating layer that fills a lower portion of the trench;

oxidizing a top surface of the first gate electrode wherein a preliminary barrier layer is formed;

nitrifying the preliminary barrier layer wherein a barrier layer is formed; and

forming a second gate electrode on the barrier layer that fills an upper portion of the trench; and

wherein nitrifying the preliminary barrier layer infiltrates nitrogen atoms into crystalline defects of the first gate electrode.

2. The method of claim 1, wherein nitrifying the preliminary barrier layer nitrifies an exposed portion of the gate insulating layer located above the first gate electrode.

3. The method of claim 1, wherein nitrifying the preliminary barrier layer nitrifies an upper portion of the first gate electrode.

4. The method of claim 1, wherein

during nitrification of the preliminary barrier layer, an upper portion of the first gate electrode is partially nitrified.

5. The method of claim 1, further comprising etching the gate insulating layer before forming the second gate electrode, wherein a thickness of a portion of the gate insulating layer exposed above the barrier layer is reduced.

6. The method of claim 1, wherein the first gate electrode comprises a first metal, and the barrier layer comprises an oxynitride of the first metal.

7. The method of claim 1, further comprising forming a liner layer that covers a top surface of the barrier layer and a side surface of the gate insulating layer exposed above the barrier layer, before forming the second gate electrode.

8. The method of claim 1, further comprising forming a capping layer on the second gate electrode that fills a remaining region of the trench.

9. A semiconductor memory device, comprising:

a semiconductor substrate that includes a trench;

a gate insulating layer disposed in the trench that covers bottom and inner side surfaces of the trench;

a first gate electrode disposed in a lower portion of the trench, the first gate electrode including a first metal;

a second gate electrode disposed in the trench and on the first gate electrode; and

a barrier layer disposed between the first and second gate electrodes, the barrier layer including an oxynitride of the first metal,

wherein the second gate electrode has a work-function that is less than the work-function of the first gate electrode; and

wherein a nitrogen concentration of a portion of the gate insulating layer adjacent to the second gate electrode is greater than the nitrogen concentration of a portion of the gate insulating layer adjacent to the first gate electrode.

10. The device of claim 9, wherein the gate insulating layer has a first portion adjacent to the first gate electrode and a second portion adjacent to the second gate electrode, and

when measured in a direction perpendicular to a side surface of the trench, the first portion is thicker than the second portion.

11. The device of claim 10, wherein a thickness of the first portion is about 40% to 70% greater than a thickness of the second portion.

12. The device of claim 9, wherein the second gate electrode is wider than the first gate electrode.

13. The device of claim 9, wherein a thickness of the barrier layer ranges from 1 Å to 30 Å.

14. The device of claim 9, wherein the second gate electrode comprises poly-silicon doped with n-type impurities.

15. The device of claim 9, further comprising a liner layer disposed between the barrier layer and the second gate electrode,

wherein the liner layer extends into a space between the gate insulating layer and the second gate electrode.

16. The device of claim 9, wherein the substrate further comprises:

active regions surrounded by a device isolation layer, wherein the active regions extend in a direction that crosses the trenches; and

doped regions formed in the active regions,

wherein the doped regions comprise first doped regions disposed between the trenches, and second doped regions disposed between the trenches and the device isolation layer.

17. The device of claim 16, further comprising

bit lines disposed on the substrate and connected to the first doped regions; and

capacitors disposed on the substrate and connected to the second doped regions.

18. A semiconductor memory device, comprising:

a substrate that includes active regions surrounded by a device isolation layer, the active regions extending in a first direction;

gate lines buried in trenches formed in an upper portion of the substrate, wherein the gate lines cross the active regions in a second direction that crosses the first direction and divide the active regions into first and second doped regions;

a gate insulating layer buried in the trenches, wherein the gate insulating layer is interposed between the gate lines and the active regions and between the gate lines and the device isolation layer; and

a bit line disposed on the gate lines that extends in a third direction that crosses both of the first and second directions,

wherein each of the gate lines comprises:

a first gate electrode disposed in a lower portion of the trench, wherein a top surface of the first gate electrode includes oxygen and nitrogen atoms;

a second gate electrode disposed on the first gate electrode; and

wherein a nitrogen concentration of a portion of the gate insulating layer adjacent to the second gate electrode is greater than the nitrogen concentration of a portion of the gate insulating layer adjacent to the first gate electrode.