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(71)(72) Applicant and Inventor: CHAPMAN, David, C. [US/US]; 2655 Keystone Avenue #41, Santa Clara, CA 95051 (US).

(74) Agents: BECKER, Edward, A. et al.; McDermott, Will & Emery, 600 13th Street, N.W., Washington, DC 20005–3096 (US).

(54) Title: APPROACH FOR ROUTING AN INTEGRATED CIRCUIT

(57) Abstract

A computer–implemented approach for routing an integrated circuit using non–orthogonal routing is accomplished during two phases: a global routing phase and a detailed routing phase. During global routing, routing indicators, in the form of hint polygons, are added to the integrated circuit layout and strategy lists, that include bias directions and straying limits, are generated for the new wires to be added. The hint polygons and strategy lists are used during detailed routing to aid in placing the new wires. If obstacle conflicts or insufficient space problems prevent the detailed routing of a new wire, then an obstacle resolution portion of global routing is used to resolve the obstacle conflict and/or provide additional space in the integrated circuit layout to route the new wires. Obstacle resolution includes, without limitation, moving or changing layout geometry, changing or add hint polygons, changing the routing strategy by changing the bias direction and/or adjusting straying limits, inserting one or more layer changes, instructing the detailed router to backup and insert a bend, ripping–up, and rerouting one or more wires, or routing the wire from the destination connection point. Also, a tight routing approach may be employed to accommodate constructing routing paths in tight layout areas. Object specific design rule checks are employed to increase routing flexibility optimize routing performance. "On–the–fly" design rule checks are performed on portions of routing paths as the routing paths are being constructed.