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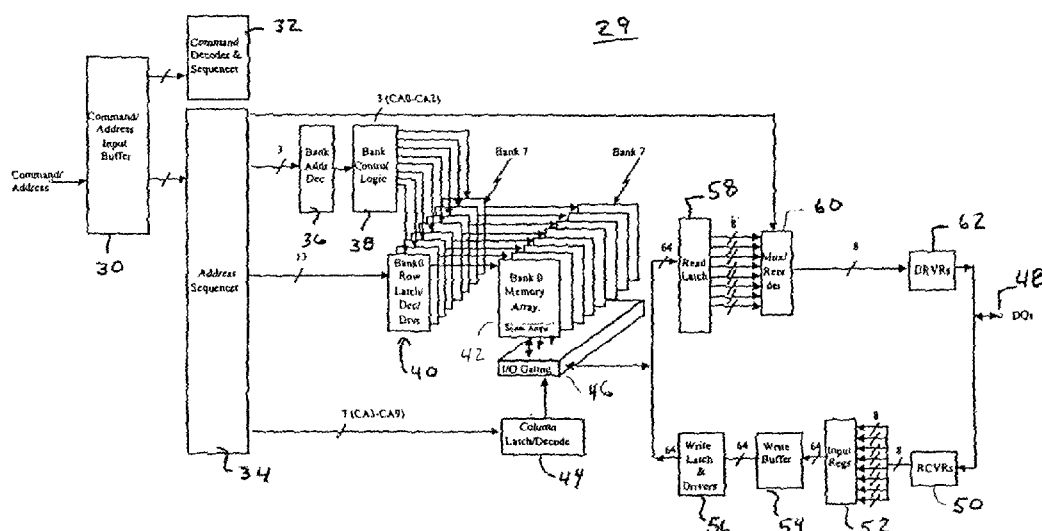
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(54) Title: MEMORY DEVICE HAVING DIFFERENT BURST ORDER ADDRESSING FOR READ AND WRITE OPERATIONS



(57) Abstract: An addressing scheme and associated hardware allows for two different types of access, one for reading and one for writing, to take place. A memory device constructed according to the invention comprises a plurality of arrays of memory cells. Peripheral devices are provided for reading information out of and for writing information into the plurality of memory cells. The peripheral devices include a reorder circuit responsive to certain address bits for ordering bits received from the plurality of arrays and an address sequencer for routing certain of the address bits to the reorder circuit during a read operation. The method of the present invention comprises reordering a block of n-bit words output from a memory array according to information in certain address bits before outputting at least one n-bit word from a memory device.