Claims

What is claimed is:

1. A method for fabricating a semiconductor device, comprising:

providing a substrate comprising a core region, a low noise amplifier (LNA) region, an input/output (I/O) region, and a power amplifier (PA) region;

forming a first gate structure on the LNA region, a second gate structure on the PA region, a third gate structure on the core region, and a fourth gate structure on the I/O region;

forming an interlayer dielectric (ILD) layer on the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure;

performing a replacement metal gate (RMG) process to transform the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure into a first metal gate, a second metal gate, a third metal gate, and a fourth metal gate respectively; and

forming a first hard mask on the first gate structure and a second hard mask on the second gate structure, wherein a width of the first hard mask is greater than a width of the first gate structure.

2. The method of claim 1, further comprising:

forming a first contact etch stop layer (CESL) adjacent to one side of the first gate structure and a second CESL adjacent to another side of the first gate structure before performing the RMG process.

3. The method of claim 2, wherein the width of the first hard mask is greater than a distance between the first CESL to the second CESL.

4. The method of claim 1, further comprising:

forming a third hard mask on the first hard mask and a fourth hard mask on the second hard mask.

5. The method of claim 4, wherein a width of the first hard mask is equal to a width of the third hard mask.

6. The method of claim 1, further comprising:

forming a third CESL adjacent to one side of the third gate structure and a fourth CESL adjacent to another side of the third gate structure before performing the RMG process; and

forming a third hard mask on the third gate structure and a fourth hard mask on the fourth gate structure.

7. The method of claim 6, wherein a width of the third hard mask is greater than a width of the third gate structure.

8. The method of claim 6, wherein a sidewall of the third hard mask is aligned with a sidewall of the third CESL.

9. The method of claim 6, further comprising forming a fifth hard mask on the third hard mask and a sixth hard mask on the fourth hard mask.

10. A semiconductor device, comprising:

a substrate comprising a core region, a low noise amplifier (LNA) region, an input/output (I/O) region, and a power amplifier (PA) region;

a first gate structure on the LNA region, a second gate structure on the PA region, a third gate structure on the core region, and a fourth gate structure on the I/O region;

an interlayer dielectric (ILD) layer on the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure; and

a first hard mask on the first gate structure, and a second hard mask on the second gate structure, wherein a width of the first hard mask is greater than a width of the first gate structure.

11. The semiconductor device of claim 10, further comprising:

a first contact etch stop layer (CESL) adjacent to one side of the first gate structure and a second CESL adjacent to another side of the first gate structure.

12. The semiconductor device of claim 11, wherein the width of the first hard mask is greater than a distance between the first CESL to the second CESL.

13. The semiconductor device of claim 10, further comprising:

a third hard mask on the first hard mask and a fourth hard mask on the second hard mask.

14. The semiconductor device of claim 13, wherein a width of the first hard mask is equal to a width of the third hard mask.

15. The semiconductor device of claim 10, further comprising:

a third CESL adjacent to one side of the third gate structure and a fourth CESL adjacent to another side of the third gate structure; and

a third hard mask on the third gate structure and a fourth hard mask on the fourth gate structure.

16. The semiconductor device of claim 15, wherein a width of the third hard mask is greater than a width of the third gate structure.

17. The semiconductor device of claim 15, wherein a sidewall of the third hard mask is aligned with a sidewall of the third CESL.

18. The semiconductor device of claim 15, further comprising a fifth hard mask on the third hard mask and a sixth hard mask on the fourth hard mask.