The application relates to a horizontal filter for a luminance signal and a chrominance signal for the formation of a reduced image.

It is known to carry out horizontal filtering by analogue filters using a corresponding sampling frequency. As a result of this filtering, a correct reduction ratio is obtained. Then, using a multiplexer and an analogue/digital converter, the video components are converted into a digital data stream. A very high-speed multiplexer with a high sampling rate is required for this purpose.

The aim of the invention is to reduce the storage capacity in respect of a complete video image.

Thus aim is fulfilled by the measures described in Claim 1. Advantageous further developments of the invention are described in the sub-claims.

In order to display a video signal of a first receiving frequency, referred to in the following as main image, simultaneously to a video signal of a second receiving frequency on an image reproducing device, it is proposed that the video signal of the second receiving frequency, referred to in the following as reduced image, be reduced in its two-dimensional dimensions.

For this purpose only two field stores or one frame store are required for each video image comprising main image and reduced image. In order to reduce the size of the video signal of the second receiving frequency and to display it in the form of a reduced image in a main image, this is subsampled.

With the subsampling, a vertical and a horizontal reduction are carried out. Then the signal values are stored. As a result of the reduction carried out prior to the storage, storage space is saved. In accordance with the invention, a horizontal reduction of the reduced image is effected as follows. The store is used both for the luminance

signal components and for the chrominance signal components. Since the human eye is more sensitive to luminance signal components than to chrominance signal components, it is proposed that a sampling frequency ratio for luminance to chrominance of, for example, 3:1 be selected. For example, the luminance could be sampled at 10.125 MHz and the chrominance at 3.375 MHz. In this case the clock frequency amounts to 13.5 MHz of the combined video signal comprising luminance and chrominance.

For the processing of the video signals it is proposed that only one processing path be provided. For this purpose it is necessary to switch over the sampling frequencies for the luminance and the chrominance. The switch-over takes place in that both luminance and chrominance are sampled in a first circuit with a clock frequency of, for example, 6.75 MHz and in a following filter the luminance is further processed with a sampling frequency of, for example, 2.53 MHz and the chrominance with a sampling frequency of, for example, 0.84 MHz. In accordance with the invention, for this purpose the luminance is sampled during a first field and the chrominance during a following second field.

In the following an exemplary embodiment will be explained making reference to the drawing wherein:

Figure 1 illustrates multiplexers according to the invention with an analogue-digital converter;

Figure 2 is a time diagram of the multiplexer signals;

Figure 3 illustrates a digital filter for a separate luminance and chrominance signal;

Figure 4 illustrates a digital filter for the luminance;

Figure 5 is a time diagram of this digital filter;

Figure 6 illustrates a digital filter for the chrominance and

Figure 7 is a time diagram for these digital filters.

Figure 1 shows the multiplexer arrangement according to the invention with an analogue/digital converter 3. The chrominance components U and V of the input signal of the second receiving frequency are fed to a respective input of a multiplexer 1 which switches over the inputs with the frequency FH/8, which corresponds to one eighth of the line frequency. The output of the multiplexer 1 is connected to one input of a multiplexer 2, the second input of which is supplied with the luminance signal Y of the second receiving frequency. This multiplexer 2 is switched over with FF/2, where FF/2 is the field frequency. The output of the multiplexer 2 is connected to an input of the analogue/digital converter 3 with a sampling rate of 6.75 MHz.

Figure 2 illustrates the associated diagram of the multiplexer signals.

This input circuit according to Figure 1 produces a data stream of the following appearance:

```
1st Field                              2nd Field
           |  ----->                   |  ----->
line n     |  YYYYYYYYYYYYYYYY..       |  UUUUUUUUUUUUUUUU..
line n+1   |  YYYYYYYYYYYYYYYY..       |  UUUUUUUUUUUUUUUU..
           |  YYYYYYYYYYYYYYYY..       |  UUUUUUUUUUUUUUUU..
           |  YYYYYYYYYYYYYYYY..       |  UUUUUUUUUUUUUUUU..
           V  YYYYYYYYYYYYYYYY..       V  VVVVVVVVVVVVVVVV..
              YYYYYYYYYYYYYYYY..          VVVVVVVVVVVVVVVV..
              YYYYYYYYYYYYYYYY..          VVVVVVVVVVVVVVVV..
              YYYYYYYYYYYYYYYY..          VVVVVVVVVVVVVVVV..
              ................            ................
```

In the first field only the luminance components Y and in the second field in alternation every four lines the chrominance components U, V are fed to the analogue/digital converter 3. In order, for example, to achieve a bit rate of

3.375 Ms/s for the reduced image, with a reproduction ratio between luminance Y and chrominance C of 3:1, on average a bit rate of 2.53 Ms/s is set for the luminance Y and a bit rate of 0.84 Ms/s is set for the chrominance C. The reduction is carried out in a horizontal filter. The signals Y and C are stored as follows in a field store or frame store:

```
Column
          |  ----->
  line    |  YYYUYYYUYYYUYYYUYYYUYYYUYYYUYYYUYYYU
          |  YYYVYYYVYYYVYYYVYYYVYYYVYYYVYYYVYYYV
          |  YYYUYYYUYYYUYYYUYYYUYYYUYYYUYYYUYYYU
          |  YYYVYYYVYYYVYYYVYYYVYYYVYYYVYYYVYYYV
          V  YYYUYYYUYYYUYYYUYYYUYYYUYYYUYYYUYYYU
             YYYVYYYVYYYVYYYVYYYVYYYVYYYVYYYVYYYV
```

From the incoming data stream only one of the components Y or C is renewed in respect of each field.

```
1st Field                          2nd Field
line        YYY.YYY.YYY.YYY.       line   ...U...U...U...U
            YYY.YYY.YYY.YYY.              ...V...V...V...V
            YYY.YYY.YYY.YYY.              ...U...U...U...U
            YYY.YYY.YYY.YYY.              ...V...V...V...V
            YYY.YYY.YYY.YYY.              ...U...U...U...U
            ................              ................
            YYY.YYY.YYY.YYY.              ...U...U...U...U
            YYY.YYY.YYY.YYY.              ...V...V...V...V
```

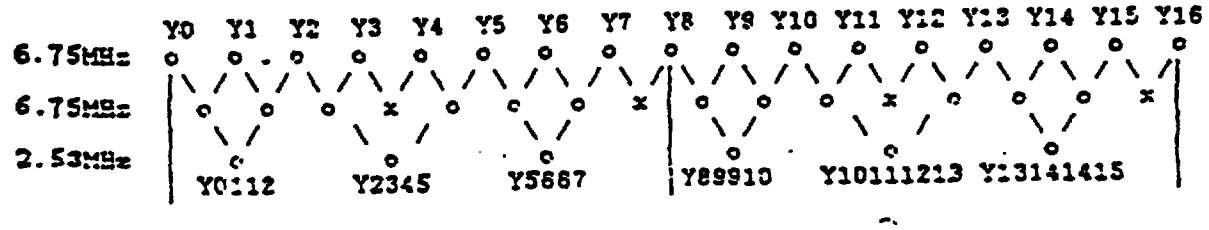
The write frequency of the store amounts to 3.375 MHz, but a few sample values of the luminance and the chrominance of a field are suppressed in dependence upon the components C, Y, the current fields and the store organisation.

To carry out the reduction, in accordance with the invention a digital filter according to Figure 3 is used. The output signal of the input circuit (Figure 1) is present at the input IN of the digital filter. This output signal is fed on the one hand to the input of a D-flip-flop 4 and on the other hand to the input of a 8x8 bit-adder 5. The D-flip-flop 4 is clocked with a clock frequency of 6.75 MHz. The outputs of the 8x8 bit-adder 5 lead to a 1:2 multiplexer 6, one output of which leads to a D-flip-flop chain 7 to 10 which is likewise clocked with 6.75 MHz. The other output of the 1:2 multiplexer 6 leads to a D- flip-flop 11 which is clocked with the clock frequency CK1. Both the output of the D- flip-flop 11 and the first output of the 1:2 multiplexer 6 lead to inputs of a 2:1 multiplexer 13 which is switched over with C, Y, where C, Y corresponds to the field frequency FF/2. One output of the D- flip-flop chain 7 to 10 and one output of the D- flip-flop 12 lead to a 2:1 multiplexer 14 which is likewise switched over with C, Y. Both outputs of the 2:1 multiplexers 13, 14 lead to a 8x8 bit-adder 15, the output of which leads to a divider 16. The output of the divider 16 leads on the one hand via a D- flip-flop 17 clocked with 6.75 MHz and also directly to an input of a 2:1 multiplexer 18. The output of the 2:1 multiplexer 18 leads via a D-flip-flop 19 clocked with CK2 and via a D- flip-flop 20 clocked with 3.375 MHz to the output OUT of the digital filter.

The digital filtering of the luminance is carried out as follows: For in each case one field of the frame of the incoming video signal, the filter processes the luminance signal Y in order to obtain a reduction for the image which is to be reduced. By means of suitable clock rates the filter is constructed in such manner that some parts are not used for the luminance filtering. Those parts which are used are represented in Figure 4 as filter for the luminance. As

can be seen from Figure 4, by means of the clock rate Y, corresponding to FF/2 for the luminance signal, the D-flip-flops 7 to 10 are not used for the luminance processing by the activation of the input of the multiplexer 14 which is connected to the output of the D-flip-flop 12. The multiplexers 6, 13 and 14 are clocked by the luminance signal Y in accordance with FF/2.

The mode of operation of the filter circuit according to Figure 4 is shown in the following plan. The input data stream, which emanates from the input multiplexer circuit (Figure 1), has a data rate of 6.75 Ms/s.



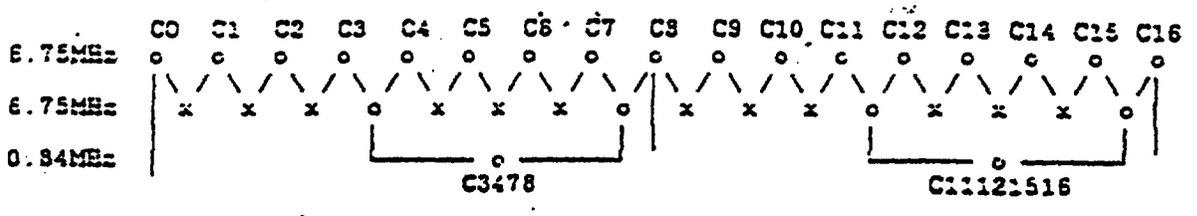
This plan represents the filter rule in accordance with which, from the three luminance values Y^0, $2*Y^1$, Y^2, by mean value formation a luminance value Y^{0112} of $Y^{0112} = (Y^0+2*Y^1+Y^2)/4$ is produced.

The same applies to the following four luminance values $Y^{2,3,4,5,}$ and so on.

Figure 5 is a time diagram of this digital filter for the luminance image components Y. Figure 5a illustrates the 6.75 MHz clock. Figure 5b illustrates the data items which occur at the output of the comb filter, comprising D-flip-flop 4 and 8x8 bit-adder 5. Here the respective luminance values Y^0 and Y^1 are combined to form a luminance value Y^{01}. Corresponding applies to the following luminance values. Figure 5c illustrates the clock signal CK1 which controls the D-flip-flop 11. In the case of

this clock signal CK1, after three respective luminance values Y^{01}, Y^{12}, Y^{23} the fourth luminance value Y^{34} is suppressed. Figure 5d illustrates the luminance values Y^{01}, Y^{12}, Y^{23}, Y^{45} ... at the point A, as occur at the output of the D-flip-flop 11. As can be seen from the time diagram (Figure 5d), the luminance values Y^{01} and Y^{12} are reproduced with a delay, and the luminance value Y^{23} is maintained for double the length of time as the luminance values Y^{01}, Y^{12}. Figure 5e illustrates the clock signal MUX with a clock frequency of 6.75/8 MHz. Figure 5d illustrates the clock frequency CK2 which for the luminance filtering is equal to the 6.75 MHz clock frequency of Figure 5a. Figure 5g shows the half clock frequency of CK2 which thus amounts to 3.375 MHz. Figure 5h shows the data output signal of the filter. As can be seen from Figure 5h, the luminance values Y^{0112}, Y^{2345}, Y^{5667} occur in serial fashion at the output, no luminance values being provided for the following clock time of 3.375 MHz as this space is reserved for the chrominance signal components C.

For the chrominance filtering according to Figure 3, the structure shown in Figure 6 is operative. The D-flip-flops 11 and 12 are not required for the filter operation. The second field of the incoming video signal is reserved for the chrominance filtering. The manner in which the chrominance values C are processed in the filter structure is schematically illustrated in the following. The data stream supplied by the input circuit again amounts to 6.75 Ms/s in the case of the chrominance. In accordance with the following filter rule, the chrominance values C^3, C^4 and C^7, C^8 are combined to form a chrominance value C^{3478}. The chrominance values $C^{1,2,5,6,}$ are suppressed.



In the time diagram of the filter for the chrominance signal components (Figure 7) the clock rates CK1 and MUX are not used. In this case the clock rate CK1 is set at logic "1". Only every eighth H-pulse of the clock rate according to Figure 7a is available for the clock rate CK2 of Figure 7f.

The filter (Figure 3) directly produces a data stream which can be written into the image store with the correct bit rate and the correct position of the individual chrominance and luminance components without additional signals. The data items are also arranged in the correct format. The reduction rate of the filter amounts to 1:4 in the horizontal direction. The vertical reduction can be effected, for example, by a vertical interpolar filter over for example four video lines. Only a small number of filter elements are employed in the filter circuit according to the invention. The number of different clock rates is small. The time bases required for the filter are produced on the one hand from the horizontal synchronizing pulse of each line and also by a 6.75 MHz clock pulse. All the other signals are produced internally.

Claims

1. A method of reducing images by subsampling and mean value formation of luminance image element values (Y) and chrominance image element values (U, V) in lines of these images, characterised in that three luminance image element values (Y0112, Y2345, Y5667) for a reduced image are calculated from in each case eight consecutive luminance image element values (Y0-Y7) by means of three mean value formations (5, 15, 16), and that a corresponding chrominance image element value (C3478) for the reduced image is calculated from in each case four (C3, C4, C7, C8) of eight consecutive chrominance image element values (C1-C8) of a chrominance component (U; V) by means of one mean value formation (5, 15, 16), where only image element values of one of the chrominance components are used on alternate lines.

2. A method as claimed in Claim 1, characterised in that prior to the mean value formations, the chrominance image element values are multiplexed with one eighth of the line frequency (FH/8) and the luminance- and chrominance components are multiplexed with the field frequency (FF/2) to form a common data stream.

3. A method as claimed in Claim 2, characterised in that the luminance- and chrominance image element values for the reduced image are stored in storage means which contain luminance- and chrominance image element values for an unreduced image.

* C L M S *