LOAD/LOAD DETECTION AND REORDER METHOD

ABSTRACT

The present invention is directed towards a means to detect and reorder out of order instructions that may violate data coherency. The invention comprises a mis-queue table (600) for holding entries (170,180) of instruction data, each entry (170,180) corresponding to an instruction in a computer microprocessor (10). The instruction data in each entry (170,180) comprises :i) instruction address information (540,550); ii) instruction ordering information (570); iii) instruction data modification information (530);
and iv) out of order information (520). The invention also comprises an out of order comparator for comparing an address of a completed instruction to any address information entries (540,550) in the miss queue (600). The invention also comprises a modification comparator for comparing addresses from data altering events to those addresses (540,550) in the entries (170,180) in the mis-queue table (600).

Fig.3