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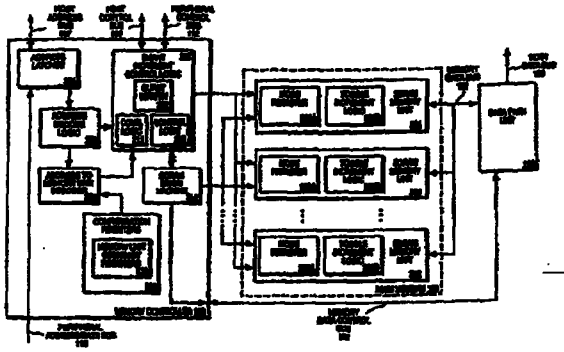
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(54) Title: A METHOD AND APPARATUS FOR CONTROLLING LINEAR AND TOGGLE MODE BURST ACCESS SEQUENCES USING TOGGLE MODE INCREMENT LOGIC



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(57) Abstract

Memory access control logic (108) for controlling sequential and toggle mode burst accesses to a memory (109) in a computer system using toggle mode automatic increment logic (201B). The memory access control logic (108) of the invention controls the sequence in which locations of a memory are accessed during a memory burst access operation wherein the burst access sequence is determined by an order in which a burst access starting address is incremented. Toggle increment logic (201B) for incrementing a starting address in a toggle sequence is included in the computer system in which the memory access control logic of the invention is used. An input bus (106) receives a burst access request and a burst access starting address indicating a first memory location to be accessed in response to the burst access request from a device in the computer system. Additional logic (117) determines whether the device requires a linear increment sequence or a toggle increment sequence for the burst access. Control logic (213) controls the toggle increment logic (201B) to increment the starting address in a linear sequence in response to determining that the device requires a linear increment sequence.

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