ABSTRACT

POWER LDMOS TRANSISTOR

A LDMOS transistor comprises a trench formed through the epitaxial layer at least to the top surface of the substrate, the trench having a bottom surface and a sidewall contacting the source region and the portion of the channel region extending under the source region. A first insulating layer is formed over the upper surface and sidewall surfaces of the conductive gate. A continuous layer of conductive material forming a source contact and a gate shield electrode is formed along the bottom surface and the sidewall of the trench and over the first insulating layer to cover the top and sidewall surfaces of the conductive gate. A second insulating layer is formed over an active area of the transistor, including over the continuous layer of conductive material and filling the trench. A drain electrode can extend over the second insulating layer to substantially cover the active area.

A laterally diffused metal-oxide-semiconductor (LDMOS) transistor device is also provided including a doped substrate having an epitaxial layer thereover having source and drain implant regions and body and lightly doped drain regions formed therein. The channel region and lightly doped drain regions are doped to a depth to abut the top surface of the substrate. In alternative embodiments, a buffer region of the second conductivity type and having dopant concentration greater than or equal to about the channel region is formed over the top surface of the substrate between the top surface of the substrate and the channel region and lightly doped drain region, wherein the channel region and lightly doped drain regions are doped to a depth to abut the buffer region.

[Figure 4]