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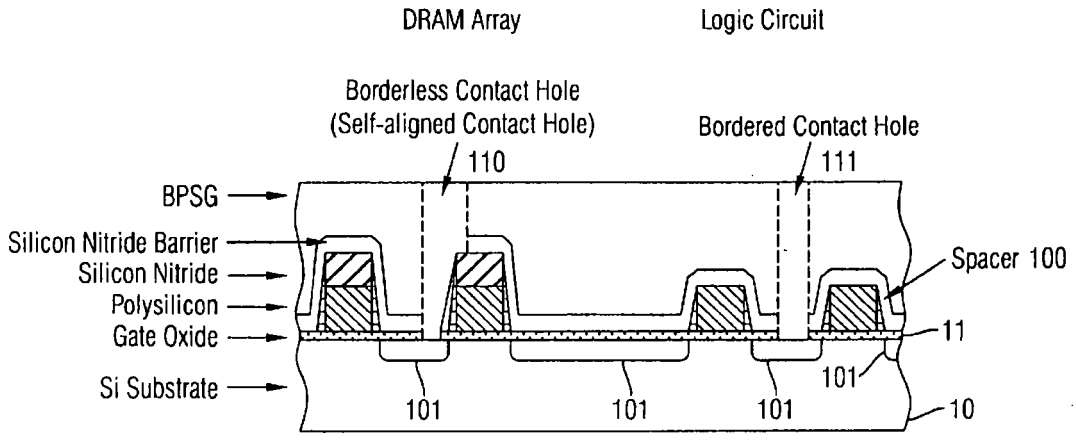
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(54) Title: DUAL LAYER HARD MASK FOR EDRAM GATE ETCH PROCESS



(57) Abstract: A method of fabricating an integrated circuit chip having a first region of a first layout rule and a second region of a second layout rule. The method includes using a first material to establish a first hard mask pattern in only the first region and using a second material to establish a second hard mask pattern on top of the first hard mask pattern. The second material is additionally used to establish a third hard mask pattern in the second region.

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