

# SPECIFICATION Frequency Sensing Circuit

The invention relates to a frequency sensing circuit, and particularly to a digital frequency sensing circuit that utilizes a relatively simple digital arrangement of known circuits.

Digital frequency sensing circuits or filters are being used more and more because of their relatively small size, high temperature stability, and similar qualities under mass production conditions. These characteristics are particularly needed and desirable where relatively low frequencies, for example audio frequencies, must be sensed or filtered. For the audio frequencies, the analog circuits require relatively large components, namely inductors and capacitors. Furthermore, those relatively large analog components are sensitive to temperature change, and typically require that their manufacturing tolerances be fairly large, unless they are individually tested and adjusted. Such testing and adjusting is expensive.

The problem addressed is to provide a frequency sensitive circuit which is compact and whose selectivity may be conveniently adjusted. The problem is solved by the use of sampling and digitizing techniques which lend themselves to the use of integrated circuits and the organization of such circuits into a particularly favorable arrangement.

Briefly, the invention involves the amplitude sampling of an input signal at a frequency that is N times the frequency to be sensed, where N is any integer that is equal to or greater than two.

The amplitude samples are quantized or encoded into digital form or words having the desired resolution. These digital words are applied to one input of a digital adder, and digital feedback words are applied to a second input of the adder.

The adder output is applied to a delay circuit which delays the digital output by an integral multiple of one-half of the period of the frequency to be sensed. The delayed digital words are multiplied by a number whose magnitude is less than one and which determines the Q of the circuit. The delayed and multiplied output words are applied as feedback words to the second adder input. Output digital signals are derived from the circuit at the adder output or at the delay circuit output, and have a magnitude that is a maximum when the input signals are

explaining the operation of the circuit of Figure 1.

As an example of the application of this frequency sensing circuit, it is assumed that one or more audio tones or sine wave signals may be received, and that it is desirable to sense or detect a particular tone frequency  $F_0$ . These tones or signals are applied to an input terminal 10 which is connected to an amplifier and limiter 12. The amplifier and limiter 12 converts the analog form of the input signal into substantially square or rectangular wave signals of the same frequency. These amplified and limited signals are applied to an amplitude sampler 14 which provides amplitude samples of the amplified and limited signals. The time duration of and interval between these samples is under the control of a clock generator 16 whose frequency  $F_c$  is set by a control signal applied to a terminal 18. The clock generator 16 produces clock signals or control pulses at the frequency  $F_c$  or rate that is N times the frequency  $F_0$  that is to be sensed. N may be any integer that is equal to or greater than two. For example, if the frequency  $F_0$  to be sensed is 300 Hertz, then the clock generator would produce control pulses at a frequency  $F_c$  or rate of at least 600 Hertz. For good operation, N is preferably at least 4, so that for a frequency  $F_0$  of 300 Hertz, the control pulses would have a frequency  $F_c$  of 1200 Hertz. Thus, the sampler 14 would provide amplitude samples at a 1200 Hertz rate. The clock generator 16 is connected to other parts of the circuit to synchronize and control the digital operations.

These amplitude samples are applied to a digital encoder 20 which converts the amplitude of each of the samples to a digitally encoded word EW. Because of the amplifier and limiter 12, the amplitude samples have only two levels, so that only one digital significant number is needed. If an amplifier and limiter are not used, the encoder words EW may include more significant digits (for example 1, 2, 4, 8, 16, and so on in binary form), depending upon the resolution desired in the remainder of the circuit. For example, if a digital word has 16 binary digits, then  $2^{16}$  or 65,536 different values or numbers could be represented in binary form. The bits forming each such word may be in series or in parallel. One of the bits forming each word represents the sign of the number. For the purpose of this explanation, it is assumed that the bits are in parallel, so that no high speed serial clock signals are needed for the digital encoder and certain other parts of the invention. The digital words from the encoder 20 are applied to one input of a digital adder 22. The output of the digital adder 22 is applied to a feedback circuit consisting only of a delay circuit 24 and a multiplier circuit 26 connected in series in either order between the adder circuit 22 output and the adder circuit 22 second input. The delay circuit 24 delays the added words AW by an integral multiple of one-half the time period  $T_0$  of the frequency  $F_0$  to be sensed. As known,  $T_0$  equals

$$\frac{1}{N}$$

times the sampling frequency.

The invention may be better understood from the following description given in connection with the accompanying drawing, in which:

Figure 1 shows a schematic block diagram of a preferred embodiment of a frequency sensing circuit in accordance with the invention; and

Figures 2, 3, and 4 show waveforms for

$$\frac{1}{F_0}$$

Or expressed mathematically, the delay is equal to

$$\frac{MT_0}{2}$$

where M is any integer. If, as is preferred, the delay circuit 24 utilizes some type of digital shift register, it is provided with clock signals from the clock generator 16. If a digital shift register is used for providing delay, the delay provided is

$$\frac{MN}{2}$$

digital words, where M and N are defined above. However, if the delay circuit is of some other type, clock signals may not be needed. The output words DW from the delay circuit 24 are fed back through a digital multiplier 26 to a second input of the binary adder 22. The multiplier 26 multiplies the delayed digital words DW by some number K (less than one but greater than zero) the value depending upon the desired circuit Q. The multiplier number K determines the Q of the sensing circuit by the relation

$$\arctan \frac{1-K}{1+K}$$

so that the Q varies in the same direction as K is varied. In the feedback circuit, the sign of the words which are applied to the second input of the adder circuit 22 is determined by the integer M used in the delay circuit 24. If M is an odd integer, the sign of the fed back words must be minus; if M is an even integer, the sign of the fed back words must be plus. Or expressed in another way, the phase of each delayed and multiplied word applied to the adder circuit 22 must be the same as the phase of the encoder word applied to the adder circuit 22 at the same time. The adder circuit 22 adds the encoder words EW and the feedback words MW from the multiplier 26 and supplies the sum of these words as adder words AW. The adder circuit 22, the delay circuit 24, and the multiplier 26 should be able to handle the number of significant digits needed for desired circuit accuracy. Output signals from this frequency sensing circuit may be derived from the output of the adder circuit 22 or may be derived from the output of the delay circuit 24.

An example of the operation of the circuit of Figure 1 is explained in connection with Figure 2 which shows waveforms and information plotted along a common time axis. In this particular

example, it is assumed that the clock generator 16 produces clock signals or pulses at a frequency  $F_c$  that is four times the frequency  $F_0$  to be sensed. Hence N is 4. The signal of frequency  $F_0$  to be sensed is shown in Figure 2(A) after being amplified and limited, and the clock frequency signal  $F_c$  is shown in Figure 2(B). Thus, for each cycle of the sensed frequency signal  $F_0$ , four amplitude samples would be taken. It is assumed that each sample is taken on the decreasing edge of each clock signal, and this is indicated by the designation S followed by a sample number at each appropriate point in Figure 2(A). For a clock frequency  $F_c$  that has an N of 4 times the frequency  $F_0$  to be sensed, generally two samples will be taken in a positive half cycle and two samples will be taken in a negative half cycle of the frequency  $F_0$ . These samples are shown in Figure 2(C). Because of the amplification and limiting, these amplitude samples would have only two values, which can be assumed to be +1.00 or -1.00. These amplitudes are converted by the encoder 20 to digital words EW indicated in Figure 2(D). The number and sign of the samples and words are also indicated. In Figure 2(D), it will be noted that four encoder words EW are provided for each period  $T_0$  of the frequency  $F_0$  to be sensed. In other words, N determines the number of encoder words EW produced in a period  $T_0$ . These words EW are applied to one input of the adder circuit 22. The adder output words AW are shown in Figure 2(G). These words AW are applied to the delay circuit 24 which is assumed to have M equal one, so that the delay is

$$\frac{T_0}{2}$$

The delay output words DW are shown in Figure 2(E), and it will be noted that they are later in time by

$$\frac{T_0}{2}$$

For example, the first sample S1 is taken at the time T1, encoded into word EW1 at the time T1, and also added at the time T1. However, the encoded word EW1 does not appear as delay word DW1 until the time T3, since

$$T1 + \frac{T_0}{2}$$

equals T3. The same delay (of

$$\frac{T_0}{2}$$

or the time duration of two words) is shown for each word number when figures 2(D) and 2(E) are

compared. The delay words DW are applied to the multiplier circuit 26 which produces multiplier words MW shown in Figure 2(F). It is assumed that the multiplier circuit 26 provides the necessary sign reversal for M equals 1. Thus, the delay word DW1+ becomes multiplier word MW1-; the delay word DW3- becomes multiplier word MW3+. The multiplier words MW and the encoder words EW are added in real time as shown by the adder words AW in Figure 2(G). It will be noticed that the signs or phases of the added words are always the same because the frequency  $F_0$  being sensed is correct for the clock frequency  $F_c$  of the generator 16. Thus, the words EW and MW applied to the adder circuit 22 have an additive or in-phase relation which causes the adder 22 to produce an output that starts at a relatively low value and approaches maximum positive and negative values as more and more words are added. The maximum values are determined by the relation

$$\frac{1}{1-K}$$

where K is the multiplication number of the multiplier 26. As the multiplication number K approaches unity, the maximum value increase. This is illustrated in Figure 3 which is a plot (against time) of the numerical values of the output of the adder (22) where the incoming frequency equals the desired frequency to be sensed, and where the multiplier K is equal to 0.95. The maximum value or output approaches

$$\frac{1}{1-.95}$$

or 20. Since only 20 cycles are shown, the output has only reached about 17. For all practical purposes, the output would reach 20 by 50 cycles. So if the circuit threshold is set at about 15, an accurate indication of the desired frequency will be obtained. For a multiplier of 0.95, the circuit Q equals

$$\frac{90^\circ}{\text{arc tan } \frac{.05}{1.95}}$$

or approximately 61. The waveform of Figure 3 is the wave that would be observed at the output of a digital-to-analog converter driven by the output of adder-circuit 22. However, if the frequency of the sensed signals is not the desired frequency as determined by the control signal applied to the clock generator 16, the output from the adder circuit 22 will not approach the maximum values, but will fluctuate up and down in a manner dependent upon the relation of the input signal frequency and the clock generator frequency.

Hence, the output of the adder circuit 22 will never approach the maximum value that would indicate or sense the desired frequency. This is illustrated in Figure 4 where the incoming frequency differs from the frequency to be sensed by about 5%, and where the multiplier K is 0.95. The output varies randomly, and occasionally just reaches a magnitude of 10, so that a threshold of 15 (as mentioned above) would prevent any indication from being given. The output of the adder 22 and for this sensing circuit may be applied to any type of threshold circuit, or may be converted to an analog signal and then applied to a threshold circuit. Either arrangement would provide the maximum indication for the desired frequency being sensed.

It will thus be seen that this new and improved digital frequency sensing circuit that is relatively simple, and that uses known components or circuit elements in a unique and improved arrangement. With previous digital frequency sensing circuits that required two or more feedback arrangements and a complicated frequency sensing circuit, it was relatively difficult to control or program the clock generator and the fractional multipliers which were needed. While only one example of the new frequency sensing circuit has been described persons skilled in the art will appreciate that it can be used as a frequency sensing or bandpass filter circuit for almost any frequency. The digital words may be formed of series bits or parallel bits, depending upon circuit requirements and preferences. Various digital codes may be used. The number of significant digits forming each word may be varied, depending upon the accuracy desired. The clock generator 16 may be operated at any integral multiple of two or more times the frequency  $F_0$  to be sensed; the delay circuit 24 may be operated at any integral multiple of one-half the period  $T_0$  of the frequency to be sensed; and the multiplier 26 may utilize any fractional or decimal multiplication depending upon the circuit Q and maximum output desired or needed. Therefore, while the invention has been described with reference to the particular embodiment shown, it is to be understood that modifications may be made without departing from the scope of the invention, as defined in the appended claims.

#### Claims

1. An improved frequency sensing circuit having means for sampling an input signal including means for producing clocking signals at a rate of N times a frequency  $F_0$  to be sensed, where N is any integer greater than one; analog to digital converting means responsive to said input signal and to said clock signals for producing a sampled digital output; adding means consisting of first and second inputs and an output; means connecting said first input of said adding means to said analog to digital converting means; delay means having an input connected to said adding means output and having an output, said delay means being arranged to delay signals applied



compared. The delay words DW are applied to the multiplier circuit 26 which produces multiplier words MW shown in Figure 2(F). It is assumed that the multiplier circuit 26 provides the necessary sign reversal for M equals 1. Thus, the delay word DW1+ becomes multiplier word MW1-; the delay word DW3- becomes multiplier word MW3+. The multiplier words MW and the encoder words EW are added in real time as shown by the adder words AW in Figure 2(G). It will be noticed that the signs or phases of the added words are always the same because the frequency  $F_0$  being sensed is correct for the clock frequency  $F_c$  of the generator 16. Thus, the words EW and MW applied to the adder circuit 22 have an additive or in-phase relation which causes the adder 22 to produce an output that starts at a relatively low value and approaches maximum positive and negative values as more and more words are added. The maximum values are determined by the relation

$$\frac{1}{1-K}$$

where K is the multiplication number of the multiplier 26. As the multiplication number K approaches unity, the maximum value increase. This is illustrated in Figure 3 which is a plot (against time) of the numerical values of the output of the adder (22) where the incoming frequency equals the desired frequency to be sensed, and where the multiplier K is equal to 0.95. The maximum value or output approaches

$$\frac{1}{1-0.95}$$

or 20. Since only 20 cycles are shown, the output has only reached about 17. For all practical purposes, the output would reach 20 by 50 cycles. So if the circuit threshold is set at about 15, an accurate indication of the desired frequency will be obtained. For a multiplier of 0.95, the circuit Q equals

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or approximately 61. The waveform of Figure 3 is the wave that would be observed at the output of a digital-to-analog converter driven by the output of adder-circuit 22. However, if the frequency of the sensed signals is not the desired frequency as determined by the control signal applied to the clock generator 16, the output from the adder circuit 22 will not approach the maximum values, but will fluctuate up and down in a manner dependent upon the relation of the input signal frequency and the clock generator frequency.

Hence, the output of the adder circuit 22 will never approach the maximum value that would indicate or sense the desired frequency. This is illustrated in Figure 4 where the incoming frequency differs from the frequency to be sensed by about 5%, and where the multiplier K is 0.95. The output varies randomly, and occasionally just reaches a magnitude of 10, so that a threshold of 15 (as mentioned above) would prevent any indication from being given. The output of the adder 22 and for this sensing circuit may be applied to any type of threshold circuit, or may be converted to an analog signal and then applied to a threshold circuit. Either arrangement would provide the maximum indication for the desired frequency being sensed.

It will thus be seen that this new and improved digital frequency sensing circuit that is relatively simple, and that uses known components or circuit elements in a unique and improved arrangement. With previous digital frequency sensing circuits that required two or more feedback arrangements and a complicated frequency sensing circuit, it was relatively difficult to control or program the clock generator and the fractional multipliers which were needed. While only one example of the new frequency sensing circuit has been described persons skilled in the art will appreciate that it can be used as a frequency sensing or bandpass filter circuit for almost any frequency. The digital words may be formed of series bits or parallel bits, depending upon circuit requirements and preferences. Various digital codes may be used. The number of significant digits forming each word may be varied, depending upon the accuracy desired. The clock generator 16 may be operated at any integral multiple of two or more times the frequency  $F_0$  to be sensed; the delay circuit 24 may be operated at any integral multiple of one-half the period  $T_0$  of the frequency to be sensed; and the multiplier 26 may utilize any fractional or decimal multiplication depending upon the circuit Q and maximum output desired or needed. Therefore, while the invention has been described with reference to the particular embodiment shown, it is to be understood that modifications may be made without departing from the scope of the invention, as defined in the appended claims.

#### Claims

1. An improved frequency sensing circuit having means for sampling an input signal including means for producing clocking signals at a rate of N times a frequency  $F_0$  to be sensed, where N is any integer greater than one; analog digital converting means responsive to said input signal and to said clock signals for producing a sampled digital output; adding means consisting of first and second inputs and an output; means connecting said first input of said adding means to said analog to digital converting means; and means having an input connected to said adding means output and having an output, said output means being arranged to delay signals applied



thereto by an amount that is an integral multiple of one-half the time period of the frequency to be sensed; multiplier means coupled to said means for producing clocking signals so as to be clocked thereby and having an input connected to said delay means output and having an output connected to said second input of said adding means; and means connected to said frequency sensing circuit for deriving an output signal therefrom having a magnitude indicative of the frequency sensed.

2. A frequency sensing circuit according to Claim 1 in which N is four.

3. A frequency sensing circuit according to Claim 1 or Claim 2 in which the delay means comprises a digital circuit connected to said means for producing clock signals.

4. The frequency sensing circuit of Claim 1 or Claim 2 in which the delay means provides signals to said second input of said adding means that are in phase with signals applied to said first input of said adding means.

5. A frequency sensing circuit according to Claim 3 in which the delay means provides signals to said second input of said adding means that are in phase with signals applied to said first input of said adding means.

6. A frequency sensing circuit according to Claim 1 for sensing the presence of a frequency  $F_0$  in an applied signal, characterized by means connected to receive the input signal for sampling said applied signal at a rate of  $NF_0$ , where N is any integer of two or more; a feedback circuit connected between said output and second input of said adding means, said feedback circuit consisting of delay means and multiplier means connected in series, said delay means producing a time delay of an integral multiple times the period

$$\frac{1}{2F_0}$$

and said multiplier means multiplying signals in said feedback circuit by a number less than one and greater than zero; and means connected to said frequency sensing circuit for deriving an output signal therefrom having a magnitude indicative of the frequency sensed.

7. A frequency sensing circuit according to Claim 6 characterized in that N is at least four, said delay multiple is one, and said feedback circuit changes the sign of signals therein.

8. A frequency sensing circuit according to Claim 6 characterized in that N is at least four, and said delay multiple is two.

9. A frequency sensing circuit according to Claim 6 or Claim 7 or Claim 8 characterized in that said adding means and said feedback circuit comprise digital circuits.

10. A frequency sensing circuit according to Claim 6, or Claim 7 or Claim 8 characterized in that said feedback circuit provides signals to said second input of said adding means that are in phase with signals applied to said first input of said adding means.

11. A frequency sensing circuit according to Claim 9 characterized in that said feedback circuit provides signals to said second input of said adding means that are in phase with signals applied to said first input of said adding means.

12. A frequency sensing circuit according to Claim 1 characterized by sampling means having an input receiving said input signal, an output, and a control input connected to said means for producing clocking signals, said sampling means providing at said output an amplitude sample of said input signal in response to each clocking signal; means connecting said first input of said adding means to said sampling means output; feedback means connecting said adding means output to said adding means second input, said feedback means consisting of delay means for producing a delay of one-half the time period  $T_0$  of said desired frequency  $F_0$ ; multiplier means for multiplying signal magnitudes by a selected amount less than one and greater than zero; and means connecting said delay means and said multiplier means in series; and means connected to said frequency sensing circuit for deriving an output signal therefrom having a magnitude indicative of the frequency sensed.

13. A frequency sensing circuit according to Claim 12 characterized in that said feedback means further includes means for changing the sign of signals therein.

14. A frequency sensing circuit according to Claim 13 and characterized by a digital encoder connected between said sampling means output and said adding means first input.

15. A frequency sensing circuit according to Claim 14 characterized in that said adding means, said delay means, and said multiplier means comprises binary digital circuits.

16. A frequency sensing circuit according to Claim 12, or Claim 13, or Claim 14, or Claim 15 characterized in that said feedback means provides signals to said second input of said adding means that are in phase with signals applied to said first input of said adding means.

17. A frequency sensing circuit substantially as described herein with reference to the accompanying drawings.