

WHAT IS CLAIMED IS:

1. A semiconductor die comprising:

first pads;

5 switches electrically connected with the first pads, respectively;

a test signal generator configured to generate test signals and to transmit the test signals to the switches;

internal circuits configured to receive first signals through the first pads and the switches, to perform operations based on the first signals, and to output second signals through
10 the switches and the first pads based on a result of the operations; and

a switch controller configured to control the switches so that the first pads communicate with the test signal generator during a test operation and the first pads communicate with the internal circuits after a completion of the test operation,

wherein the first pads are disposed in line along a first direction, and intervals between
15 the first pads gradually increase or decrease in the first direction.

2. The semiconductor die of claim 1, wherein the test signals transmitted from the test signal generator to the switches are voltages of the same level or currents of the same amount.

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3. The semiconductor die of claim 1 or claim 2, further comprising:

a second pad electrically connected with the test signal generator,

wherein the test signal generator is configured to transmit the test signals depending on a test command received through the second pad.

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4. The semiconductor die of claim 1 or claim 2, further comprising:

a second pad configured to supply a power to the test signal generator and the switch controller in the test operation.

5 5. The semiconductor die of any one of claims 1 to 4, wherein the switch controller includes a laser fuse,

wherein, when the laser fuse is in a connected state, the switch controller controls the switches such that the test signal generator and the first pads communicate with each other; and

10 wherein, when the laser fuse is in a disconnected state, the switch controller controls the switches such that the internal circuits and the first pads communicate with each other.

6. The semiconductor die of any one of claims 1 to 4, wherein the switch controller includes an electrical fuse,

15 wherein, when the electrical fuse is in a first state, the switch controller controls the switches such that the test signal generator and the first pads communicate with each other; and

wherein, when the electrical fuse is in a second state, the switch controller controls the switches such that the internal circuits and the first pads communicate with each other.

7. The semiconductor die of claim 1 or claim 2, further comprising:

20 second pads directly connected with the internal circuits.

8. The semiconductor die of any one of claims 1 to 7, wherein an interval between at least two pads from among the first pads is smaller than a width of each of the at least two pads.

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9. The semiconductor die of any one of claims 1 to 8, wherein the internal circuits include memory cells electrically connected with string selection lines, word lines, ground selection lines, and bit lines, and

wherein at least some of the string selection lines, the word lines, the ground selection lines, and the bit lines are electrically connected with the first pads through the switches.

10. The semiconductor die of claim 1 or claim 2, further comprising:

second pads and third pads configured to communicate with an external device, and

wherein the internal circuits include:

10 a buffer block configured to receive a row address, a column address and a command from the external device through the second pads and to exchange read data or write data with the external device through the second pads;

a row decoder block electrically connected with string selection lines, word lines, ground selection lines, and configured to receive the row address from the buffer block and to adjust voltages of the string selection lines, the word lines, and the ground selection lines based on the row address;

a page buffer block electrically connected with bit lines, and configured to adjust voltages of the bit lines based on the write data stored therein in a write operation and to store the voltages of the bit lines therein as the read data in a read operation;

20 a data input and output block electrically connected between the page buffer block and the buffer block, and configured to receive the column address from the buffer block and to exchange the write data and the read data between the page buffer block and the buffer block based on the column address; and

a control logic block configured to receive a control signal from the external device through the third pads, to receive the command from the buffer block, and to control the write

operation and the read operation based on the command and the control signal.

11. A semiconductor die comprising:

first pads;

5 switches electrically connected with the first pads;

a test signal receiver configured to receive reception signals through the first pads and the switches;

internal circuits configured to receive first signals through the first pads and the switches, to perform operations based on the first signals, and to output second signals through the switches and the first pads based on a result of the operations; and

a switch controller configured to control the switches so that the first pads communicate with the test signal receiver during a test operation and that the first pads communicate with the internal circuits after a completion of the test operation,

15 wherein the first pads are disposed in line along a first direction, and intervals between the first pads gradually increase or decrease in the first direction.

12. The semiconductor die of claim 11, further comprising:

a second pad electrically connected with the test signal receiver,

20 wherein the reception signals vary depending on a test command received through the second pad.

13. The semiconductor die of claim 11, further comprising:

a second pad configured to be used for the test signal receiver to output a result of the test operation to an external device after the reception signals are received.

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14. A semiconductor wafer comprising:

first pads disposed in line along a first direction, wherein intervals between the first pads gradually increase or decrease in the first direction;

test signal devices electrically connected with the first pads, and configured to
5 transmit or receive test signals through the first pads; and

internal circuits, each of the internal circuits being one of a nonvolatile memory cell array and a peripheral device configured to access the nonvolatile memory cell array.

15. The semiconductor wafer of claim 14, further comprising:

10 second pads disposed in line along a second direction crossing the first direction,
wherein intervals between the second pads gradually increase or decrease in the second direction, and

wherein the second pads are electrically connected with the test signal devices to
transmit or receive the test signals.

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16. The semiconductor wafer of claim 14 or claim 15, further comprising:

switches configured to control so that the first pads communicate with the test signal
devices in a test operation and the first pads communicate with the internal circuits after a
completion of the test operation.

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17. The semiconductor wafer of any one of claims 14 to 16, wherein the
semiconductor wafer comprises a plurality of semiconductor dies configured to be divided into
separate semiconductor dies, and

wherein the first pads and the test signal devices are disposed on a cutting line disposed
25 between the semiconductor dies.

18. The semiconductor wafer of claim 14, further comprising:
second pads disposed in line along the first direction at regular intervals.