



ABSTRACT

DISPLAY LOCKED TIMING SIGNALS FOR VIDEO PROCESSING

A circuit (12) for receiving a video signal with a horizontal synchronizing component (on 11) at a horizontal scanning frequency generates an intermediate synchronizing signal (on 47) synchronized with the horizontal synchronizing component. A horizontal deflection circuit (40, 50) generates horizontal deflection current synchronized with the intermediate synchronizing signal (on 47). An oscillator (62) generates a display-locked clock signal (on 65) synchronously with a clock synchronizing signal (on 59) derived from the horizontal deflection current. A counter (64) divides the clock signal, producing decodable outputs. A decoding circuit generates display locked timing signals, at the frequency of the horizontal synchronizing component and at the frequency of the intermediate signal, from the outputs of the counter (64). Where the frequency of the intermediate signal (on 47) is a multiple of the frequency of the horizontal synchronizing component, for example by a factor of two, a circuit coupled to the counter (64) and the decoding circuit associates certain pulses of the display locked clock signal with commencement of video line intervals in the video signal.

FIG 2