

ABSTRACT

A memory device can include a memory block operatively connected to a common source line and a plurality of bit lines, wherein the memory block includes first and second sub-blocks each having a respective position in the memory block relative to the common source line and the plurality of bit lines. The memory device can be operated by receiving a command and an address from outside the memory device and performing a precharge operation on the memory block in response to the command, using a first precharge path through the memory block or a second precharge path through the memory block based on the respective position of the first or second sub-block that includes a word line that is configured to activate responsive to the address.

FIG. 1A