

SPECIFICATION

TITLE OF THE INVENTION:

**SEMICONDUCTOR INTEGRATED CIRCUITRY AND METHOD FOR
MANUFACTURING THE CIRCUITRY**

TECHNICAL FIELD

The present invention relates to a semiconductor integrated circuitry and a technology for manufacturing the semiconductor integrated circuitry, more particularly, the present invention relates to a technology effectively applicable for realizing higher integration and higher performance of a DRAM (Dynamic Random Access Memory) or an electrically reloadable nonvolatile memory, or for a highly integrated semiconductor circuitry provided with a logic circuit and a DRAM or an electrically reloadable nonvolatile memory.

BACKGROUND ART

There is a DRAM used as a semiconductor memory representing a large capacity memory. The memory capacity of this DRAM is increasing more and more, and under the circumstances, the memory cells occupied area is forced to be reduced to improve the degree of integration of the DRAM.

However, the storage capacity of an information storing capacity element (capacitor) in DRAM memory cells must be fixed to a certain value regardless of the generation when in taking a DRAM operation margin, software errors,

etc. into consideration. Generally, it is known that the storage capacity cannot be reduced proportionally.

This is why it is now under development of a capacitor structure that can secure a storage capacity necessary in a limited small occupation area. As such a capacitor structure, for example, there is adopted a three-dimensional capacitor such as a so-called stacked capacitor composed of two-layer electrodes composed of polysilicon, etc. and stacked via a capacity insulating film.

A stacked capacitor is generally composed of capacitor electrodes disposed in the upper layer of a memory cell selecting MISFET (Metal Insulator Semiconductor Field Effect Transistor). In this case, a small occupied area can secure a large storage capacity, as well as only a small storage capacity is needed.

As such a stacked capacitor structure, for example, there are a so-called capacitor over bit-line (hereafter, to be abbreviated as COB) structure in which a capacitor is disposed over the bit-line and a capacitor under bit-line (hereafter, to be abbreviated as CUB) structure in which a capacitor is disposed under the bit-line.

In a DRAM having such a COB/CUB structure, capacitor connecting holes must be formed so that a conductor film or a bit-line in each capacitor connecting hole is not short-circuited with a word-line. Thus, the interval

between adjacent word-lines must be widened to cope with connecting hole positioning failures. And, this hinders improvement of the degree of integration of elements, as well as reduction of chip sizes. In order to realize high integration, therefore, high technology of positioning and alignment, as well as process management are needed.

In order to solve the problems and meet the requirements, there is proposed a technology for forming capacitor connecting holes and bit-line connecting holes by etching in a self-matching manner with respect to the word-lines by covering the top and side surfaces of the word-lines by an insulating material different in type from an interlaminar insulating film such as a nitride film, etc.

In the case of such a technology, when capacitor connecting holes and bit-line connecting holes are formed by etching, it is possible to prevent the word-lines from being exposed from the connecting holes even when the connecting holes overlap the word-lines, since the nitride film around the word-lines functions as an etching stopper. Thus, the connecting holes can be formed properly.

The technology for forming capacitor connecting holes and bit-line connecting holes in a self-matching manner with respect to the word-lines is disclosed in the official report of Unexamined Published Japanese Patent Application No.9-55479.

Under the circumstances, the present inventor examined the technology for forming the capacitor connecting holes and bit-line connecting holes in a self-matching manner with respect to word-lines. The following technologies are not well-known, but examined by the present inventor. The outline of those technologies will be described below.

The DRAM described above is formed in a process flow shown below. At first, a conductor layer is formed on a semiconductor substrate via a gate insulating film. On the conductor film is deposited the first nitride film. Then, the first nitride film and the conductor film are patterned using the same mask to form gate electrodes of the memory cell selecting MISFET and gate electrodes of the peripheral circuit MISFET. At this time, the gate electrodes of plural memory cells disposed in the row direction of the memory cell array are formed unitarily and functions as a DRAM word line. Next, a low density semiconductor area is formed for the memory cell selecting MISFET and the peripheral circuit MISFET respectively in a self-matching manner with respect to the memory cell selecting MISFET and the peripheral circuit MISFET respectively. Then, the second nitride film is deposited on the semiconductor substrate and applied anisotropic etching to form nitride film side wall spacers on side walls of the gate electrodes of both the memory cell

selecting MISFET and the peripheral circuit MISFET. Then, a high density semiconductor area is formed for the peripheral circuit MISFET in a self-matching manner with respect to the side wall spacers. Thereafter, on the semiconductor substrate is deposited an interlaminar insulating film composed of an oxide film and bit-line and capacitor connecting holes are opened in the memory cell area in a self-matching manner with respect to word-lines. This process for opening the bit-line and capacitor connecting holes in this interlaminar insulating film is performed on conditions to increase the etching selection ratio of the nitride film composing side walls to the oxide film composing the interlaminar insulating film, so the bit-line and capacitor connecting holes can be formed without exposing the word-lines.

On the other hand, in order to improve the degree of integration of the DRAM memory cells, the interval between word-lines must be minimized. When the second nitride film is deposited on the word-lines disposed at minimized intervals up to a specified film thickness or over, every space between word-lines in the memory cell area is filled completely with the second nitride film, so that the surface of the semiconductor substrate is not exposed even after anisotropic etching is carried out for the nitride film to form side wall spacers. Otherwise, a problem that the

exposed area is very small and the contact resistance generated between the exposed area and each bit-line or capacitor electrode is increased significantly arises.

In addition, side wall spacers formed on side walls of the gate electrodes of both the memory cell selecting MISFET and the peripheral circuit MISFET decide the length of the low density semiconductor area of the peripheral circuit MISFET having an LDD structure. And, when this side wall spacer is reduced in width, a problem that the short channeling effect of the peripheral circuit MISFET becomes remarkable and the punched-through dielectric strength between source and drain is lowered will arise. This is why the second nitride film for forming side wall spacers must have a thickness over a specified value.

In other words, in order to secure a specified performance of a MISFET, the LDD structure must be optimized. When the DRAM memory cell selecting MISFET is divided finely to reduce the side wall spacer in width, the side wall spacer width must be over a specified value to prevent the high density semiconductor area of the peripheral circuit MISFET from being distributed over the low density semiconductor area. This means that the width of each side wall spacer has a lower limit.

On the other hand, when the memory array is divided finely, the interval between gate electrodes, that is, the

interval between adjacent memory cell selecting MISFETs is narrowed accordingly. Thus, every portion to be connected in a self-matching manner is also reduced in width. When such a connecting area is narrowed, the contact resistance in the area is also increased significantly. Thus, the side wall spacer must be minimized in width. Such a requirement conflicts with a requirement for optimizing the LDD structure. And in the worst case, when the LDD structure is optimized, adjacent side wall spacers are overlapped in the memory array area so that self-matching connections are disabled.

Under the circumstances, it is an object of the present invention to provide a semiconductor integrated circuitry technology for dividing DRAM memory cells finely so as to be more highly integrated and to make the operation faster in the semiconductor integrated circuitry provided with a DRAM.

It is another object of the present invention to provide a semiconductor integrated circuitry technology for dividing memory cells finely so as to be more highly integrated and make the operation faster in the semiconductor integrated circuitry provided with a DRAM and an electrically reloadable nonvolatile memory.

It is still another object of the present invention to provide a technology for realizing a high performance

semiconductor integrated circuitry having excellent refreshing characteristics of DRAM.

It is still another object of the present invention to provide a technology for realizing a semiconductor integrated circuitry that can prevent the element isolating area on the semiconductor substrate from over-etching when in opening of the connecting holes to improve the reliability of the semiconductor integrated circuitry.

It is still another object of the present invention to provide a technology for simplifying the manufacturing method of a semiconductor integrated circuitry provided with a DRAM and an electrically reloadable nonvolatile memory.

It is still another object of the present invention to provide a technology for realizing a semiconductor integrated circuitry, which can divide DRAM cells finely so as to be more highly integrated and improve the reliability of the peripheral circuit MISFET.

It is still another object of the present invention to provide a technology for forming connecting holes in a self-matching manner even in a highly integrated DRAM memory cell area and prevent the element isolating area at the bottom of each of the connecting holes from over-etching.

It is still another object of the present invention to provide a technology for improving the connecting hole

treatment margin when the connecting holes are formed in a self-matching manner and preventing the element isolating area at the bottom of each connecting hole from over-etching.

It is still another object of the present invention to provide a technology for suppressing the number of processes to be increased when the connecting holes are formed in a self-matching manner and the element isolating area at the bottom of each connecting hole is prevented from over-etching.

It is still another object of the present invention to provide a technology for integrating a semiconductor integrated circuitry more highly and improving the refreshing characteristics of the DRAM and the transistor characteristics of the memory cell area.

The above and other objects and novel features of the present invention will fully appear from the description of the specification and the accompanying drawings.

DISCLOSURE OF THE INVENTION

Of the inventions disclosed in this specification, the representative ones will be summarized as follows.

(1) The semiconductor integrated circuitry of the present invention comprises the first MISFET including gate electrodes formed on the main surface of a semiconductor substrate via a gate insulating film and a semiconductor

area being in contact with a channel area on the main surface of the semiconductor substrate under the gate electrodes; and the second MISFET including the gate electrodes formed on the main surface of a semiconductor substrate via a gate insulating film and a low density semiconductor area in contact with a channel area on the main surface of the semiconductor substrate under the gate electrodes and a high density semiconductor area formed outside the low density semiconductor area, wherein a cap insulating film is formed on top of the first and second MISFET gate electrodes, the first side walls composed of the first insulating film are formed on side surfaces of the second MISFET gate electrodes, and the second side walls composed of the second insulating film composed with a member different from that of the first insulating film are formed outside the first side walls. Then, a conductor portion connecting the first MISFET semiconductor area to a member formed in the upper layer of the first MISFET is formed in a self-matching manner with respect to the third side walls formed with the first insulating film, and the second MISFET high density semiconductor is formed in a self-matching manner with respect to the second side walls formed with the second insulating film.

According to the semiconductor integrated circuitry, since the first and second insulating films are formed on

side surfaces of the gate electrodes, the connecting portion connecting a member formed in the upper layer of the first MISFET is formed in a self-matching manner with respect to the third side walls formed with the first insulating film, and the second MISFET high density semiconductor area is formed in a self-matching manner with respect to the second side walls formed with the second insulating film, the degree of integration and the performance of the semiconductor integrated circuitry can be improved significantly.

In other words, the third side walls formed with the first insulating film can secure the self-matching properties of the conductor portion used to connect the first MISFET semiconductor area to the member formed in the upper layer of the first MISFET, as well as the second side walls formed with the second insulating film can optimize the position of the high density semiconductor area necessary to form a so-called LDD of the second MISFET, so that the second MISFET high performance can be kept satisfactorily. In other words, the first insulating film may be, for example, a silicon nitride film, which is a material having an etching selection ratio for the silicon oxide film, which is a material of general interlaminar insulating films and the second insulating film may be a silicon oxide film that can block implanted ions necessary

for forming an LDD. And, the second insulating film does not disturb self-matching connection for the first MISFET. On the other hand, the first and second insulating films can function as effective spacers for forming the LDD. Consequently, as for the first insulating film, it is no need to take any space into consideration when in designing an LDD structure and it is only needed to make the second insulating film thick enough to realize the self-matching connection. Thus, the second insulating film can be reduced in thickness to make the first MISFET integrated more highly. On the other hand, as for the second insulating film, it is no need to take the interval between gate electrode wirings in the first MISFET forming area into consideration. Thus, side wall spacers can be formed with a film thickness enough to keep the second MISFET performance, so that the performance of the second MISFET can be improved more significantly.

The first insulating film can be the first and third side wall spacers composed of a silicon nitride film formed on side surfaces of the gate electrodes and the second insulating film can be the second side wall spacers composed of a silicon oxide film formed on side surfaces of the gate electrodes with a first side wall spacer put therebetween respectively.

The first insulating film can be a silicon nitride film formed on the semiconductor substrate including side surfaces of the gate electrodes and the second insulating film can be side wall spacers composed of a silicon oxide film formed on side surfaces of the gate electrodes with a silicon nitride film put therebetween respectively. In such a case, when the connecting holes are opened for connecting each MISFET, the etching process can be divided into the first etching process for etching a silicon nitride film and the second etching process for etching a silicon nitride film, so that a silicon nitride film can be used as an etching stopper for the first etching process. When the etching process is divided into two stages such way, connecting holes can be opened surely in the first etching and over-etching can be prevented in the second etching process.

Furthermore, the semiconductor integrated circuitry of the present invention includes an N channel MISFET and a P channel MISFET in the second MISFET and can have a C (Complementary) MISFET structure. According to the semiconductor integrated circuitry, a higher performance and a lower power consumption can be realized due to the CMISFET structure, so that it is possible to form not only DRAM peripheral circuits, but also logic circuits using the second MISFET. Thus, the semiconductor integrated circuitry can have memory and logic circuits together.

(2) The semiconductor integrated circuitry of the present invention is as described in (1), and the first MISFET is a DRAM selecting MISFET disposed in the DRAM cell memory array area and the member formed in the upper layer of the first MISFET is a DRAM storage capacitor or a bit line.

According to the semiconductor integrated circuitry, the DRAM memory cell integration degree is improved and the performance of the peripheral circuits formed with the second MISFET is improved, so that it is possible to realize a high speed high performance DRAM integrated circuitry.

In addition, phosphorus is doped in the selecting MISFET semiconductor area as an impurity and at least arsenic can be doped in the low density or high density semiconductor area of the N channel MISFET of the second MISFET. In addition, the N channel MISFET can include the first N channel MISFET and the second N channel MISFET, and the first N channel MISFET can include an arsenic doped low density semiconductor area, a phosphorus doped high density semiconductor area, and a arsenic doped high density semiconductor area. In addition, the first N channel MISFET can include a semiconductor in which boron is doped in an area in contact with the high density semiconductor area under the low density semiconductor area, and the second N channel MISFET does not include any boron doped semiconductor area.

When phosphorus is doped in the selecting MISFET semiconductor area as an impurity such way, the selecting MISFET dielectric strength can be improved and the leak current from between source and drain can be reduced to improve the refreshing characteristics of the DRAM.

Furthermore, when arsenic is doped in both low density and high density semiconductor areas of the first N channel MISFET, the first N channel MISFET channel length can be shortened and when phosphorus is doped in the low density semiconductor area and arsenic is doped in the high density semiconductor area of the second N channel MISFET, the dielectric strength of the second N channel MISFET can be improved significantly. Furthermore, since a boron-doped semiconductor area is formed in the first N channel MISFET so as to function as a punched-through stopper, the channel length can further be shortened and since no punched-through stopper is provided in the second N channel MISFET, the dielectric strength of the MISFET can further be improved.

Furthermore, it can be expected that no silicide layer is formed on the surface of the selecting MISFET semiconductor area and a silicide layer is formed on the surface of the high density semiconductor area. Since no silicide layer is formed on the surface of the selecting MISFET semiconductor area, the leak from between channels can be suppressed to form a DRAM having excellent refreshing

characteristics, and since a silicide layer is formed on the surface of the high density semiconductor area, the resistance in the second MISFET connecting holes and the sheet resistance of the semiconductor area can be reduced to make the MISFET operation faster and improve the performance of the semiconductor integrated circuitry.

The selecting MISFET gate insulating film can be thicker than the second MISFET gate insulating film. Since the second MISFET gate insulating film is thinned such way, the second MISFET channel length can be shortened, and since the selecting MISFET gate insulating film is thickened such way, the dielectric strength of the MISFET can be improved to form a DRAM having excellent refreshing characteristics. Furthermore, when the second MISFET channel length is shortened, the semiconductor integrated circuitry can increase the MISFET driving current and enable its performance to be higher and its operation to be faster.

(3) The semiconductor integrated circuitry of the present invention is as described in (1), and the first MISFET gate can be a floating gate type MISFET, where the insulating film is a tunnel insulating film. The floating gate type MISFET is disposed in the memory array area for nonvolatile memory cells including the gate electrodes, floating gates, and control gates formed on the floating electrodes via an insulating film.

According to the semiconductor integrated circuitry, just like the DRAM described in (2), the memory array area for the nonvolatile memory cells can be highly integrated and the performance of the peripheral circuit MISFET of the nonvolatile memory composed of the second MISFET can be improved significantly.

The second MISFET gate insulating film can be thicker than the first MISFET gate insulating film. Since the second MISFET gate insulating film is thickened such way, the dielectric strength of the peripheral circuit MISFET of the nonvolatile memory driven with a general high voltage can be increased more significantly.

(4) The semiconductor integrated circuitry of the present invention includes both the DRAM and the nonvolatile memory as described in (2) and (3). In other words, the first MISFET includes both the selecting MISFET and the floating gate type MISFET.

According to the semiconductor integrated circuitry, the DRAM and the nonvolatile memory array area can be highly integrated and the peripheral or logic circuit area can also be highly integrated.

The DRAM bit line and the wiring formed in the upper layer of the floating gate type MISFET can be formed in the same process. Consequently, the number of processes can be reduced.

The insulating films of the selecting MISFET, the floating gate type MISFET, the peripheral circuit or logic circuit MISFET that drives the DRAM, and the peripheral circuit MISFET that drives the floating gate type MISFET are differ in thickness from each other. And, it can be expected that the gate insulating film of the peripheral circuit MISFET that drives the floating gate type MISFET is thicker than that of the floating gate type MISFET, and the gate insulating film of the floating gate type MISFET is thicker than that of the selecting MISFET, and the selecting MISFET gate insulating film is thicker than the gate insulating film of the peripheral circuit or logic circuit MISFET that drives the DRAM. Consequently, the gate insulating films of the selecting MISFET, the floating gate type MISFET, and the peripheral circuit or logic circuit MISFET that drives the DRAM, and the peripheral circuit MISFET that drives the floating gate type MISFET can be optimized in thickness for each MISFET.

In the semiconductor integrated circuitry as described in any of (1) to (4), it can be expected that a silicon nitride film is formed in the second MISFET formed area so as to cover the second MISFET and the semiconductor substrate respectively.

According to the semiconductor integrated circuitry, since a silicon nitride film is formed in the peripheral

circuit or logic circuit area on the semiconductor substrate, the element isolating area can be prevented from over-etching even when connecting holes are formed in the element isolating area on the semiconductor substrate. Thus, no leak occurs from between elements. And accordingly, the semiconductor integrated circuitry can prevent generation of defects, improving the reliability and performance.

(5) The manufacturing method of the semiconductor integrated circuitry of the present invention includes processes (a) for forming a gate insulating film on the main surface of a semiconductor substrate; (b) for forming gate electrodes and a cap insulating film on the gate insulating film; (c) forming a low density semiconductor area of the first and second MISFETs in a self-matching manner respectively with respect to the gate electrodes; (d) for forming the first side wall spacers on side surfaces of each of the gate electrodes; (e) for forming the second side wall spacers outside the first side wall spacers; (f) for forming a high density semiconductor area in a self-matching manner with respect to the second side wall spacers of the second MISFET; (g) for depositing an interlaminar insulating film composed of a silicon oxide film all over the semiconductor substrate; (h) etching the interlaminar insulating film and the second side wall spacers and opening the connecting

holes in a self-matching manner with respect to the first side wall spacers of the first MISFET; and (i) for forming a conductor portion in each of the connecting holes.

Furthermore, the manufacturing method of the semiconductor integrated circuitry of the present invention includes processes (a) for forming a gate insulating film on the main surface of a semiconductor substrate; (b) for forming gate electrodes and a cap insulating film on the gate insulating film; (c) forming a low density semiconductor area of the first and second MISFETs in a self-matching manner respectively with respect to the gate electrodes; (d) for depositing a silicon nitride film all over the surface of the semiconductor substrate including the side surfaces of each of the gate electrodes; (e) for forming side wall spacers on side surfaces of the gate electrodes with a silicon nitride film formed therebetween; (f) for forming a high density semiconductor area in a self-matching manner with respect to the side wall spacers of the second MISFET; (g) for depositing an interlaminar insulating film composed of a silicon oxide film all over the semiconductor substrate; (h) etching the interlaminar insulating film and the side wall spacers to form openings in a self-matching manner with respect to the silicon nitride film, further etching the silicon nitride film at the bottom of each

opening to open the connecting holes; and (i) for forming a conductor portion in each of the connecting holes.

According to the semiconductor integrated circuitry, it is possible to form a semiconductor integrated circuitry as described in (1).

(6) In the process (c), the manufacturing method of the semiconductor integrated circuitry can implant phosphorus in the first MISFET semiconductor area and implant arsenic in at least one or more low density n-type semiconductor areas of the second MISFET. According to the manufacturing method of the semiconductor integrated circuitry, the dielectric strength of the first MISFET can be improved and when arsenic is implanted in the low density semiconductor area of the second MISFET, the second MISFET channel length can be shortened.

Furthermore, in the process (a), both the first MISFET gate insulating film and the second MISFET gate insulating film can be formed in the same process.

In such a case, the gate insulating film forming process can be shortened and simplified.

Furthermore, the process (a) for forming an insulating film can include a process for forming the first gate insulating film in an area where the first and second MISFETs are formed, a process for removing the first insulating film selectively from the area where the second

MISFET is formed, and a process for forming the second insulating film in an area where the second MISFET is formed. When those additional processes are included in the process (a), since the first and second MISFET gate insulating films can be formed differently in thickness from each other and after the first gate insulating film is formed, the second insulating film is formed, the second gate insulating film can be thinner than the first gate insulating film.

The manufacturing method of the semiconductor integrated circuitry of the present invention is as described in (5), and the gate insulating film can be a tunnel insulating film of the floating gate type MISFET composing a nonvolatile memory and the process for forming gate electrodes can include a process for forming the floating gate electrodes of the floating gate type MISOET and a process for forming the control gate electrodes of the floating gate type MISFET. According to the manufacturing method of the semiconductor integrated circuitry, it is possible to form a nonvolatile memory in which the memory array area can be highly integrated and the performance of the peripheral circuit area can be improved significantly.

(8) The manufacturing method of the semiconductor integrated circuitry of the present invention is as described in (5) or (6), and in prior to the process (a) are included a process for forming the tunnel insulating film

of the floating gate type MISFET composing a nonvolatile memory on the main surface of the semiconductor substrate and a process for forming the floating gate electrodes of the floating gate type MISFET on the tunnel insulating film.

According to the manufacturing method of the semiconductor integrated circuitry, it is possible to manufacture a semiconductor integrated circuitry provided with both DRAM and nonvolatile memory in which the memory array area is highly integrated and the performance of the peripheral circuit area is improved significantly.

The gate electrodes formed in the process (b) and the control gates of the floating gate type MISFET can be formed in the same process to simplify the process.

Furthermore, the tunnel insulating film can be thicker than the gate insulating film formed in the process (a).

(9) The manufacturing method of the semiconductor integrated circuitry is as described in (5) to (8), and in prior to the process (g) can be included a process for depositing the second silicon nitride film in the area where the second MISFET is formed, etching the interlaminar insulating film in the area where the conductor portion connecting the second MISFET to a member formed in the upper layer of the second MISFET on conditions decided so that an etching selection ratio can be taken for the second silicon

nitride film to form openings, and furthermore etching the second silicon nitride film at the bottom of each opening to open connecting holes to form a conductor portion.

According to the manufacturing method of the semiconductor integrated circuitry, since etching of the interlaminar insulating film is stopped by the second silicon nitride film, then the second silicon nitride film that can be thinned much more than the interlaminar insulating film can be etched, over-etching will be enough if it is made up to $1/2$ of the second silicon nitride film. And, even when connecting holes overlap on the element isolating area on the semiconductor substrate, the element isolating area can be prevented from over-etching. Consequently, a proper etching process margin can be secured, the element isolating function of the element isolating area can be kept, and the performance and reliability of the semiconductor integrated circuitry can be secured.

The second silicon nitride film and the silicon nitride film formed as the first insulating film can be formed in the same process.

Hereunder, the effects to be obtained by the representative inventions of the disclosed ones above will be described briefly.

(1) The present invention can provide a semiconductor integrated circuitry technology for dividing the memory cells of the DRAM or the nonvolatile memory finely so as to be integrated more highly and to make the operation faster in a semiconductor integrated circuitry provided with a DRAM or a nonvolatile memory.

(2) The present invention can provide a semiconductor integrated circuitry technology for dividing memory cells finely so as to be integrated more highly and make the operation faster in a semiconductor integrated circuitry provided with a DRAM or an electrically reloadable nonvolatile memory.

(3) It is possible to provide a technology for realizing a high performance semiconductor integrated circuitry with excellent DRAM refreshing characteristics.

(4) It is possible to provide a technology for realizing a highly reliable semiconductor integrated circuitry that can prevent the element isolating area on the semiconductor substrate from over-etching when connecting holes are opened.

(5) It is possible to simplify the manufacturing processes for a semiconductor integrated circuitry provided with a DRAM and an electrically reloadable nonvolatile memory.

BRIEF DESCRIPTION OF DRAWINGS

Fig.1 is a cross sectional view of the major portion of a semiconductor integrated circuitry in the first embodiment of the present invention. Fig.2 is a top view of a DRAM in a memory cell area, included in the semiconductor integrated circuitry in the first embodiment of the present invention. Fig.3 is a block diagram of the semiconductor integrated circuitry in the first embodiment of the present invention. Fig.4 is an equivalent circuit diagram of the DRAM included in the semiconductor integrated circuitry in the first embodiment of the present invention. Figs.5 to 25 are cross sectional or top views of an example of how to manufacture the semiconductor integrated circuitry in the first embodiment in order of the processes. Figs.48 and 49 are cross sectional views of another example of how to manufacture the semiconductor integrated circuitry in the first embodiment of the present invention in order of the processes.

Fig.26 is a cross sectional view of the major portion of a semiconductor integrated circuitry in the second embodiment of the present invention. Figs.27 to 29 are cross sectional views of a manufacturing method of the semiconductor integrated circuitry in the second embodiment in order of the processes.

Fig.30 is a cross sectional view of the major portion of a semiconductor integrated circuitry in the third

embodiment of the present invention. Figs.31 to 33 are cross sectional views of a manufacturing method of the semiconductor integrated circuitry in the third embodiment in order of the processes.

Fig.34 is a cross sectional view of the major portion of a semiconductor integrated circuitry in the fourth embodiment of the present invention. Figs.35 is an expanded cross sectional view of the areas C and D shown in Fig.34. Fig.36 is a top view of an electrically reloadable batch erasure type nonvolatile memory, so-called a flash memory array area included in the semiconductor integrated circuitry in the fourth embodiment. Fig.37 is an equivalent circuit diagram of the flash memory portion. Figs.38 to 46 are top or cross sectional view of a manufacturing method for the semiconductor integrated circuitry in the fourth embodiment in order of the processes.

Fig.47 is a cross sectional view of the major portion of a semiconductor integrated circuitry in the fifth embodiment of the present invention.

Fig.50(a) is a cross sectional view of a memory cell area of the DRAM in the sixth embodiment of the present invention. Fig.50(b) is a cross sectional view of a peripheral circuit area of the DRAM in the sixth embodiment. Fig.51 is a top view of the memory cell area of the DRAM

in the sixth embodiment. Fig.52(a) is a cross sectional view of the line IIIa-IIIa shown in Fig.51. Fig.52(b) is a cross sectional view of the line IIIb-IIIb shown in Fig.51. Figs.35 to 79 are cross sectional views of a manufacturing method for the DRAM in the sixth embodiment in order of the processes.

Figs.80 and 81 are cross sectional views of a manufacturing method for the DRAM in the seventh embodiment of the present invention. Figs.82 to 84 are cross sectional views of a manufacturing method for the DRAM in the eighth embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Hereunder, the embodiments of the present invention will be described with reference to the accompanying drawings. In all the drawings explaining the embodiments, the same numerals will be given to the members having the same functions, avoiding redundant explanation.

(1st Embodiment)

Fig.1 is a cross sectional view of the major portion of a semiconductor integrated circuitry in an embodiment of the present invention. Fig.2 is a top view of a DRAM memory cell area included in the semiconductor integrated circuitry in the first embodiment of the present invention. Fig.3 is a block diagram of the semiconductor integrated circuitry in the first embodiment of the present invention.

Fig.4 illustrates an equivalent circuit of a DRAM included in the semiconductor integrated circuitry in the first embodiment of the present invention.

The semiconductor integrated circuitry in the first embodiment of the present invention, as shown in the area A in Fig.1, includes storage capacity elements (capacitors) C2 and C3 for storing information and composing DRAM memory cells; selecting MISFETs Qs2 and Qs3 connected to the storage capacity elements C2 and C3; and word lines WL1 and WL4 adjacent to those Qs2 and Qs3. The cross section of the DRAM shown in Fig.1 indicates a cross section of the I-I line in the top view of the DRAM memory cell area shown in Fig.2. The semiconductor integrated circuitry in the first embodiment, as shown in the area B in Fig.1, includes an N channel MISFET Qn1, a P channel MISFET Qp1, and the second N channel MISFET Qn2 used to compose peripheral circuits other than DRAM memory cells, as well as other logical circuits.

The semiconductor integrated circuitry in the first embodiment, as shown in Fig.3, is a microcomputer formed on a semiconductor substrate 1 together with an information processing CPU; input and output ports; an analog digital circuit ADC; a timer, as well as a logical circuit LG; a ROM for storing OS, etc.; and a DRAM used as a memory. The circuits of the microcomputer are connected to each other

via a bus BUS. The N channel MISFET Qn1 and the P channel MISFET Qp1 can be used for logical configuration such as the information processing CPU.

As shown in the equivalent circuit in Fig.4, a single bit memory cell is comprised of the storage capacity element C for storing information and the selecting MISFET Qs (Qs2 and Qs3). The storage capacity element C and the selecting MISFET Qs are connected serially. The gate electrode of the selecting MISFET Qs is connected electrically to word lines WL (WK0, WL1, and WLn) and formed integrally. The word line WL is connected to a word line driver WD. One of the source or drain area of the selecting MISFET Qs is connected electrically to one side electrodes of the storage capacity element C. The other side electrodes of the source or drain area of the selecting MISFET are connected to a bit line BL and the bit line BL is connected to a sense amplifier SA. In such way, the single bit memory cell is disposed at an intersection point of the word line WL and the bit line BL. As to be described later, the word line WL is extended in the first direction and the bit line BL is extended vertically in the second direction.

The sense amplifier SA is not specified specially, but it can be comprised of the N channel MISFET Qn1 and the P channel MISFET Qp1. The N channel MOSFET used to compose the word line driver WD, as to be described later, can be

comprised of the N channel MISFET Qn2 containing different impurities in a low density semiconductor area from those of the N channel MISFET Qn1. In addition, this N channel MISFET Qn2 is used for a circuit of a charger pump circuit, as well as input and output ports as needed, which are operated with a higher voltage than that of the N channel MISFET Qn1.

Next, each part configuration will be described with reference to Fig.1 indicating a cross sectional view of the major portion of the semiconductor integrated circuitry in the first embodiment of the present invention.

The single bit memory cell is comprised of the storage capacity element C for storing information (C2 and C3) and the selecting MISFET Qs (Qs2 and Qs3). The selecting MISFET Qs is formed in a P-type well area 5 formed on the main surface of the P-type semiconductor substrate 1. The P-type well area 5 of the memory cell is separated electrically from the P-type semiconductor substrate in the N-type semiconductor area 3. Consequently, in order to prevent noises from other circuits mounted on the same semiconductor substrate 1 and reduce the DRAM bit line storage capacity, a substrate bias can be applied to the P-type well area 5, which is a channel area of the selecting MISFET Qs.

The selecting MISFET Qs is formed in an activating area 5b limited by a field insulating film 2 in the P-type

well area 5. The selecting MISFET Qs is comprised of a P-type well area 5 (channel forming area); a gate insulating film 6; a gate electrode 7; and a pair of low density N-type semiconductor areas 9 composing source/drain areas, into which impurities are doped at a low density. To reduce the resistance, the gate electrode 7 may be structured with multiple layers of a silicon film containing impurities of phosphorus (P), etc. or a silicon film on which silicide such as tungsten silicide (WSi) or a metallic film such as tungsten (W) is formed.

The top of the gate electrode 7 is covered with a silicon nitride film 8 and on the side surfaces of the gate electrode 7 and the silicon nitride film 8 are formed the first side wall spacers 14 composed of silicon nitride and the second side wall spacers 15 composed of silicon oxide. The silicon nitride film 8 is formed so that the same pattern is also formed on the gate electrodes 7.

In the low density N-type semiconductor area 9, for example, phosphorus can be doped as an impurity. Consequently, the strength of the electrical field (strength of the electrical field at the end portion of the drain) between the end portion of the gate electrodes 7 and the P-type well area 5 can be lowered, and further it is possible to prevent generation of defective crystallization

when impurities are implanted to reduce the leak current and extend the refreshing time.

As shown in Fig.6 to be described later, the selecting MISFET Qs is separated electrically from the memory cells (in units of a pair of memory cells) by a field insulating film 2 and the active area 5b is limited by the field insulating film 2.

One low density N-type semiconductor area 9 of the selecting MISFET Qs is connected to an electric conductor 20 via connecting holes 19 and the electric conductor 20 is connected to one side electrodes of the storage capacity element C for storing information.

The electric conductor 20 is formed in a self-matching manner with respect to the first side wall spacers 14 composed of silicon nitride. In other words, the connecting holes 19 are formed in a self-matching manner with respect to the first side wall spacers 14 composed of silicon nitride and formed on side surfaces of the gate electrodes 7. Since the second side wall spacers 15 are formed with silicon oxide, which is the same material as that of the insulating film 18 to be described later and the second side wall spacers 15 and the insulating film 18 are formed with a material whose etching rate is different from that of the first side wall spacers 14, the electric conductor 20 can be connected to the low density N-type semiconductor area

9 in a self-matching manner such way with respect to the first side wall spacers 14. In other words, when the insulating film 18 and the second side wall spacers 15 are to be etched, the first side wall spacers 14 are etched under more strict etching conditions than those of the silicon oxide. Consequently, when the connecting holes 19 are to be formed, the connecting holes 19 are opened widely and a proper large margin is secured, so that the interval between gate electrodes 7 can be reduced to improve the integrating degree. This is because the electric conductor 20 is connected in a self-matching manner with respect to the first side wall spacers 14. In other words, as to be described with reference to Fig.8, even when the interval between adjacent word lines in the second direction, that is, the interval between gate electrodes 7 is reduced to improve the integrating degree, the connecting holes 19 can be opened widely and the contact resistance of each hole can be lowered. In addition, when the connecting holes 19 are formed by lithography, the margin of alignment in the second direction can be reduced, so the interval in the second direction can be reduced.

In the first embodiment, the connecting holes 19 are formed not to be positioned on top of the gate electrodes 7. On top of the gate electrodes 7, however, a silicon nitride film 8 is also formed, so the connecting holes 19

may be opened so as to be positioned on the gate electrodes 7. Consequently, a larger margin of alignment can be secured.

The other low density N-type semiconductor area of the selecting MISFET Qs is formed integrally with the bit line BL and connected to an electric conductor 22 via the connecting holes 21.

Just like the electric conductor 20, the electric conductor 22 is also formed in a self-matching manner with respect to the first side wall spacers formed with silicon nitride on side surfaces of the gate electrodes 7. In addition, just like the connecting holes 19, the connecting holes 21 led to the bit line BL may be extended to be positioned on top of the gate electrodes 7. Consequently, like the connecting holes 19, the connecting holes 21 can be opened widely and take a large margin of alignment. The interval between gate electrodes 7 (interval between word lines WL) can thus be reduced to improve the integrating density. In other words, as to be described later with reference to Fig.20, even when the interval between adjacent memory cell selecting MISFETs Qs in the second direction, that is, the interval between gate electrodes is reduced to improve the integrating degree, the connecting holes 21 can be opened widely and the contact resistance of each hole can be lowered. And, when the connecting holes 21 are to be

formed by lithography, the margin of alignment in the second direction can be reduced, so the interval between gate electrodes 7 in the second direction can also be reduced.

The electric conductors 20 and 22 may be formed with silicon containing impurities such as phosphorus, etc. or silicide such as WSi to lower the resistance.

The storage capacity element C for storing information is composed of electric conductors 25 and 27 composing one side electrodes (lower electrodes), a dielectric material 28 and upper electrodes 29 composing the other side electrodes. As to be described later with reference to Fig.22, the electric conductors 25 and 27 are connected to the electric conductor 20 via connecting holes 24 and isolated electrically from one side respective electrodes of the other storage capacity element C for storing information. Each of the one side electrodes is connected to one low density N-type semiconductor area of one selecting MISFET Qs corresponding to the electrode. Each of the other side electrodes of the storage capacity element C for storing information are connected electrically to between plural memory cells. In an area (not illustrated), for example, those electrodes are connected to a plate potential generator circuit whose voltage is $1/2$ of the supply voltage.

The electric conductors 25 and 27, and the upper electrodes 29 are formed with a silicon film containing impurities such as phosphorus to reduce, for example, the resistance respectively. The dielectric material film 28 is formed with a laminated film composed of, for example, a silicon nitride film and a silicon oxide film, or a laminated film composed of a tantalum oxide film, etc.

The N channel MISFET Qn1 is formed in the P-type well area 5 and the Qn1 is composed of the P-type well area 5 (channel forming area); a gate insulating film 6; gate electrodes 7; and a pair of low density semiconductor areas 10 composing a source and a drain. Under the low density semiconductor areas 10 is formed a P-type semiconductor area 11 to obtain an N channel MISFET (short channel) whose gate is shorter than that of the N channel MISFET Qn1. The P-type semiconductor area 11 functions as a so-called punched-through stopper of the MISFET.

Just like the DRAM selecting MISFET Qs, a silicon nitride film 8 is formed on the gate electrodes 7 and on side surfaces of the gate electrodes 7 are formed the first side wall spacer 14 composing of silicon nitride and the second side wall spacers 15 composing of silicon oxide. The high density N-type semiconductor area 16, as described later, is formed in a self-matching manner with respect to the second side wall spacers 15 composing of silicon oxide.

Since the high density N-type semiconductor area 16 is formed in a self-matching manner with respect to the second side wall spacers 15 such way, the thickness of the second side wall spacers 15 can be optimized to improve the performance of the N channel MISFET Qn1.

The low density N-type semiconductor area 10 is implanted, for example, arsenic (As) as an impurity to obtain a long-gate and short-channel N channel MISFET. Since the thermal diffusion coefficient of arsenic is smaller than that of phosphorus, the horizontal diffusion of impurity can be shortened. It is thus possible to obtain a long-gate and short-channel N channel MISFET. In addition, since the thermal diffusion coefficient is small such way, the density of the low density semiconductor area 10 can be more increased. The parasitic resistance can thus be reduced and a high performance N channel MISFET can be obtained. The low density N-type semiconductor area 10 is formed in a self-matching manner with respect to the gate electrodes 7 and the silicon nitride film 8.

Under the low density semiconductor area 10 is formed a P-type semiconductor area 11 that functions as a punched-through stopper. Boron (B) is implanted into the area P-type semiconductor area 11 as an impurity. Since this P-type semiconductor area 11 is provided such way, the extension of a barrier layer can be suppressed, and

accordingly the short channel characteristics can be improved.

The P channel MISFET Qp1 is formed in the N type well area 4. The Qp1 is composed of the N type well area 4 (channel forming area); a gate insulating film 6; gate electrodes 7, and a pair of low density P-type semiconductor areas 12 composing a source and a drain. The low density P-type semiconductor area 12 is formed between the channel forming area and the high density P-type semiconductor area 17. Under the low density P-type semiconductor area 12 is formed an N-type semiconductor area 13 to obtain a short-gate and short-channel P channel MISFET, which can be obtained by shortening the gate length of the P channel MISFET Qp1. The N-type semiconductor area 13 functions as a so-called punched-through stopper of the MISFET. Just like the DRAM selecting MISFET Qs, a silicon nitride film 8 is formed on the gate electrodes 7. On the side surfaces of both the gate electrodes 7 and the silicon nitride film 8 are formed the first side wall spacers 14 composed of silicon nitride and the second side wall spacers 15 composed of silicon oxide. The high density P-type semiconductor area 17, as to be described later, is formed in a self-matching manner with respect to the second side wall spacers 15 composed of silicon oxide. Since the high density P-type semiconductor area 17 is formed in a self-matching manner with respect to

the second side wall spacers 15 such way, the thickness of the second side wall spacer 15 can be optimized to improve the performance of the P channel MISFET Qp1. Consequently, the high density P-type semiconductor area 17 can be prevented from diffusion over the low density P-type semiconductor area 12.

Boron is implanted into the low density P-type semiconductor area 12 as an impurity. Under the low density P-type semiconductor area 12 is formed an N-type semiconductor area 13, which functions as a punched-through stopper. The N-type semiconductor area 13 is implanted with arsenic or phosphorus as an impurity. Since the N-type semiconductor area 13 is provided such way, the extension of the barrier layer can be suppressed and further the short channel characteristics can be improved.

The N channel MISFET Qn2 is formed in the P type well area 5 and composed of the P type well area 5 (channel forming area); a gate insulating film 6; gate electrodes 7; and a pair of low density semiconductor areas 10b composing a source and a drain; and the high density N-type semiconductor area 16b. The pair of low density semiconductor areas 10b are formed between the channel forming area and the high density N-type semiconductor area 16b. Just like the DRAM selecting MISFET Qs, on the gate electrode 7 is formed a silicon nitride film 8 and on the

side surfaces of the gate electrodes 7 are formed the first side wall spacer 14 composed of silicon nitride and the second side wall spacers 15 composed of silicon oxide. And, the low density semiconductor area 10b is formed in a self-matching manner with respect to the gate electrodes 7 and the silicon nitride film 8. The high density N-type semiconductor area 16b, to be described later, is formed in a self-matching manner with respect to the second side wall spacers 15 composed of silicon oxide. Since the high density N-type semiconductor area 16b is formed in a self-matching manner with respect to the second side wall spacers 15 such way, the high density N-type semiconductor area 16b can be prevented from diffusion over the low density semiconductor area 10b and the strength of the electrical field in the low density semiconductor area 10b can be reduced. In addition, the thickness of each second side wall spacer 15 can be optimized so as to have a specified resistance value and to improve the performance of the N channel MISFET Qn2. In other words, even when the thickness of the second side wall spacer 15 is optimized to improve the performance of the N channel MISFET Qn2, the interval between word lines WL in the second direction in the memory cell array, that is, the interval between gate electrodes of the selecting MISFET Qs can be reduced and the connecting holes 19 and 20 can be

opened widely to take a large margin of alignment. Thus, the contact resistance of each hole can be lowered.

For example, phosphorus is implanted into the low density N-type semiconductor area 10b as an impurity and under the low density N-type semiconductor area 10b is not provided a punched-through stopper of the P type semiconductor area. Since the low density N-type semiconductor area 10b of the N channel MISFET Qn2 contains phosphorus as an impurity, the withstand voltage can be set higher than that of the N channel MISFET Qn1 in which the same low density semiconductor area 10 is formed with arsenic. In addition, since no punched-through stopper is provided, the withstand voltage can be set higher. This N channel MISFET Qn2 can be used for a circuit such as a DRAM word line driver WD, a charge pump circuit, or an input/output port, which must operate with a higher voltage than that of the N channel MISFET Qn1.

The semiconductor area composing each source/drain of the N channel MISFET Qn1, the N channel MISFET Qn2, and the P channel MISFET Qp1 is connected to a connecting member 31 connected to the first wiring 32, via connecting holes 30. The connecting member 31 can be formed in a self-matching manner with respect to the first side wall spacers 14 composed of silicon nitride on side surfaces of the MISFET gate electrodes 7 in case of need. In Fig.1, the side

surfaces of the gate electrodes 7 mentioned here are the left connecting area of the P channel MISFET Qp1.

In addition, each line of the first wiring 32 is connected to a connecting member 35 connected to the second wiring 36, via a connecting hole 34. Each line of the second wiring 36 is connected to a connecting member 39 connected to the third wiring 40, via a connecting hole 38. And, on those first, second, and third wirings is formed a passivation film 41 on which a bonding area 42 formed.

The material of the connecting members 31, 35, and 39 for connecting upper and lower wirings is not specified specially, but may be composed of tungsten (W). The material of the wirings 32, 36, and 40 is not specified specially, but may be composed of an integrated film of titanium nitride (TiN) and aluminum (Al) containing copper (Cu).

Each line of the wirings 32, 36, and 40 is insulated by insulating films 18, 23, 33, and 37 respectively and the insulating films 18, 23, 33, and 37 can be formed with a silicon oxide film or a silicon oxide film into which either of boron or phosphorus, or both of them are doped. The passivation film 41 can be formed with a silicon oxide film or a silicon oxide film into which either of boron or phosphorus, or both of them are doped, or a silicon nitride film formed on the film.

Next, a method for manufacturing the semiconductor integrated circuitry in the first embodiment will be described with reference to Figs.5 to 25. Figs.5 to 25 are cross sectional or top views indicating a method for manufacturing the semiconductor integrated circuitry in the first embodiment in order of the processes.

At first, as shown in Figs.5 and 6, field insulating films 2 are formed in specified areas on the P type semiconductor substrate 1. The field insulating films 2 can be formed with silicon nitride using the LOCOS (Local Oxidation of Silicon) method that uses a well-known selective oxidation method or a shallow groove isolation method to be explained briefly below.

The shallow isolation method forms a silicon oxide film (not illustrated) and a silicon nitride film sequentially on the main surface of a P type semiconductor substrate 1. Then, the silicon oxide film and the silicon nitride film are removed with photo resist, etc. from the area where the field insulating film 2 is formed.

Thereafter, a 0.3 to 0.4 μm groove is formed in the depth direction of the P type semiconductor substrate 1. Then, a thermal silicon oxide film is formed on the side surfaces and at the bottom surface of the groove using the silicon nitride film as an oxidation mask. And, a silicon oxide film is deposited all over the thermal silicon oxide film with

the CVD (Chemical Vapor Deposition) method, then the silicon oxide film is removed from the area except for the groove with the CMP (Chemical Mechanical Polishing) method or the dry etching method, silicon oxide embedding selectively in the groove. The silicon oxide film is densified (thermal treatment for densifying) with the CVD method in an acid atmosphere. Then, the silicon nitride film is removed, so that the field insulating film 2 is formed with the shallow groove isolation method. The residual portions are formed as active areas 5b.

Next, an N type semiconductor area 3 is formed as shown in Fig.7. The N type semiconductor area 3 can be formed, for example, using photo resist as a mask and by ion-implantation of phosphorus, under the conditions (accelerating energy of 500 to 1000 keV and a dosing amount of about 1×10^{12} atoms/cm²). The phosphorus is implanted once or a few times by changing the conditions each time. Thereafter, impurities of the area are activated with a thermal treatment of about 1000°C. In this case, the thermal treatment can be performed for 20 to 30 min in an atmosphere of nitrogen including about 1% of oxygen. Preferably, the RTA (Rapid Thermal Annealing) method that uses an infrared light for heating should be used to finish the thermal treatment within a short time to enable the distribution of impurities to be controlled.

Next, an N type well area 4 and a P type well area 5 are formed. The N type well area 4 can be formed, for example, using photo resist as a mask and by ion-implantation of phosphorus, which implantation is performed once or a few times by changing the conditions each time, under the conditions (an accelerating energy of 300 to 500 keV and a dosing amount of about 1×10^{13} atoms/cm²). The P type well area 5 can be formed, for example, using photo resist as a mask and by ion-implantation of boron, under the conditions (an accelerating energy of 200 to 300 keV and a dosing amount of about 1×10^{13} atoms/cm²). The phosphorus is implanted once or a few times by changing the conditions each time. Thereafter, a thermal treatment of about 1000°C is performed to activate the impurities. In this case, the thermal treatment can be performed for 20 to 30 min in an atmosphere of nitrogen including about 1% of oxygen. Preferably, the RTA (Rapid Thermal Annealing) method should be used to finish the thermal treatment within a short time to enable the distribution of impurities to be controlled.

Then, as shown in Figs.8 and 9, the silicon oxide film is removed from the P type semiconductor substrate 1 and a clean gate insulating film 6 is newly formed. A silicon oxide is formed with a thermal oxidation method of 700 to 800°C, then a gate insulating film 6 composing of a silicon oxide film containing nitrogen by a thermal treatment in an

atmosphere of nitrogen oxide composed of NO or N₂O is formed. In the atmosphere of NO, the thermal treatment in the atmosphere of nitrogen oxide can be performed at 900 to 1000°C. In the atmosphere of N₂O, the thermal treatment can be performed at 1000 to 1100°C for 20 to 30 min respectively. Otherwise, the RTA method can be used to finish the thermal treatment within a short time at 1000 to 1100°C. With this thermal treatment, the phase boundary between the gate insulating film 6 and the P type semiconductor substrate 1 is formed satisfactorily, so that the gate insulating film 6 can be suppressed from degradation due to the hot carrier generated by a MISFET operation. The reason why this phase boundary is formed satisfactorily is based on the presumption that Si-N binding that is stronger than the Si-O binding is formed on the phase boundary between the gate insulating film 6 and the semiconductor substrate 1.

The thickness of the gate insulating film 6 is set so that the maximum electrical field becomes 5 MeV/cm or under in operation. For example, when in an operation at 3.3V, the thickness can be set to 7 to 9nm. When in an operation at 2.5V, the thickness can be set to 5 to 7nm and when in an operation at 1.8V, the thickness can be set to 4 to 5nm.

Next, the gate electrodes 7 and the silicon nitride film 8 are formed sequentially. Each gate electrode 7 is formed with a silicon film containing impurities such as

phosphorus or with a multi-layer structure formed with silicide such as WSi or metal such as W is formed on a silicon film. Those conductor films are deposited all over the surface with the CVD method or sputtering method. Then, a silicon nitride film 8 is deposited all over the film with the CVD or plasma CVD method, then for example, a silicon nitride film and a conductor film are patterned sequentially as specified using photo resist as a mask. With this, the gate electrodes such as the DRAM memory cell selecting MISFET Qs, the N channel MISFET Qn1, the N channel MISFET Qn2, and the P channel MISFET Qp1, as well as the word lines WL extended in the first direction are formed. The channel length of each gate electrode 7 is formed so as to be 0.2 to 0.4 μm . On the gate electrodes 7 and the word lines WL is formed a silicon nitride film 8 so as to have on the same flat pattern.

Channel impurities for controlling the MISFET threshold value (V_{th}) can be implanted by ion implantation before the gate insulating film 6 is formed or after the gate electrodes 7 are formed.

Next, a low density N-type semiconductor area 9 of the selecting MISFET Qs and a low density N-type semiconductor area 10b of the N channel MISFET Qn2 are formed selectively as shown in Figs. 10 and 11 using photo resist as a mask. The low density N-type semiconductor area 9, 10b are formed by

ion implantation of phosphorus at an acceleration energy of 20 to 40 keV and at a dosing amount of about 5×10^{13} atoms/cm². The low density N-type semiconductor area 9, 10b are formed such way by implanting impurities in a self-matching manner with respect to the gate electrodes 7 and the silicon nitride film 8. In other words, a low density N-type semiconductor area 9, 10b are formed in a self-matching manner with respect to the gate electrodes 7 and the silicon nitride film 8.

Next, the low density semiconductor area 10 of the N channel MISFET Qn1 and the P type semiconductor area 11 under the area 10 are formed selectively using photo resist as a mask. The low density semiconductor area 10 is formed, for example, by ion implantation of arsenic at an acceleration energy of 20 to 40 keV and at a dosing amount of about 1×10^{14} atoms/cm². In this case, arsenic can be implanted at an angle of 30 to 50° to the side surface of each gate electrode 7 (at 30 to 50° to the perpendicular of the P type semiconductor area), although it is not specified specially. Consequently, the low density semiconductor area 10 is also formed under the gate electrodes 7, so the hot carrier resistant properties can be improved. The low density N-type semiconductor area 10 is formed such way by implanting impurities in a self-matching manner with respect to the gate electrodes 7 and the silicon nitride film 8. In other words, the low density semiconductor area 10

is formed in a self-matching manner with respect to the gate electrodes 7 and the silicon nitride film 8.

The P-type semiconductor area 11 is formed, for example, by ion implantation of boron at an acceleration energy of 10 to 20 keV and a dose of about 1×10^{13} atoms/cm². In this case, boron can be implanted at an angle of 30 to 50° to the side surface of each gate electrode (at an angle of 30 to 50° to the perpendicular of the P type semiconductor area), although it is not specified specially. Consequently, the boron can be supplied enough under the low density semiconductor area 10, so that satisfactory short channel characteristics can be obtained.

Furthermore, the low density P-type semiconductor area 12 of the P channel MISFET Qp1 and the N-type semiconductor area 13 under the Qp1 are formed. The low density P-type semiconductor area 12 is formed, for example, by ion implantation of boron at an acceleration energy of 5 to 10 keV and a dose of about 5×10^{13} atoms/cm². In this case, boron can be implanted at an angle of 30 to 50° to the side surface of each gate electrode (at an angle of 30 to 50° to the perpendicular of the P type semiconductor area), although it is not specified specially. The N-type semiconductor area 13 is formed, for example, by ion implantation of phosphorus at an acceleration energy of 50 to 80 keV and a dose of about 1×10^{13} atoms/cm². In this case,

boron can be implanted at an angle of 30 to 50° to the side surface of each gate electrode (at an angle of 30 to 50° to the perpendicular of the P type semiconductor area). Consequently, the boron can be supplied enough under the low density P-type semiconductor area 12, so that satisfactory short channel characteristics can be obtained.

Thereafter, impurities are activated by a thermal treatment of about 850°C. In this case, the thermal treatment is performed for 20 to 30min in an atmosphere of nitrogen containing about 1% of oxygen. Preferably, the RTA method should be used to finish the thermal treatment of about 1000°C within a short time to control the distribution of impurities.

The thermal treatment can also be performed at 700 to 800°C in an atmosphere of oxidation before each of the low density semiconductor areas is formed. Consequently, the end portion of each gate electrode 7 that is thinned when in patterning can be reinforced, thus improving the withstand voltage of each gate.

As shown in Figs.12 and 13, the first side wall spacers 14 composed of silicon nitride are formed on the side surfaces of the gate electrodes 7 and each silicon nitride film 8. The first side wall spacers 14 can be formed by depositing a silicon nitride film all over the surface with the CVD or the plasma CVD method, then etching the film with

anisotropic dry-etching. The thickness of each first side wall spacer 14 composed of silicon nitride should be 0.04 to 0.08 μm in the longitudinal direction (the second direction) under the gate electrode 7. Consequently, each gate electrode 7 is covered with the silicon nitride film 8 on its top and with the first side wall spacer 14 composed of silicon nitride on its side surfaces. Thus, connecting holes 19 and 21 to be explained later can be opened in a self-matching manner. In addition, since the thickness of the first side wall spacer 14 can be thinned to about 0.04 to 0.08 μm , the interval between gate electrodes 7 of the selecting MISFET Qs in the second direction can be reduced to improve the integrating degree of the semiconductor integrated circuitry of the present invention.

The first side wall spacers 14 composed of silicon nitride can also be thinned and the low density semiconductor area may be formed after the first side wall spacers 14 are formed. In this case, more shorter channel characteristics can be obtained. In other words, as shown in Fig.48, after the first side wall spacers 14 are formed, low density N-type semiconductor areas 9, 10, and 10b, as well as a low density P-type semiconductor area 12 can be formed in a self-matching manner with respect to the first side wall spacers 14.

Next, as shown in Figs.14 and 15, the second side wall spacers 15 composed of silicon oxide are formed on the side surfaces of the first side wall spacers 14. The second side wall spacers 15 can be formed by depositing a silicon oxide film all over the surface with the CVD or plasma CVD method, then etching the film with anisotropic dry-etching. The thickness (width) of each second side wall spacer 15 should be greater than that of each first side wall spacer 14. The total thickness t_2 of the first side wall spacer 14 composed of silicon nitride and the second side wall spacer 15 composed of silicon oxide should be 0.1 to $0.15\mu\text{m}$ in the channel direction under the gate electrodes 7. At this time, even when a second side wall spacer 15 composed of silicon oxide fills between two gate electrodes 7 of the selecting MISFET Qs in the second direction, no problem will arise as to be described later. In other words, only a space t_3 of the first side wall spacer 14 composed of silicon nitride is needed between them. In other words, the connecting holes 19 and 21 can be opened in a self-matching manner with respect to the first side wall spacers 14, so the intervals t_3 of the first side wall spacers 14 in the second direction is assumed to be openings of the connecting holes 19 and 21 respectively. In other words, the thickness t_1 of the first side wall spacer 14 can be minimized in the second direction

until a specified contact resistance is assumed in the intervals t_3 of the first side wall spacers 14.

Next, the high density N-type semiconductor area 16 of the N channel MISFET Qn1 and the high density N-type semiconductor area 16b of the N channel MISFET Qn2 are formed as shown in Fig.16. The high density N-type semiconductor area 16, 16b of the N channel MISFET Qn1 and the high density N-type semiconductor area 16b of the N channel MISFET Qn2 can be formed, for example, by ion implantation by implanting arsenic at an acceleration energy of 20 to 60 keV and a dose of about 1 to 5×10^{15} atoms/cm². At this time, no high density semiconductor area is formed in the selecting MISFET Qs. Consequently, it is possible to suppress crystallization defects causing by ion implantation when in forming of a high density semiconductor area, and prevent a problem that the leak current from a PN junction is increased to shorten the refreshing time.

Next, the high density P-type semiconductor area 17 of the P channel MISFET Qp1 is formed. The high density P-type semiconductor area 17 can be formed, for example, by ion implantation of boron at an acceleration energy of 10 to 20 keV and at a dose of about 1 to 5×10^{15} atoms/cm². Thereafter, the impurities in the area are activated by a thermal treatment of about 850°C, which treatment is performed for 20 to 30 min in an atmosphere of nitrogen

containing about 1% of oxygen. Preferably, the RTA method should be used to finish the thermal treatment of about 1000°C within a short time to control distribution of the impurities.

Since the second side wall spacers 15 are provided and the high density semiconductor area can be formed with the optimal side wall spacer length t_2 such way, a high performance N channel MISFETs Q_{n1} and Q_{n2} , as well as a P channel MISFET Q_{p1} can be obtained. On the other hand, in the memory array, the thickness t_1 of the first side wall spacers 14 and the interval t_3 between the first side wall spacers 14 can be reduced respectively and the interval in the second direction can be minimized. In addition, the opening margin of the connecting holes 19 and 21 can be taken widely to lower the contact resistance.

Next, an insulating film 18 is formed as shown in Figs.17 and 18. The film 18 is composed of a silicon oxide film or a silicon oxide film into which either or both of boron and phosphorus are doped. The insulating film 18 is formed by depositing a silicon oxide film or a silicon oxide film into which one or both of boron and phosphorus are doped all over the surface, for example, with the CVD or plasma CVD method, then the film is smoothed with the reflowing method or the CMP method so that the height from the surface of the substrate is smoothed in uniform.

Furthermore, connecting holes 19 are formed so as to be connected to the one side electrodes of the storage capacity element C for storing information, for the DRAM memory cells. The connecting holes 19 are formed by dry-etching under the conditions decided so that the selection ratio of the silicon nitride film 8 on the gate electrodes 7 and the first side wall spacers 14 composed of silicon nitride to the second side wall spacers 15 composed of silicon oxide and the insulating film 18 composed of silicon oxide is set large. In other words, the etching conditions are set so that the etching speed (capacity) of the silicon nitride is slower and the etching speed (capacity) of the silicon oxide is faster. Such etching is possible when performed together with Ar sputtering performed for the mixed gas of, for example, C_4F_8 and O_2 . Etching under the conditions to allow the connecting holes 19 to be opened in a self-matching manner with respect to the first side wall spacers 14. In other words, since the light lithography technology is used to form the connecting holes 19, the margin of alignment in the second direction can be reduced and fine pitches can be assumed in the second direction.

Furthermore, a polycrystal silicon film containing impurities such as phosphorus is formed all over the semiconductor substrate 1 to lower the resistance. Then,

anisotropic etching is performed to remove the polycrystal silicon film except for the connecting holes 19 to form an electric conductor 20 in each of the connecting holes 19.

Thereafter, an insulating film (silicon oxide film, not illustrated) is deposited to cover the electric conductor 20.

Next, connecting holes 21 to be connected to the DRAM memory cell bit lines BL are formed as shown in Figs. 19 and 20. Dry etching is performed to form the connecting holes 21 on conditions in which a large selection ratio of silicon nitride to silicon oxide is taken, just like the connecting holes 19. Consequently, each of the connecting holes 21 can be opened in a self-matching manner with respect to the first side wall spacer 14. Thus, just like the connecting holes 19, when the light lithography is used to form the connecting holes 21, the margin of alignment in the second direction can be reduced and the fine pitches of members can be assumed in the second direction.

Furthermore, a silicon film containing impurities such as phosphorus or a silicide film such as WSi is formed to lower the resistance. Then, an electric conductor 22 is formed in each connecting hole 21 using photo resist as a mask and patterned so that the electric conductor 22 is extended vertically (to second direction) to the word line WL to serve as a bit line BL.

Next, as shown in Figs.21 and 22, an insulating film 23 composed of silicon oxide or silicon oxide into which one or both of boron and phosphorus are doped is formed. The insulating film 23 is formed just like the insulating film 18 with, for example, the CVD or plasma CVD method so that a silicon oxide film or a silicon oxide film in which one or both boron and phosphorus are doped is deposited all over the surface, then the film is flattened with the reflowing or CMP method so that the height from the surface of the substrate 1 is smoothed in uniform all over. Then, connecting holes 24 are formed so as to be connected to one side electrodes of the storage capacity element C for storing information of DRAM memory cells. The connecting holes 24 are dry-etched to form holes reaching the electric conductors 20. Such the etching is possible when performed together with Ar sputtering performed with a mixed gas of CF_4 and CHF_3 .

Furthermore, electric conductors 25 are formed. The electric conductors 25 are used as one side electrodes of the storage element C for storing DRAM memory cell information. Each electric conductor is formed with a polycrystal silicon film containing impurities such as phosphorus, etc. or a silicide film such as WSi , etc. to reduce the resistance. Then, an insulating film 26 composed of, for example, silicon oxide, is formed and an electric

conductor 25 is formed in each connecting hole using photo resist as a mark. And, both the insulating film 26 and the electric conductors 25 are patterned so as to be used as one side electrodes of the storage element C for storing information.

As shown in Fig.23, a polycrystal silicon film containing impurities such as phosphorus or a silicide film such as WSi is formed to lower the resistance. Then, anisotropic dry etching is performed to form electric conductors 27 connected to the electric conductors 25 on the side surfaces of each insulating film 26. The electric conductors 25 and 27 are used to form one side electrodes of the storage capacity element C for storing information.

As shown in Fig.24, after the insulating film 26 is removed, a dielectric material film 28 and upper electrodes 29 are formed sequentially for the storage capacitor element C for storing information. The dielectric material film 28 is formed with a laminated film composed of silicon oxide and silicon nitride or a tantalum oxide (Ta_2O_3) film. The upper electrodes 29 are formed with a polycrystal silicon film containing impurities such as phosphorus or a silicide film such as WSi to lower the resistance.

As shown in Fig.25, connecting holes 30 are formed. The connecting holes 20 are used to connect the first wiring 32 to gate electrodes or a semiconductor area. Just like

the connecting holes 19 and 21, the connecting holes 30 are formed on conditions to take a large selection ratio for the silicon nitride 8 and the first side wall spacers 14 composed of silicon nitride to the second side wall spacers 15 composed of silicon oxide and the insulating film 8 composed of silicon oxide. Then, a connecting member 31 is formed in each connecting hole 30. The connecting member 31 is formed by forming a titanium (Ti) film of 10 to 50 μm in thickness and titanium nitride (TiN) film of about 100nm in thickness by the sputtering method, then removing the tungsten film from areas other than the connecting holes 30 with dry etching or the CMP method.

Furthermore, the first wiring 32 is formed. The first wiring can be formed with a laminated film of a titanium nitride (TiN) and an aluminum (AL) film containing copper (Cu).

Finally, an insulating film 33, connecting holes 34, connecting members 35, the second wiring 36, an insulating film 37, connecting holes 38, connecting members 39, and the second wiring 40 are formed sequentially. The insulating films 33 and 37 are formed just like the insulating film 23. The connecting holes 34 and 38 are formed just like the connecting holes 30. The connecting members 35 and 39 and the second and third wirings 36 and 40 are formed just like the connecting members 31 and the first wiring 32. And, a

silicon nitride or a laminated passivation film 41 composed of silicon oxide is formed under the silicon nitride by the CVD method, then a bonding area 42 is formed almost to complete the manufacturing of the semiconductor integrated circuitry shown in Fig.1.

(2nd Embodiment)

Fig.26 is a cross sectional view of the major portion of a semiconductor integrated circuitry in another embodiment of the present invention.

The semiconductor integrated circuitry in the second embodiment is the same as that in the first embodiment except that a silicon nitride film 104 is formed on the N channel MISFET Qn1, the N channel MISFET Qn2, and the P channel MISFET Qp1 respectively, and this silicon nitride film 104 is used as an etching stopper for forming connecting holes 30. Thus, since other configuration items are the same as those in the first embodiment, explanation for them will be omitted. And, since a silicon nitride film 104 is provided such way in the semiconductor integrated circuitry in this second embodiment, even when some of connecting holes 30 overlap the field insulating film 2 as shown on the right side of the P channel MISFET Qp1 in Fig.26, the field insulating film 2 is prevented from over-etching when the connecting holes 30 are opened. Leak current and other problems to be caused by over-etching can thus be

suppressed, maintaining the performance and reliability of the semiconductor integrated circuitry.

Hereunder, a manufacturing method of the semiconductor integrated circuitry in the second embodiment will be described with reference to Figs.27 to 29. Figs.27 to 29 are cross sectional views indicating how to manufacture the semiconductor integrated circuitry in the second embodiment in order of the processes.

Just like the first embodiment, at first, the selecting MISFET Qs, the N channel MISFETs Qn1 and Qn2, and the P channel MISFET Qp1 are formed, then a silicon nitride film 104 is deposited on the N channel MISFETs Qn1 and Qn2, and the P channel MISFET Qp1 with a thickness of about 50nm respectively. Then, the silicon nitride film 104 masked with photo resist is not removed by etching except for at least the area where the connecting holes 19 and 21 of the DRAM memory cells are formed. (Fig.27)

Thereafter, just like in the first embodiment, the insulating film 18, the bit lines BL, the storage capacity element C for storing information are formed. Then, when the connecting holes 30 are opened, the first stage etching is performed (Fig.28). In this first stage etching, an etching selection ratio is set so that the silicon oxide etching is faster than the silicon nitride etching, so to speak, in the condition of high etching selection rate.

Consequently, the connecting holes 30 can be opened surely up to the surface of the silicon nitride 104. In addition, in this first stage etching, since the silicon nitride film 104 functions as an etching stopper, the etching can be performed enough to take a larger process margin without considering a peril of over-etching.

Next, the second stage etching is performed for the silicon nitride film 104 at the bottom of each connecting hole 30 (Fig.29). This second stage etching is performed on conditions for etching silicon nitride, and it is no need to take an etching selection ratio for silicon oxide. The etching at this time is decided to be a little deeper than the thickness of the silicon nitride film 104. For example, the etching depth is decided to be 110 to 130% of the thickness of the silicon nitride film 104. Such the etching is possible when performed together with AR sputtering with a mixed gas of CF_4 and CHF_3 . As a result, the field insulating film 2 is hardly etched. This prevents the bottom of each etched connecting hole 30 from becoming deeper than the semiconductor area composing a source and a drain. In other words, the silicon nitride film 104 is thinned enough with respect to the field insulating film 2, so that even when the silicon nitride film 104 is over-etched, the field insulating film 2 is etched only by less than a half of the

silicon nitride 104 in thickness, and the over-etching causes no problem to the processes.

Since the second stage etching is performed using such a silicon nitride film 104, the connecting holes 30 can be opened surely with an enough process margin. The performance and reliability of the semiconductor integrated circuitry can thus be maintained.

Hereafter, the manufacturing method of the second embodiment is completely the same as that of the first embodiment, thus the explanation will be omitted here.

(3rd Embodiment)

Fig.30 is a cross sectional view of the major portion of a semiconductor integrated circuitry in another embodiment of the present invention.

The semiconductor integrated circuitry in the third embodiment is the same as that in the first and second embodiments except that a silicide layer 105 is formed on the semiconductor areas except for at least the low density N-type semiconductor area composing the source and the drain of the DRAM memory cell selecting MISFET Qs. In addition, in this third embodiment, a silicon nitride film 104 is also provided just like in the second embodiment. Consequently, the parasitic resistance of the semiconductor area composing the sources and the drains of the MISFETs Qn1, Qn2, and Qp1 can be reduced to improve the performance of the

MISFET Qn1, Qn2, and Qp1 significantly without increasing the leak current from DRAM memory cells.

Next, a manufacturing method of the semiconductor integrated circuitry in the third embodiment will be described with reference to Figs.31 to 33. Figs.31 to 33 are cross sectional views of a manufacturing method of the semiconductor integrated circuitry in the third embodiment.

At first, just like the first embodiment, the high density N-type semiconductor areas 16 and 16b, and a high density P-type semiconductor area 17 shown in Fig.16 are formed. Then, an insulating film 106 is formed and the film 106 is removed by etching using photo resist as a mask except for at least the area of the DRAM memory cells (Fig.31). When an insulating film exists on the semiconductor area before the insulating film 106 is formed, the insulating film 106 is not formed, and instead, the insulating film mentioned above is removed selectively.

Next, a metallic film 107 composed of titanium (Ti) or cobalt (Co) is deposited all over the surface with the sputtering method (Fig.32). Then, the first silicide reaction is performed in an inactive atmosphere of about 500°C, then non-reacted portions of the metallic film 107 except for the semiconductor area are removed. Thereafter, in an inactive atmosphere of about 700 to 900°C, the second silicide reaction is performed to reduce the resistance and

form a silicide layer 105 (Fig.33). A silicide layer 105 is thus formed on the semiconductor area composing the sources and the drains of the MISFET Qn1, Qn2, and Qp1 except for the low density N-type semiconductor area 9 composing the source and the drain of the DRAM memory cell selecting MISFET Qs. No silicide layer 105 is needed on the semiconductor area composing sources and drains of the output circuit output MISFET and the input protection MISFET.

Hereafter, the processes are the same as those shown in Fig.27 in the second embodiment, so the explanation will be omitted here.

(4th Embodiment)

Fig.34 is a cross sectional view of the major portion of a semiconductor integrated circuitry in another embodiment of the present invention.

In the semiconductor integrated circuitry in the fourth embodiment, a flash memory is used as a ROM as shown in the block diagram in Fig.3 indicating the first embodiment of the present invention. In Fig.34, areas A and B are the same as those in the first embodiment. Thus, the explanation for those items will be omitted here.

Fig.35 is an expanded view of the areas C and D shown in Fig.34. Fig.36 is a top view of the memory array area of an electrically reloadable batch erasure type volatile

memory, that is, a flash memory included in the semiconductor integrated circuitry in the fourth embodiment. Fig.37 is an equivalent circuit diagram of the flash memory portion. Hereunder, explanation will be made with reference to Figs.35 to 37.

In the flash memory in this fourth embodiment, a single bit memory cell is composed of a tunnel insulating film 202; floating gate electrodes 203; an interlaminar insulating film 204; control gates 7 formed unitarily with word lines; P type well areas 5 (channel forming areas); and a floating gate MISFET Qf having a pair of N type semiconductor areas composing sources and drains.

Just like the N channel MISFET Qn1 in the first embodiment, the source of the floating gate type MISFET Qf is formed with a low density N-type semiconductor area 10 and a P-type semiconductor area 11 formed under the area 10, and a high density N-type semiconductor area 16. The drain of the floating gate type MISFET Qf is formed with a high density N-type semiconductor area 205. The thickness of the tunnel insulating film 202 is set to 9 to 10nm. The high density N-type semiconductor area 205 has a impurity density higher than that of the low density N-type semiconductor area 10 and has a high impurity density enough to reduce depression of the surface of the high density N-type

semiconductor area 205 under the floating gate electrodes 203 when information is written.

The drain of the floating gate type MISFET Qf is connected to the first wiring 32 via a connecting hole 30. The first wiring 32 composes sub-bit lines subBL in the fourth embodiment. A memory cell composed of 16 to 64 bits is connected to a sub-bit line subBL and to the main bit line BL composed of the second wiring 36 via the selecting MISFET Qs. In other words, the flash memory in this fourth embodiment is divided into blocks by the selecting MISFET Qsf. The block selecting lines tWL1 and tWL2 are formed unitarily with the gate electrodes 203 of the selecting MISFET Qsf.

The memory cell source is connected to the source line SL via a connecting hole 21. The source is also connected to the source line BSL shared by all the divided blocks.

The selecting MISFET Qsf selects a block. In other words, the potential of the main bit line BL is supplied to memory cells via the selecting MISFET Qsf. As shown in Fig.36, the word lines MWL (7), the block selection lines tWL1 and tWL2, and the source lines SL are extended in the first direction. The sub-bit lines subBL (32) are extended in the second direction.

The selecting MISFET Qsf is composed of a gate insulating film 201; floating gate electrodes 203; gate

electrodes 203 disposed in the same layer as the floating gate electrodes 203; and a high density N-type semiconductor area 205 composed of a source and a drain. In Fig.34, each gate electrode has a two-layer structure, but in an area (not illustrated), a control gate electrode 7 formed unitarily with a word line is connected to the first wiring 32, and shunted by the third wiring 40. The thickness of the gate insulating film 201 is set to about 20nm.

The connecting holes 21 and 30 connected to the source and the drain of the floating gate type MISFET Qf, as shown in Figs.45 and 46 to be described later, are formed in a self-matching manner with respect to the first side wall spacers 14 composed of silicon nitride just like the connecting holes 19 and 21 in the first embodiment. Those memory cells are isolated by the N type semiconductor area 3 so that writing and erasing to be described below are performed.

Writing data in the flash memory of the present invention is composed by discharging electrons from the floating gate electrodes 203 and lowering the threshold value (V_{th}). In other words, a negative voltage of about 9V is applied to the control electrodes 7. Then, a positive voltage of about 7V is applied to the drain so that electrons are discharged from the floating gate electrodes 203 to the high density N-type semiconductor area 205, which is a drain

through the FN (Fowler Nordheim) tunnel via the tunnel insulating film to lower the threshold value (V_{th}).

To erase data, electrons are charged in the floating gate electrodes 203 to increase the threshold value (V_{th}). In other words, a positive voltage of about 9V is applied to the control gate electrodes 7. Then, a negative voltage of about 9V is applied to the source and the P type well area 5 to charge electrons from an inverse layer formed in a channel area into the floating gate electrodes through the FN tunnel via the tunnel insulating film. Thus, the threshold value is increased.

The N channel MISFET Qn3 and the P channel MISFET Qp2 are used for a circuit for writing and erasing data in and from the flash memory.

With the semiconductor integrated circuitry, even when a flash memory is included in the circuitry, the first and second side wall spacers 14 and 15 are formed to divide the memory cell area finely, so that the LDD can be optimized for the peripheral circuit areas MISFET Qn1, Qn2, Qn3, Qp1, and Qp2. The fine division and performance of the semiconductor integrated circuitry can thus be improved.

Next, a manufacturing method for the semiconductor integrated circuitry in this fourth embodiment will be explained with reference to Figs.38 to 46. Figs.38 to 46 are cross sectional or top views indicating a manufacturing

method for the semiconductor integrated circuitry in this fourth embodiment in order of the processes.

At first, just like the first embodiment, the field insulating film 2; the N type semiconductor area 3; the N type well area 4; and the P type well area 5 are formed. Fig.38 is a top view of a flash memory areas after the field insulating film 2 is formed.

Next, as shown in Figs.39 and 40, a gate insulating film 201 is formed with a thermal oxidation method. Then, the film 201 except for the selecting MISFET Qsf, the N channel MISFET Qn3, and the P channel MISFET Qp2 is removed. Then, a tunnel insulating film 202 is formed with a thermal oxidation method. Since the tunnel insulating film 202 is formed after the gate insulating film 201 is removed such way, the tunnel insulating film 202 which is thinner than the gate insulating film 201 can be formed easily.

Thereafter, the flash memory floating gate electrodes 203, as well as electric conductors 206 used as the floating gate electrodes 203 of the selecting MISFET Qsf, the N channel MISFET Qn3, and the P channel MISFET Qp2 are formed. The electric conductors 206 are formed with a silicon film in which impurities such as phosphorus are implanted to lower the resistance. Thereafter, the silicon film masked with photo resist is patterned.

As shown in Fig.41, the floating gate electrodes 203 of the flash memory and an interlaminar insulating film 204 is formed between control electrodes 7. The interlaminar insulating film 204 is formed with a multi-layer film formed by laminating a silicon oxide film and a silicon nitride film sequentially. Then, the interlaminar insulating film 204 is selectively removed from the areas where the DRAM memory cell selecting MISFET Qs, the N channel MISFET Qn1, the N channel MISFET Qn2, and the P channel MISFET Qp1 are formed. Then, the silicon nitride film on the interlaminar insulating film 204 is used as an oxidation resistance mask to form a gate insulating film 6 just like in the first embodiment.

Next, as shown in Figs.42 and 43, the control gate electrodes 7 and the silicon nitride film 8 on the electrodes 7 are formed, then the film 8 is patterned using photo resist as a mask. The floating gate electrodes 203 of the flash memory and the control gate electrodes 7 are thus formed.

Hereafter, the processes are almost the same as those shown in Fig.10 in the first embodiment. In other words, as shown in Fig.44, the first and second side wall spacers 14 and 15 are formed in the DRAM memory cell area, and at the same time, they are formed in the flash memory cell area in the same way. The number of processes can thus be reduced.

Next, just like in the first embodiment, an insulating film 18 is formed, then connecting holes 21 are formed as shown in Fig.45.

Next, an insulating film 23 is formed, then connecting holes 30 are formed as shown in Fig.46.

The connecting holes 21 and 30, just like the connecting holes 19 and 21 in the first embodiment, are formed in a self-matching manner with respect to the first side wall spacers 14 composed of silicon nitride, so the interval t_3 between word lines WL (gate electrodes 7) in the second direction, the interval t_3 between word lines WL (gate electrodes 7) and block selecting lines tWL1 and tWL2, and the interval t_3 between block selecting lines tWL1 and tWL2 can be reduced finely in the second direction.

In addition, since the margin of alignment in the second direction can be reduced, the interval between elements in the second direction can be reduced finely. In other words, the interval between memory cells in the second direction can be reduced significantly, enabling the semiconductor integrated circuitry of the present invention to be integrated much more finely.

Next, the first wiring 32 is formed just like in the first embodiment. Consequently, DRAM memory cell bit lines BL and flash memory source lines SL can be formed in the same process, so the process can be shortened and simplified.

According to the method for manufacturing the semiconductor integrated circuitry in the fourth embodiment, the circuitry can be manufactured just like the semiconductor integrated circuitry provided with a flash memory in the first embodiment, and the memory cell array can be integrated very finely in the flash memory. In addition, the thickness of the gate insulating film can be varied according to the MISFET requirement.

Needless to say, the silicon nitride film 104 or the silicide layer 105 described in the second and third embodiments may be included in the method for manufacturing the semiconductor integrated circuitry in this fourth embodiment. In this fourth embodiment, needless to say, the semiconductor integrated circuitry is provided with both DRAM and flash memory, but this invention can also apply to a semiconductor integrated circuitry provided only with a flash memory.

(5th Embodiment)

Fig.47 is a cross sectional view of the major portion of a semiconductor integrated circuitry in another embodiment of the present invention.

The semiconductor integrated circuitry in this fifth embodiment is the same as that in the first embodiment except for that a silicon nitride film (the first side wall spacer) 207 is formed instead of the first side wall spacers 14.

Other configuration items are completely the same as those in the first embodiment, thus explanation for them will be omitted here. In the semiconductor integrated circuitry in this fifth embodiment, a silicon nitride film (the first side wall spacers) 207 of t1 in thickness is provided, so the integration degree of the memory cell area can be improved and the MISFET LDD structure other than the memory cell area can be optimized due to the second side wall spacers 15 to improve the performance of the semiconductor integrated circuitry just like in the first embodiment.

In the method for manufacturing the semiconductor integrated circuitry in this fifth embodiment, the process for forming the first side wall spacers 14 shown in Fig.12 in the first embodiment is replaced with a process for depositing a silicon nitride film 207 all over the semiconductor substrate 1. Consequently, the isotropic etching and other processes are omitted to simplify the manufacturing method significantly. In the processes for opening the connecting holes 19 and 21, however, the second stage etching is needed as described in the second embodiment. The number of processes is thus increased, but the semiconductor substrate 1 exposed at the bottoms of the connecting holes 19 and 21 can be prevented from over-etching, so that the contact reliability is improved.

The embodiments of the present invention are as described in detail above, but the present invention is not limited only to those embodiments. Needless to say, they can be varied as long as the substance of the present invention is not overstepped.

For example, in the first to fifth embodiments, it is a complementary MISFET is used to form peripheral or logic circuits, but only an N channel MISFET or P channel MISFET may be used to form peripheral circuits.

In addition, in the first to fifth embodiments, the thickness of the gate insulating film of the DRAM memory cell area selecting MISFET Qs is equal to those of the gate insulating films of the N channel MISFET Qn1, Qn2, and the P channel MISFET Qp1, but those insulating films may differ in thickness from each another. Especially, when the gate insulating films of the N channel MISFET Qn1, Qn2, and the P channel MISFET Qp1 is thinned than the selecting MISFET Qs, the N channel MISFET Qn1, Qn2, the P channel MISFET Qp1 can further be converted to shorter channels. The performance of the semiconductor integrated circuitry can thus be furthermore improved. In the case of the manufacturing method of the gate insulating film in such a case, it is possible to use the same method as that described in the fourth embodiment to form the gate insulating films

of the flash memory area and the DRAM area in different processes separately.

In addition, although a DRAM or a flash memory that is a nonvolatile memory is used as the memory cells in the first to fifth embodiments, an SRAM (Static RAM), a masked ROM, etc. may be used instead of those; for example, a memory structure that a side wall spacer is put between word lines to connect each electric conductor to the source or the drain area of the MISFET in a self-matching manner may be adopted as the memory cell structure.

(6th Embodiment)

Fig.50(a) is a cross sectional view of the memory cell area of the DRAM in the first embodiment of the present invention. Fig.50(b) is a cross section view of the peripheral circuit area. Fig.51 is a top view of the DRAM memory cell area in this sixth embodiment. Fig.52 is a cross sectional view of the DRAM memory cell area in this sixth embodiment. Fig.52(a) is a cross sectional view of the IIIa-IIIa line shown in Fig.51. Fig.52(b) is a cross sectional view of the IIIb-IIIb line shown in Fig.51. In Fig.51, some members are hatched or shown with broken lines for easier looking. The Ia-Ia line in Fig.51 indicates a cut-off portion of the cross sectional view shown in Fig.50(a).

In the DRAM memory cell area in the sixth embodiment, a memory cell selecting MISFET Q_t is formed and a charge storage capacity element and bit lines BL connected to the selecting MISFET Q_t are formed on the main surface of the semiconductor substrate 301.

In addition, in the DRAM peripheral circuit area is formed an n-type MISFET Q_n composing peripheral circuits. However, a p-type MISFET (not illustrated) is formed in a peripheral circuit, and the n-type MISFET Q_n and the p-type MISFET may be combined to form a CMISFET. In addition to the n-type MISFET Q_n , a high withstand voltage n-type MISFET (not illustrated) may be formed.

The semiconductor substrate 301 is composed of, for example, p-type silicon (Si) single crystal and on the main surface is formed a shallow groove 302a. In addition, in the shallow groove 302a is embedded an element isolating insulating film 302b composed of, for example, silicon dioxide (SiO_2) to form a shallow groove element isolating area.

On the semiconductor substrate 301 is also formed a p-type well 303. In the p-type well 303 is included, for example, boron, which is a p-type impurity. Under the p-type well 303 in the area where a memory cell selecting MISFET Q_t is formed is formed a deep well 303b. In the deep well 303b is implanted phosphorus, which is an n-type impurity,

so that the selecting MISFET Q_t is insulated from the substrate potential to improve the noise resistance of the circuitry.

When a p-type MISFET is formed, an n-type well (not illustrated) into which, for example, phosphorus is implanted is formed in the area where the p-type MISFET is formed. In addition, in the p-type well 303 and in the n-type well, if it exists, may be formed a MISFET threshold value control layer.

The memory cell selecting MISFET Q_t is formed in an active area surrounded by the element isolating insulating film 302b. In an active area are formed 2 selecting MISFETs Q_t . Each selecting MISFET Q_t has gate electrodes 305 composed of a polycrystal silicon film 305a and a tungsten silicide (W_{Si_2}) film 305b formed on the semiconductor substrate 301 via the gate insulating film 304 formed in the active area of the p-type well 303, and a pair of n-type semiconductor areas 306a and 306b formed on the p-type wells 303 on both sides of gate electrodes 305 so as to be separated from each other.

Each gate electrode functions as a DRAM word line WL. Both n-type semiconductor areas 306a and 306b are implanted an n-type impurity, but the impurity may be any of phosphorus and boron (As). In order to improve the withstand voltage between channels of the selecting MISFET Q_t to improve the

refreshing characteristics of the DRAM, however, phosphorus should preferably be implanted.

The n-type semiconductor area 306a is shared by two selecting MISFETs Q_t . And, a channel area of the selecting MISFET Q_t is formed between the n-type semiconductor areas 306a and 306b. The gate insulating film 304 is composed of, for example, SiO_2 . The film 304 may be thicker than the gate insulating film 304 of the n-type MISFET Q_n of the peripheral circuit area to be described later so that the dielectric strength of the selecting MISFET Q_t is improved. In such a case, the dielectric strength of the selecting MISFET Q_t is improved so that the refreshing characteristics of the DRAM is improved.

On top of gate electrodes (word lines WL) is formed a cap insulating film 307b composed of, for example, silicon nitride via an insulating film 307a composed of, for example, SiO_2 . Needless to say. The cap insulating film 307b functions as a blocking film when in opening of the connecting holes 311a and 311b in a process to be explained later in a self-matching matter with respect to the gate electrodes 305. The cap insulating film 307a prevents connecting members such as plugs from being short-circuited with gate electrodes 305.

The surface of the cap insulating film 307b, the side surfaces of each gate electrode 305, and the main surface

of the semiconductor substrate 301 except for the bottoms of the connecting holes 311a and 311b are covered respectively by an insulating film for self-matching treatment 309 composed of, for example, a silicon nitride film. The insulating film 309 for self-matching treatment functions as an etching stopper when the connecting holes 311a and 311b are opened in a self-matching manner with respect to the word lines, as well as it can prevent the semiconductor substrate 301, especially the element isolating insulating film 302b, from over-etching when the connecting holes 311a and 311b are opened.

At the phase boundary between the side surfaces of each gate electrodes 305 and the insulating film 309 for self-matching treatment may be formed an insulating film (not illustrated) composed of, for example, Needless to say. Such an insulating film and the insulating film 307a are provided to prevent a film forming apparatus from being contaminated with metal that composes the WSi film 305b and reduces the thermal stress to the cap insulating film 307b and the insulating film 309 for self-matching treatment when the cap insulating film 307b and the insulating film 309 for self-matching treatment are formed.

The insulating film 309 for self-matching treatment is covered by an interlaminar insulating film 310a composed of, for example, SOG (Spin On Glass). The interlaminar

insulating film 310a may be BPSG (Boron Phosphor Silicate Glass), but it should be a silicon oxide film that can secure a proper etching selection ratio for silicon nitride films. And, in the interlaminar insulating film 310a are formed connecting holes 311a from which the n-type semiconductor area 306a formed as an upper layer of the semiconductor substrate 301 is exposed and connecting holes 311b from which the n-type semiconductor area 306b formed as an upper layer of the semiconductor substrate 301 is exposed.

The cap insulating film 307b and the insulating film 309 for self-matching treatment can function as an etching stopper respectively as described above when the connecting holes 311a and 311b are opened in a self-matching manner. In addition, since the insulating film 309 for self-matching treatment is formed and the connecting holes 311a and 311b are opened in two-stage etching (the first etching process conditioned to make it easy to etch the interlaminar insulating film 310a (etching depth and etching speed; larger) and not easy to etch the insulating film 309 for self-matching treatment (etching depth and etching speed; small) and the second etching process conditioned to make it easy to etch the insulating film 309 for self-matching treatment and not easy to etch the element isolating insulating film 302b), the element isolating insulating film 302b formed up to the bottoms of the connecting holes

311a and 311b is prevented from over-etching even when the bottoms of the connecting holes 311a and 311b are off the active area of the semiconductor substrate 301 and overlap part of the element isolating insulating film 302b as shown in Figs.52(a) and (b). Thus, the bottoms of the connecting holes 311a and 311b do not reach the deep area of the element isolating insulating film 302b. In other words, even when the element isolating insulating film 302b is etched excessively, the etching arises no problem from the process. For example, etching can be controlled equally to or under the thickness of the insulating film 309 for self-matching treatment.

In each connecting hole 311b is formed a plug 314 composed of polycrystal silicon in which, for example, phosphorus is implanted at a high density. At the bottom of the plug 314 is formed an element isolating insulating film 302b even in an over-etched area. The etching depth is controlled to an extent to suppress problems in the process as described above. Thus, the performance of the DRAM refreshing characteristics will not be affected by the etching depth at all.

On both the interlaminar insulating film 310a and on the plug 314 is formed an interlaminar insulating film 310b. The interlaminar insulating film 310b may be a silicon oxide

film deposited with the thermal CVD method, for example, using TEOS (tetraethoxysilane).

On the interlaminar insulating film 310b are formed bit lines BL. The bit line BL is composed of a polycrystal silicon film 312 and a WSi_2 film 313 and connected electrically to the n-type semiconductor area 306a via connecting holes 311a. At the bottom of the polycrystal silicon film 312 is formed an element isolating insulating film 302b even in an over-etched area just like the plug 314, but the etching depth is controlled to an extent to suppress problems as described above. Thus, the DRAM performance is not affected by the etching depth at all.

This bit lines BL are covered by an interlaminar insulating film 310c composed of a silicon oxide film deposited with the thermal CVD method, for example, using TEOS. Furthermore, on the interlaminar insulating film 310c is formed an interlaminar insulating film 310d and polished and flattened with the CMP method. The interlaminar insulating film 310d is formed with the CMP method by polishing a silicon oxide film deposited with the plasma CVD method, for example, using TEOS. The interlaminar insulating film 310d may be formed using SOG or BPSG with the etch-back method, etc.

On the interlaminar insulating film 310d is formed an the interlaminar insulating film 310e composed, for

example, a silicon nitride film. The interlaminar insulating film 310e is used as a blocking film when a crown-like storage capacity SN to be explained later is formed.

On the interlaminar insulating film 310d is formed a storage capacity SN which is like a cylindrical crown in shape. The storage capacity SN is composed of capacitor electrodes 320a composed of the first electrodes 320a connected to the n-type semiconductor area 306b via connecting holes 311c and the second electrodes 320b provided vertically to the semiconductor substrate 301; a capacitor insulating film 321; and plate electrodes 322 connected to a specified wiring electrically. The first and second electrodes 320a and 320b may be a polycrystal film in which, for example, phosphorus is implanted at a high density. The capacitor insulating film 321 may be a laminated film formed by depositing Needless to say on a silicon nitride film, but it may also be a high permittivity thin film such as tantalum oxide. The plate electrodes 322 may be a polycrystal silicon film in which, for example, phosphorus is implanted at a high density, but it may also be a metallic compound such as tungsten silicide.

Under the first electrodes 320a are formed side walls 320d composed of a polycrystal silicon film 320c and a polycrystal silicon. The walls function as part of the

capacitor electrodes 320. The polycrystal silicon film 320c and the side walls 320d also function as a hardware mask respectively for opening connecting holes 311c and decide the diameter of each connecting hole 311c to a fine one under the resolution of the photolithography.

On the other hand, the n-type MISFET Qn of the peripheral circuit area is formed in an active area surrounded by the element isolating insulating film 302b. The n-type MISFET is composed of gate electrodes 305 composed of a polycrystal silicon film 305a formed on the semiconductor substrate 301 via a gate insulating film 304 formed in an active area of the p-type well 303 and a WSi_2 film 305b; and a pair of n-type semiconductor areas 306c formed on both ends of the gate electrodes 305 so as to be separated from each other.

The gate electrodes 305 are formed together with the word lines WL. Each n-type semiconductor area 306c includes a low density n-type semiconductor area 306c-1 and a high density n-type semiconductor area 306c-2 (higher density than the low density n-type semiconductor area 306c-1) formed in a self-matching manner with respect to the second side walls 323b. In other words, the n-type semiconductor area 306c has a so-called LDD (Lightly Doped Drain) structure. And, between the high density n-type semiconductor area 306c-2 formed under the low density

n-type semiconductor area 306c-1 and the channel area is formed a p-type semiconductor area 306d that functions as a punched-through stopper. In the n-type semiconductor area 306c is implanted, for example, phosphorus or arsenic. However, in order to shorten the channel length of the n-type MISFET Qn to improve the performance, arsenic should be implanted. To form a high dielectric strength type MISFET, phosphorus should be implanted in the low density n-type semiconductor area 306c-1. Consequently, the dielectric strength between channels is improved.

The gate insulating film 304 is the same as that of the selecting MISFET Qt, so the explanation will be omitted here.

Just like the selecting MISFET Qt described above, a cap insulating film 307b is also formed on top of each gate electrode 305 via an insulating film 307a. Thus, the explanation will also be omitted here.

On both side surfaces of each gate electrode 305 are formed the first side walls 323a and outside the side walls 323a are formed the second side walls 323b.

The first side walls 323a are formed by anisotropic etching performed for the insulating film 309 for self-matching treatment to be described later. For example, the first side walls 323a are composed of a silicon nitride film. This first side walls 323a can also be used as side walls

for opening connecting holes in a self-matching manner with respect to gate electrodes 305 when the connecting holes are formed in the peripheral circuit area.

The second side walls 323b are composed of, for example, a silicon oxide film and they are used as a mask for ion-implanting of impurities to form a high density n-type semiconductor area 306c-2, so that the high density n-type semiconductor area 306c-2 is formed in a self-matching manner. By controlling the thickness of this second side wall film 323b, the LDD structure can be optimized to improve the performance of the n-type MISFET Qn.

As described above, the insulating film 309 for self-matching treatment on the semiconductor substrate 301 is removed by anisotropic etching and the insulating film for self-matching treatment 309 is not provided in the peripheral circuit area. Thus, it is no need to open the connecting holes in the peripheral circuit area in two stages, permitting the holes to be opened easily. When the gate electrodes 305 in the peripheral circuit area are connected to a wiring in the upper layer, the connecting holes can be opened easily. Why it is no need to provide the insulating film for self-matching treatment 309 in the peripheral circuit area is as follows; the MISFET formed in the peripheral circuit area does not require a high

integration so much and a rather large margin can be secured for the disposing pitches of elements, as well as a margin can be secured for forming active areas. Thus, failures in opening the connecting holes can be taken into consideration when in designing. When a high integration is required for the peripheral circuit area, therefore, the etching stopper 104 described in the second embodiment may be formed selectively in the peripheral circuit area after the second side walls 323b are formed, of course.

When it is needed to form a p-type MISFET, it can be formed in the same configuration as that of the n-type MISFET Qn just by reversing the electrical conductivity.

At the phase boundary between side surfaces of each gate electrode 305 and the first side walls 323a may be formed an insulating film (not illustrated) composed of, for example, Needless to say. Such an insulating film and the insulating film 307a are provided to prevent a film forming apparatus from being contaminated with the metal used for forming the WSi_2 film 305b and to reduce the thermal stress onto the cap insulating film 307b and the first side walls 323a when the cap insulating film 307b and the first side walls 323a are formed.

The n-type MISFET Qn is covered by an interlaminar insulating film 310f composed of a silicon oxide film deposited with the CVD method using, for example, TEOS. In

addition, on the interlaminar insulating film 310f is formed an interlaminar insulating film 310g flattened with, for example, the CMP method. The interlaminar insulating film 310g may be a silicon oxide film deposited with the plasma CVD method using, for example, TEOS. The interlaminar insulating film 310g may be formed with SOG or BSPG and flattened with the etch-back method.

On the interlaminar insulating film 310g is formed the interlaminar insulating film 310b described above and on the interlaminar insulating film 310b is formed the bit lines BL described above. The bit lines BL are covered by an interlaminar insulating film 310c described above and on the interlaminar insulating film 310c is formed the interlaminar insulating film 310d described above.

Both on the interlaminar insulating film 310d and on the plate electrodes 322 is formed an interlaminar insulating film 324 composed of, for example, BPSG. The interlaminar insulating film 324 is flattened by the reflowing method.

On the interlaminar insulating film 324 in the peripheral circuit area is formed the first wiring layer 325. The first wiring layer 325 is connected to the high density n-type semiconductor area 306c-2 of the n-type MISFET Qn via connecting holes 326. The first wiring layer 325 may be a laminated film composed of a metallic film such

as titan nitride, titan, or aluminum. The laminated film may be deposited with, for example, the sputtering method. A plug composed of, for example, tungsten may be formed in each connecting hole 326. The tungsten plug may be formed with the tungsten CVD method. At this time, titan nitride should be used for forming a bonding layer beforehand in each connecting hole.

The first wiring layer 325 is covered by an interlaminar insulating film 327 and on the interlaminar insulating film 327 is formed the second wiring layer 328. The second wiring layer 328 is connected to the first wiring layer 325 via connecting holes 329. The interlaminar insulating film 327 may be a silicon oxide film composed of, for example, a silicon oxide film and SOG, but it should be a laminated film formed by sandwiching the silicon oxide film between silicon oxide films deposited with the plasma CVD method. The second wiring layer 328 should take the same configuration as that of the first wiring layer 325.

The second wiring layer 328 is covered by an interlaminar insulating film 330 and on the interlaminar insulating film 330 is formed the third wiring layer 331. The third wiring layer 331 is connected to the second wiring layer 328 via connecting holes 332. The interlaminar insulating film 330 may take the same configuration as that of the interlaminar insulating film 327 and the third wiring

layer 331 may take the same configuration as that of the first wiring layer 325.

The third wiring layer 331 is covered by a passivation film 333. The passivation film 333 may be a laminated film composed of a silicon oxide film and a silicon nitride film.

Next, how to manufacture the DRAM will be described with reference to Figs.53 to 79.

Figs.53 to 79 are cross sectional views of a manufacturing method of the DRAM in this sixth embodiment in order of the processes. Figs.53 to 79 except for Figs.63, 65, 67, 69, and 71 indicate a portion equivalent to the cross sectional view of the Ia-Ia line shown in Fig.51 in each (a) and in each (b) respectively. They indicate a cross sectional view of the peripheral circuit area. In Figs.63, 65, 67, 69, and 71 (a) indicate a portion equivalent to a cross sectional view of the IIIa-IIIa line, and (b) indicates a portion equivalent to a cross sectional view of the IIIb-IIIb line, shown in Fig.51 respectively.

At first, as shown in Fig.53, a shallow groove element isolating area is formed in each specified area on the semiconductor substrate 301. In the shallow groove element isolating area is formed a silicon oxide film and a silicon nitride film (both not illustrated) sequentially on the main surface of the semiconductor substrate 301. Then, both silicon oxide film and silicon nitride film are removed by

photo resist from the shallow groove 302a, then a groove of 0.3 to 0.4 μm in depth is formed in the semiconductor substrate 301. Next, a silicon thermal-oxide film (not illustrated) is formed on surfaces of both sides and bottom surface of the groove using the silicon nitride film as an oxidation mask. Then, a silicon oxide film is deposited all over the semiconductor substrate 301 with the CVD (Chemical Vapor Deposition) method. The silicon oxide film is removed from the areas except for the shallow groove 302a with the CMP (Chemical Mechanical Polishing) method or the dry-etching method to embed the silicon oxide film in the shallow groove 302a selectively.

The element isolating insulating film 302b should be densified in an atmosphere of oxidation. Then, the silicon nitride film is removed with heated phosphoric acid to form an element isolating insulating film 302b. At this time, the element isolating insulating film 302b is a little etched with the heated phosphoric acid to be lowered in position than the active areas on the semiconductor substrate 301. Consequently, the gate electrodes 305 can be patterned more satisfactorily to improve the performance of the MISFET.

As shown in Fig.54, an n-type impurity, for example, phosphorus is ion-implanted in the memory cell array forming area on the semiconductor substrate 301 using photo resist

as a mask. Then, the photo resist is removed and a p-type impurity, for example, boron is ion-implanted in the memory cell array forming area and the n-type MISFET Q_n forming area on the semiconductor substrate 301 respectively. The photo resist is then removed and a heat distribution treatment is performed for the semiconductor substrate 301 to form a deep well 303b and a p-well 303. To form a p-type MISFET, for example, phosphorus is implanted in the area to form an n-well.

And, in order to optimize the impurity density in a channel area and obtain the threshold voltage of a desired memory cell selecting MISFET Q_t or an n-type MISFET Q_n, a p-type impurity, for example, boron can be ion-implanted in the main surface of the active area of the p-well 303.

As shown in Fig.55, a gate insulating film 304 is formed on the surface of the semiconductor substrate 301. This gate insulating film 304 is formed with the thermal oxidation method with a thickness of about 7nm. In addition, a polycrystal silicon film 305a formed by implanting phosphorus all over the semiconductor substrate 301 and a WSi₂ film 305b are deposited sequentially. The CVD method is used to form the polycrystal silicon film 305a and the WSi₂ film 305b. They are 40nm and 100nm in thickness respectively. Then, on the WSi₂ film 305b are deposited an insulating film 307a composed of a silicon oxide film and

a cap insulating film 307b composed of a silicon nitride sequentially. The CVD method is used to form the insulating film 307a and the cap insulating film 307b. The films 307a and 307b are 10nm and 160nm in thickness respectively.

As shown in Fig.56, the gate electrodes 305 of the selecting MISFET Q_t for the memory cells composed of a polycrystal silicon film 305a and a WSi_2 film 305b and the peripheral circuit MISFET Q_n are formed by etching a cap insulating film 307b, an insulating film 307a, a WSi_2 film 305b, a polycrystal silicon film 305a of an laminating film sequentially using photo resist as a mask.

Next, the photo resist is removed, then a thermal oxidation treatment is performed on the semiconductor substrate 301 to form a thin silicon oxide film on side surfaces of the polycrystal silicon film 305a composing of gate electrodes 305 and the WSi_2 film 305b.

As shown in Fig.57, a p-type impurity, for example, boron is ion-implanted in the main surface of the p-well in the area where an n-type MISFET Q_n of the peripheral circuit area is formed using the laminated film described above and photo resist as masks, then an n-type impurity, for example, arsenic is ion-implanted in the same main surface. Furthermore, after the photo resist is removed, an n-impurity, for example, phosphorus is ion-implanted in the main surface of the p-well 303 where a selecting MISFET Q_t

is formed, using the laminated film described above and photo resist as masks. Then, those impurities are expanded and distributed to form a low density n-type semiconductor area 306c-1 and a p-type semiconductor area 306d of the n-type MISFET Q_n and an n-type semiconductor areas 306a and 306b of the selecting MISFET Q_t. To form a high dielectric strength n-type MISFET, phosphorus is implanted in the area. To form a p-type MISFET, arsenic for a punched-through stopper and boron (BF₂) for a low density semiconductor area are implanted in the area. The low density n-type semiconductor area 306c-1 for the peripheral circuit MISFET Q_n and the n-type semiconductor areas 306a and 306b of the memory cell selecting MISFET Q_t are formed in a self-matching manner with respect to the gate electrodes.

As shown in Fig.58, a silicon nitride film 334 is deposited. The thickness of the silicon nitride film 334 can be, for example, 80nm. Then, an SOG film 335 is deposited, and the memory array area is masked with photo resist to etch the SOG film 335 and the silicon nitride film 334. The etching may be anisotropic etching such as RIE (Reactive Ion Etching). Consequently, the SOG film 335 and the silicon nitride film 334 are removed from the peripheral circuit area to form an insulating film for self-matching treatment 309 and an interlaminar insulating film 310a in the memory array area. The interlaminar insulating film

310a is composed of SOG, so the film 310a can fill each recess and flatten the surfaces of the gate electrodes 305 and the cap insulating film 307b respectively. Furthermore, since anisotropic etching is performed, the first side walls 323a composed of a silicon nitride film are formed on side surfaces of the gate electrodes 305 of the n-type MISFET Qn and the cap insulating film 307b in the peripheral circuit area.

As shown in Fig.59, a TEOS silicon oxide film (not illustrated) is formed all over the surface of the semiconductor substrate 301, then the film is anisotropic-etched to form the second side walls 323b on side surfaces of the first side walls 323a. The second side walls 323b should be thicker (wider) than the first side walls 323a. The memory cell can thus be divided finely and the characteristics of the peripheral circuit MISFET is improved.

As shown in Fig.60, n-type impurities, for example, arsenic and phosphorus are ion-implanted in the peripheral circuit area where the n-type MISFET Qn is formed, using the gate electrodes 305, the cap insulating film 307b, the second side walls 323b, and photo resist as masks. Then, the photo resist is removed and the impurities are expanded and distributed to form a high density n-type semiconductor area 306c-2 of the n-type MISFET Qn. To form a p-type MISFET,

boron (BF_2) for a high density semiconductor area is implanted in the area. This high density n-type semiconductor area 306c-2 is formed in a self-matching manner with respect to the second side walls 323b.

As shown in Fig.61, a TEOS silicon oxide film is deposited to form an interlaminar insulating film 310f. In addition, a silicon oxide film is deposited with the plasma CVD method using TEOS, then the silicon oxide film is flattened with the CMP method (polishing) to form an interlaminar insulating film 310g. In the memory cell portion is deposited a TEOS silicon oxide film 310f and another silicon oxide film while the SOG film 335 is left as it is. The surface is flattened with the CMP method. Thereafter, in the memory cell portion are left the SOG film 335, the TEOS silicon oxide film 310f, and the polished silicon oxide film. This 3-layer insulating film is referred to as an interlaminar insulating film 310g.

Next, as shown in Figs.62 to 65, the interlaminar insulating film 310a is etched using photo resist as a mask to form connecting holes 311b. The connecting holes 311b are opened by etching performed in two stages.

At first, the first etching process is performed on conditions to make it easy to etch the silicon oxide film and not easy to etch the silicon nitride film. Such the etching is performed as an anisotropic plasma etching using

a mixed gas containing, for example, C_4F_8 and argon as material gases. In this first etching process, it is not easy to etch the silicon nitride film, so etching of the interlaminar insulating film 310a composed of a silicon oxide is advanced into the stage in which the insulating film for self-matching treatment 309 composed of a silicon nitride film is exposed. Figs. 62 and 63 indicate this state. In other words, the insulating film for self-matching treatment 309 functions as an etching stopper in the first etching process.

Next, the second etching process is performed on conditions to make it easy to etch the silicon nitride film. Such the etching is performed as an anisotropic plasma etching using a mixed gas containing CHF_3 , CF_4 and argon is used as material gases. In the second etching process, it is only needed to etch the thinner insulating film for self-matching treatment 309, since the thicker interlaminar insulating film 310a is already removed in the first etching process. In other words, it is possible to etch the insulating film for self-matching treatment 309 with an enough process margin by suppressing over-etching to the ground of the insulating film for self-matching treatment 309. This means that on conditions to make it easy to etch silicon nitride films, no selection ratio of silicon nitride films to silicon oxide films can be taken. Thus, both

silicon nitride and silicon oxide films are etched. As a result, as shown in Fig. 65, when the bottom of any connecting hole 311b overlaps the element isolating insulating film 302b, the insulating film 302b composed of a silicon oxide film is also etched. To be ideally, the etching should be a just etching that only the insulating film for self-matching treatment 309 is etched and the etching is ended just after the insulating film for self-matching treatment 309 is removed. It is generally difficult, however, to open connecting holes 311b in every area on the substrate and perform a just-etching because of problems such as etching speed distribution on the substrate, etc. Over-etching cannot thus be avoided to a certain extent. When the bottom of any connecting hole 311b goes over an active area and overlaps the element isolating insulating film 302b, therefore, the insulating film 302b might be over-etched. In this method, however, the insulating film for self-matching treatment 309 is as thin as 80nm and it is needed to etch only the insulating film for self-matching treatment 309, so the over-etching will be enough if the depth reaches 30 to 50% of the thickness of the insulating film for self-matching treatment 309 and at most the thickness of the insulating film for self-matching treatment 309. Over-etching for the element isolating insulating film 302b can thus be minimized and the refreshing characteristics of the

DRAM is improved significantly to improve the performance of the DRAM.

In the second etching process, the gate electrodes 305 are covered by both the insulating film for self-matching treatment 309 and the cap insulating film 307b as shown in Fig. 64, so the gate electrodes 305 are not exposed even when designed so that the connecting holes 311b overlap the gate electrodes 305. Connecting holes 311b can thus be opened in a self-matching manner. In other words, the insulating film for self-matching treatment 309 can function to open connecting holes 311b in a self-matching manner with respect to gate electrodes 305 and functions to suppress over-etching of the element isolating insulating film 302b.

In the two-stage etching method that uses the insulating film for self-matching treatment 309 such way, the degree of integration is improved and effective especially for a DRAM in which the interval between gate electrodes 305 is narrow. In other words, when side walls are formed on side surfaces of each gate electrode 305 for opening connecting holes in a self-matching manner with respect to the gate electrodes 305, if an attempt is made to form a stopper film to suppress over-etching of the element isolating insulating film 302b, each connecting hole 311b composing each space between gate electrodes 305 is filled or even when the space is not filled, the bottom

area of each connecting hole 311b is minimized. And, this makes it difficult to secure an enough connecting conductivity. In the case of the manufacturing method in the sixth embodiment, however, no side wall is formed for self-matching opening of connecting holes with respect to gate electrodes 305. Instead, the insulating film for self-matching treatment 309 is provided with a function for such a self-matching opening, so that a space can be secured enough between gate electrodes 305 and the connecting reliability is assured while the process margin for opening connecting holes 311b is kept properly.

Next, as shown in Figs.66 and 67, a plug 314 is formed in each connecting hole 311b. The plug 314 may be polycrystal silicon implanted with phosphorus. The plug 314 can be formed by depositing a polycrystal silicon film all over the surface of the semiconductor substrate 301, the etching-back the polycrystal silicon film. Since the bottom of the connecting hole 311b does not reach the depth of the element isolating insulating film 302b, the bottom of the plug 314 is formed in a shallow area even in an area where a connecting hole 311b overlaps on the insulating film 302b, so that the reliability of the DRAM is improved.

Next, as shown in Figs.68 and 69, an interlaminar insulating film 310b is formed composed of a TOES silicon oxide film all over the semiconductor substrate 301, then

connecting holes 311a are formed. The connecting holes 311a can be formed in a two-stage etching process just like the connecting holes 311b. And, just like connecting holes 311b, the plug is not formed in the depth of the element isolating insulating film 302b even in each connecting hole 311a.

Next, as shown in Figs. 70 and 71, a polycrystal silicon film 312 implanted with phosphorus and a WSi_2 film 313 are deposited sequentially with the CVD method, then patterned to form bit lines BL. The bit lines BL are connected to one n-type semiconductor area 306a of the memory cell selecting MISFET Qt. Just like the plug 314, the bottom of the polycrystal silicon film 312 is formed in the shallow area even in the area where the connecting holes 311a overlap the element isolating insulating film 302b. The reliability of the DRAM is thus improved.

As shown in Fig. 72, on the semiconductor substrate 301 is deposited an interlaminar insulating film 310c composed of a silicon oxide film and an interlaminar insulating film 310d with the CVD method, then the surface of the interlaminar insulating film 310d is flattened with, for example, the CMP method. On the semiconductor substrate 3-1 is formed an interlaminar insulating film 310e composed of a silicon nitride film.

As shown in Fig.73, a silicon oxide film 336 is deposited, then a polycrystal silicon film 320c is deposited, then patterned using photo resist as a mask. Furthermore, a polycrystal silicon film (not illustrated) is deposited and anisotropic-etched to form side walls 320d. Since side walls 320d are formed such way, holes can be formed with a smaller diameter than those of the polycrystal silicon film 320c patterned with the minimum resolution of lithography.

As shown in Fig.74, connecting holes 311c, masked by the polycrystal silicon film 320c and the side walls 320d, are opened.

Then, as shown in Fig.75, the first electrodes 320a implanted with phosphorus and a silicon oxide film 337 are deposited sequentially on the semiconductor substrate 301. Each of the first electrodes 320a is deposited in a connecting hole 311c and connected to a plug 314.

As shown in Fig.76, the silicon oxide film 337 masked by photo resist is etched, then the first electrodes 320a and the polycrystal silicon film 320c are etched sequentially. The treated first electrodes 320a and the polycrystal silicon film 320c are used as part of the storage capacity element for storing information in the memory cell area.

Next, the photo resist is removed, a polycrystal silicon film (not illustrated) is deposited as shown in Fig.77 on the semiconductor substrate 301 with the CVD method. Then, anisotropic etching is performed for the polycrystal silicon film to form the second electrodes 320b. Furthermore, the silicon oxide films 336 and 337 are removed by wet etching using, for example, an acid fluoride solution to form the first electrodes 320a, the second electrodes 320b, and the crown-like capacitor electrodes 320 composed of a polycrystal silicon film 320c and side walls 320d.

As shown in Fig.78, polycrystal silicon particles of about 40nm in diameter are grown on each capacitor electrode 320, then a silicon nitride film (not illustrated) is deposited on the semiconductor substrate 301 with the CVD method. An oxidation treatment is performed for the film to form a silicon oxide film on the surface of the silicon nitride film and form a capacitor insulating film 321 composed of a silicon oxide film and a silicon nitride film on the surfaces of the capacitor electrodes 320.

Thereafter, on the semiconductor substrate 301 is deposited a polycrystal silicon film (not illustrated) with the CVD method and this polycrystal silicon film is masked with photo resist and etched to form plate electrodes 322.

As shown in Fig.79, a BPSG film is deposited and annealed to form an interlaminar insulating film 324. Then,

the interlaminar insulating film 324 is masked with photo resist and etched to open connecting holes 326. When the holes 326 are opened, the first side walls 323a can be used to open the connecting holes 326 in a self-matching manner with respect to the gate electrodes 305 in the peripheral circuit area. Furthermore, titan, titan nitride, aluminum, and titan are deposited sequentially and patterned to form the first wiring layer 325. On inner surface of each connecting hole 326 may also be deposited titan to form a tungsten film with the CVD method, then etched back to form a tungsten plug. The sputtering method can be used for depositing titan nitride, aluminum, and titan.

Finally, a TEOS silicon oxide film is deposited with the plasma CVD method, then an SOG film is coated on the film and a TEOS silicon oxide film is deposited on the film with the plasma CVD method to form an interlaminar insulating film 327. Just like the first wiring layer, connecting holes 329, the second wiring layer 328, the interlaminar insulating film 330, connecting holes 332, and the third wiring layer 331 are formed. Then, a TEOS silicon oxide film and a silicon nitride film are deposited on the surface with the plasma CVD method to form a passivation film 333. Thus, the manufacturing of the DRAM shown in Fig.50 is almost finished.

According to the DRAM in this sixth embodiment, since the insulating film for self-matching treatment 309 is used to open the connecting holes 311a and 311b by two-stage etching, plugs 314 and bit lines BL can be formed in a self-matching manner with respect to gate electrodes 305, as well as the element isolating insulating film 302b is prevented from over-etching. The refreshing characteristics of the DRAM can thus be improved. In addition, no side wall is formed on the side surfaces of each gate electrode 305 in the memory cell area, this sixth embodiment can also cope with higher integration of the DRAM.

In addition, the insulating film for self-matching treatment 309 is provided with two functions for forming self-matching contacts with respect to the gate electrodes 305 and for preventing the element isolating insulating film 302b from over-etching, so it is no need to form a member for realizing each of the functions specially. The number of processes can be reduced, suppressing an increase of processes.

In this sixth embodiment, plugs 314 are used. However, no plug 314 is used and the capacitor electrodes 320 may be connected to the n-type semiconductor area 306b directly via connecting holes 311b. In this case, connecting holes 311b are formed deeply, the etching margin

becomes small and treatment of those holes becomes difficult. When the two-stage etching in this sixth embodiment is used, however, the etching margin is increased and it becomes possible to cope with opening of the connecting holes. In other words, when no plug 314 is used, the effect of the present invention becomes more clear.

Needless to say, the two-stage etching described above may also be performed as continuous processes.

In Fig.60, after a high density n-type semiconductor area 6c-2 of the n-type MISFET Qn is formed, the silicon nitride film 104 shown in the second embodiment is formed selectively in the peripheral circuit area, then the TEOS silicon oxide film shown in Fig.61 is deposited to form an interlaminar insulating film 310f. The subsequent processes can also be performed.

After a high density n-type semiconductor area 6c-2 of the n-type MISFET Qn is formed as shown in Fig.60, the third embodiment can be performed.

In other words, after a high density n-type semiconductor area 6c-2 of the n-type MISFET Qn is formed, high melting-point metals such as molybdenum and cobalt are deposited in the peripheral circuit area to form a silicide layer on the surface of the high density n-type semiconductor area 6c-2 of the n-type MISFET Qn for peripheral circuits. Thereafter, non-reacted high

melting-point metals are removed and a TEOS silicon film shown in Fig.61 is deposited to form an interlaminar insulating film 310f. The subsequent processes can also be performed.

The above examples can also be applied in the case of the seventh and eighth embodiments.

(7th Embodiment)

Figs.80 and 81 are cross sectional views indicating a manufacturing method of the DRAM in another embodiment of the present invention.

The method for manufacturing the DRAM in this seventh embodiment are the same as that in the sixth embodiment up to the forming of the gate electrodes 305 and the cap insulating film 307b (Fig.57). The explanation will thus be omitted here, avoiding redundant explanation.

The method for manufacturing the DRAM in this seventh embodiment indicates a case that the gate electrodes 305 in the memory array area are disposed finely and the insulating film 309 for self-matching treatment is removed without using any mask from the peripheral circuit area.

After the gate electrodes 305 and the cap insulating film 307b are formed, a silicon nitride film to be used as an insulating film for self-matching treatment 309 is deposited as shown in Fig.80, then a silicon oxide film 339 is deposited on the film 309. In the memory array area, since

the gate electrodes 305 are disposed finely as shown in Fig.80(a), the recesses of the silicon oxide film 339 are filled completely, so that the surface is flattened. On the other hand, the gate electrodes 305 are formed more thinly in the peripheral circuit area as shown in Fig.80(b) than in the memory array area, so unevenness of those electrodes 305 appear almost faithfully on the surface of the film 339.

As shown in Fig.81, the silicon nitride film 309 and the silicon oxide film 339 are etched by anisotropic etching. This etching is performed on conditions to make it easy to etch silicon nitride films using, for example, a mixed gas of CHF_3 , CF_4 and argon. In the memory array area, since the surface of the silicon oxide film 339 is flat, only the silicon nitride film 309 is etched both on the flat surface of the silicon oxide film 339 and on the surface of the silicon nitride film 307b. Consequently, in the memory array area, the silicon nitride film 309 is left on the main surface of the semiconductor substrate 301 and the film 309 functions as an insulating film 309 for self-matching treatment. On the other hand, in the peripheral circuit area, the silicon nitride film 309 and the silicon oxide film 330 on the main surface of the semiconductor substrate 301 and the surface of the cap insulating film 307b except for the side surfaces of the gate electrodes 305 are etched. The silicon nitride film 309 and the silicon oxide film 330 are

left only as the first side walls 323a and the second side walls 323b of the gate electrodes 305.

According to the method for manufacturing the DRAM in this seventh embodiment, the insulating film for self-matching treatment 309 is formed in the memory array area and at the same time the first and second side walls 323a and 323b can be formed on the side surfaces of each gate electrode in the peripheral circuit area even without using photo masks, etc. Thus, the process can be simplified.

Hereafter, the processes are the same as those shown in Fig.60 in the sixth embodiment and after. The explanation will thus be omitted here, avoiding redundant explanation.
(8th Embodiment)

Figs.82 to 84 are cross sectional views indicating a manufacturing method of the DRAM in another embodiment of the present invention.

The manufacturing method in this eighth embodiment is the same as that in the sixth embodiment up to forming of the gate electrodes 305 and the cap insulating film 307 (Fig.57). The explanation for the same processes will thus be omitted here.

The manufacturing method in this eighth embodiment indicates a case that the gate electrodes 305 are disposed thinly in the memory array area and a mask is used to remove

the insulating film for self-matching treatment 309 in the peripheral circuit area.

After the gate electrodes 305 and the cap insulating film 307b are formed, a silicon nitride film to be used as an insulating film for self-matching treatment 309 is deposited to form a photo mask 340 in the memory array area.

Then, as shown in Fig.83, the insulating film for self-matching treatment 309 masked by the photo mask 340 is etched by anisotropic etching. This etching is performed on conditions to make it easy to etch the silicon nitride film using a mixed gas of, for example, CHF_3 , CF_4 , and argon. Consequently, the first side walls 323a are formed on side surfaces of each gate electrode 305 in the peripheral circuit area.

Furthermore, the photo mask 340 is removed, then a silicon oxide film 341 is deposited all over the surface of the semiconductor substrate 301.

As shown in Fig.84, the silicon oxide film 341 may be etched by anisotropic etching on conditions to make it difficult to etch silicon nitride films using, for example, a mixed gas of C_4F_8 and argon. Consequently, the second side walls 323b are formed on side surfaces of the gate electrodes 305 not only in the peripheral circuit area, but also in the memory cell array area.

According to the manufacturing method, the insulating film for self-matching treatment 309 is removed from the peripheral circuit area and the second side walls 323b can be formed on side surfaces of the gate electrodes 305. And, as described in the sixth embodiment, the thickness of the second side walls 323b can be adjusted to optimize the LDD structure.

The subsequent processes are the same as those shown in Fig.60 in the sixth embodiment and after, thus, explanation for those processes will be omitted here, avoiding redundant explanation.

The invention of the present inventor is as described above with reference to embodiments, but the present invention is not limited only to those embodiments. Needless to say, the embodiments may be varied freely as long as the substance of the present invention is not overstepped.

For example, although the element isolating area is provided in the shallow groove element isolating area in the sixth to eighth embodiments, the element isolating area may be composed of a thick field insulating film formed with the LOCOS method. In the present invention, since the shallow groove of the shallow groove element isolating area is formed more sharply than a bird's beak of the field insulating film, the present invention, when applied to a

shallow element isolating area that will be affected significantly even by a slight deviation from connecting holes, can obtain more remarkable effects. And, the same effect can also be obtained when the present invention is applied to an element isolating area formed with a field insulating film, of course.

The present invention also includes the following inventions.

(1) The semiconductor integrated circuitry of the present invention comprises a semiconductor substrate having an element isolating area and active areas surrounded by the element isolating area respectively on its main surface; a gate insulating film formed on the main surface; gate electrodes formed on the gate insulating film; a cap insulating film formed on the gate electrodes; an MISFET including a semiconductor area formed in both active areas on both sides of the gate electrodes; and an interlaminar insulating film insulating the MISFET and a conductive member formed in the upper layer of the MISFET, wherein an insulating film for self-matching treatment having an etching selection ratio for interlaminar insulating films is formed on the main surface of the semiconductor substrate including the top and side surfaces of the cap insulating film in all or part of the MISFET areas, as well as side surfaces of the gate electrodes, and the insulating film for

self-matching treatment is used to open the holes for connecting the conductive member to the semiconductor area in a self-matching manner with respect to the gate electrodes and to prevent the bottom of each connecting hole going into the element isolating area off the active area from over-etching.

According to the semiconductor integrated circuitry, since the insulating film for self-matching treatment is formed on side surfaces of the gate electrodes and on the main surface of the semiconductor substrate so as to be used as side walls of the gate electrodes to open the connecting holes in a self-matching manner and as a stopper film to prevent the element isolating area on the semiconductor substrate from over-etching, the gate electrodes can be disposed at fine intervals to improve the integration degree of the circuitry and especially to secure an enough connecting area at the bottom of each connecting hole even in every MISFET in the highly integrated DRAM memory mat area. As a result, even in a highly integrated semiconductor integrated circuitry, self-matching contact technologies and over-etching preventive technologies for the element isolating area can be used together to improve the integration degree and reliability of the semiconductor integrated circuitry.

(2) In the semiconductor integrated circuitry, the insulating film for self-matching treatment can be formed in adjacent to the side surfaces of the cap insulating film and the gate electrodes or via a thinner film than the insulating film for self-matching treatment. In addition, it is no need to form any side wall among the insulating film for self-matching treatment, the side surfaces of the cap insulating film, and the gate electrodes. This is because the insulating film for self-matching treatment can be used as side walls of each gate electrode. Consequently, the margin for opening each connecting hole can be increased and the process can be simplified to minimize an increase of processes.

(3) In addition, the insulating film for self-matching treatment may be a silicon nitride film and each interlaminar insulating film may be a silicon oxide film. And, since the silicon nitride film and the silicon oxide film used frequently in the manufacturing processes of conventional semiconductor integrated circuitries such way are used and the solid state properties of those films are well known. It is thus possible to design processes and select conditions using existing established manufacturing processes to start up production processes speedily.

(4) In addition, the element isolating area can be formed in the shallow groove element isolating area

structured to isolate each element from others in a shallow groove or in the element isolating area having a thick field insulating film formed with the selective oxidation method. Especially, in the case of the shallow groove element isolating area, the area is formed to rise sharply at a boundary between an active area and the element isolating area, so an over-etched portion formed in the element isolating area due to a slight deviation when in forming of connecting holes is deepened more than the thick field insulating film, so that the over-etching problem caused by such a deviation described above arises remarkably. When the present invention applies to a semiconductor integrated circuitry having a shallow groove element isolating area to prevent the element isolating area from over-etching, therefore, the effect appears more remarkably.

(5) In addition, the semiconductor integrated circuitry of the present invention includes a DRAM memory mat area and the insulating film for self-matching treatment is formed only in the DRAM memory mat area. In other words, the insulating film for self-matching treatment is formed only in the memory mat area that must be highly integrated to assure high integration and high reliability thereof. And, the insulating film for self-matching treatment is not formed in other areas including the peripheral circuit area, which are not needed to be highly integrated so much.

According to the semiconductor integrated circuitry, since a high integration and a high reliability are assured in the memory mat area, as well as no insulation film for self-matching treatment is formed in other areas including the peripheral circuit area, the process for forming holes connecting a wiring layer formed together with the gate electrodes to the upper layer of the wiring layer or the process for forming holes connecting the MISFET semiconductor area in the peripheral circuit area to the upper layer of the semiconductor area can be simplified. In other words, when an insulating film for self-matching treatment is also formed in the peripheral circuit area, a two-stage etching process is needed for etching the insulating film for self-matching treatment when the holes connecting the semiconductor area to the upper layer, as well as the cap insulating film formed on top of the gate electrodes and the insulating film for self-matching treatment must also be etched when the holes connecting the wiring layer formed together with the gate electrodes to the upper layer are formed, resulting in the complicated process. In the present invention, however, since no insulating film for self-matching treatment is formed in the peripheral circuit area, the process is not complicated.

(6) In addition, the semiconductor integrated circuitry of the present invention includes a DRAM memory

mat area, and on side surfaces of each MISFET gate electrode formed in areas other than the memory mat area are formed side walls via an insulating film deposited in the same process as that of the insulating film for self-matching treatment or in contact with the side surfaces of the insulation film.

According to the semiconductor integrated circuitry, the LDD (Lightly Doped Drain) of each MISFET formed in areas other than the memory mat area can be optimized to shorten the channel of the MISFET in areas other than the memory mat area and improve the performance.

The method for manufacturing the semiconductor integrated circuitry of the present invention includes (a) a process for forming an element isolating area on the main surface of a semiconductor substrate; (b) a process for depositing a silicon oxide film, serving as a gate insulating film, a conductor film composed mainly with a polycrystal silicon film, serving as gate electrodes, and a silicon nitride film, serving as a cap insulating film sequentially to form a laminated film composed of those films all over the surface of the semiconductor substrate, then patterning the laminated film to form a gate insulating film, gate electrodes, and a cap insulating film; (c) a process for forming a semiconductor area in an active area on the main surface of the semiconductor substrate,

surrounded by the element isolating area by implanting impurities using the gate electrodes as a mask; (d) a process for depositing an insulating film for self-matching treatment all over the surface of the semiconductor substrate; (e) the first etching process for depositing an interlaminar insulating film all over the surface of the semiconductor substrate on which the insulating film for self-matching treatment is formed; (f) a process for etching the interlaminar insulating film on conditions to make the etching of the insulating film for self-matching treatment slower enough than the etching of the interlaminar insulating film selectively, and opening part of the connecting holes in a self-matching manner with respect to the gate electrodes; and (g) the second etching process for performing anisotropic etching for the insulating film for self-matching treatment at the bottom of each connecting hole.

According to the manufacturing method of the semiconductor integrated circuitry, since the insulating film for self-matching treatment is deposited without forming side walls after the gate electrodes and the cap insulating film are formed, the contact margin between gate electrodes can be taken enough. As a result, the reliability of the semiconductor integrated circuitry in connecting the

member formed in each connecting hole to the semiconductor area formed in an active area can be improved significantly.

In addition, since connecting holes are opened in two stages (the first and second etching processes), the connecting holes can be opened in a self-matching manner with respect to the gate electrodes, as well as the element isolating area going into the bottom of each connecting hole can be prevented from over-etching. Consequently, the integration of the semiconductor integrated circuitry is improved and the characteristics of the MISFET of the semiconductor integrated circuitry is improved to improve the reliability. The first and second etching processes in the two-stage etching can be continued processes, of course.

(8) In addition, in order to form the element isolating area in the process (a), any of the first configuration that a shallow groove is formed, then the shallow groove is covered by a silicon oxide film and the surface is polished by etching-back or with the CMP method to leave the silicon oxide film only in the shallow groove or the second configuration that a thick field insulating film formed with the thermal oxidation method selectively using a patterned silicon nitride film as a mask can be taken. According to the manufacturing method of the semiconductor integrated circuitry, it is possible to easily manufacture a semiconductor integrated circuitry

having a shallow groove element isolating area or a thick field insulating film formed with the LOCOS method.

(9) In addition, in the method for manufacturing the semiconductor integrated circuitry of the present invention, the insulating film for self-matching treatment may be a silicon nitride film and the interlaminar insulating film may be a silicon oxide film. The etching in the first etching process may be plasma etching using a mixed gas of C_4F_8 and argon and the etching in the second etching process may be plasma etching using a mixed gas of CHF_3 , CF_4 , and argon.

According to the manufacturing method of the semiconductor integrated circuitry, since plasma etching is performed using a mixed gas of C_4F_8 and argon in the first etching process, the silicon oxide film can be etched on conditions to make it difficult to etch silicon nitride films, that is, the silicon oxide film can be etched on conditions that can take an enough etching selection ratio for silicon nitride films. In addition, the interlaminar insulating film in the connecting hole area can be etched with an enough treatment margin up to the insulating film for self-matching treatment formed on the main surface of the semiconductor substrate. The insulating film for self-matching treatment functions a stopper film. In the second etching process, plasma etching can be performed

using a mixed gas of CHF_3 , CF_4 , and argon, so the insulating film for self-matching treatment, composed of a silicon nitride film, can be etched easily. And, since only comparatively a thin silicon nitride film is etched in the second etching process, the connecting holes can be opened with an enough margin and accordingly, the element isolating area can be prevented from over-etching effectively as described above.

(10) The method for manufacturing the semiconductor integrated circuitry of the present invention applies over-etching in the second etching process so that the etching time is reduced than the time necessary for etching the total thickness of the insulating film for self-matching treatment.

Such the over-etching is possible because the insulating film for self-matching treatment is used as a stopper film when in opening of the connecting holes by two-stage etching. And, because of the over-etching applied, connecting holes can be opened surely while active areas are etched slightly. The connecting reliability at the bottom of each hole can be improved. The etching depth in active areas is equal to the thickness of the insulating film for self-matching treatment or under, since the over-etching time is less than the time of etching necessary for etching the total thickness of the insulating film for

self-matching treatment. In addition, since the insulating film for self-matching treatment can be as thinned as 30 to 50nm, the over-etching arises no problem from the etching process.

(11) The method for manufacturing the semiconductor integrated circuitry of the present invention allows the DRAM memory mat area to be included in the semiconductor integrated circuitry and the method includes a process for forming side walls on side surfaces of the gate electrodes in areas other than the memory mat area and the cap insulating film with the insulating film for self-matching treatment put therebetween after the insulating film for self-matching treatment is deposited.

According to the manufacturing method of the semiconductor integrated circuitry, a proper LDD structure can be formed in every MISFET other than in the memory mat area. As a result, the channel of every MISFET in areas other than the memory mat area, for example, the channel of the MISFET in the peripheral circuit area, can be shortened to improve the performance of the MISFET. And, since it is possible to generally take a margin for the interval between gate electrodes in the peripheral circuit area, side walls can be formed on side surfaces of each gate electrode in the MISFET in the peripheral circuit area even when the

insulating film for self-matching treatment is formed there.

(12) In addition, the method for manufacturing the semiconductor integrated circuitry of the present invention allows the DRAM memory mat area to be included in the semiconductor integrated circuitry and the method includes a process for removing the insulating film for self-matching treatment at least on the main surface of the semiconductor substrate except for the memory mat area after the insulating film for self-matching treatment is deposited.

According to the manufacturing method of the semiconductor integrated circuitry, since the method includes a process for removing the insulating film for self-matching treatment from the main surface of the semiconductor substrate except for at least the memory mat area, it is possible to remove, for example, the insulating film for self-matching treatment from the peripheral circuit area of the DRAM. Thus, it is possible to easily open the connecting holes connected to the MISFET semiconductor area or the gate electrodes in the peripheral circuit area.

(13) Side walls can be formed after the insulating film for self-matching treatment is deposited by etching the insulating film for self-matching treatment using the photo resist covering the memory mat area as a mask, then by

removing the photo resist, depositing an insulating film all over the semiconductor substrate and anisotropic-etching the insulating film. The etching of the insulating film for self-matching treatment may be anisotropic etching leaving the insulating film for self-matching treatment on side surfaces of each gate electrode as side walls or isotropic etching not leaving the insulating film for self-matching treatment as side walls.

In addition, side walls can be formed after the insulating film for self-matching treatment is deposited by depositing an insulating film that covers uneven portions caused by the gate electrodes and the cap insulating film formed in the memory mat area on the insulating film and etching the insulating film by anisotropic etching. In such a case, since the insulating film fills each space between the gate electrodes in the memory mat area, the insulating film for self-matching treatment formed on the main surface of the semiconductor substrate, between the gate electrodes in the memory mat area is not etched by anisotropic etching performed later. On the other hand, the insulating film for self-matching treatment in areas other than the memory mat area, for example, in the peripheral circuit area, can be etched together with the insulating film used for forming side walls in the anisotropic etching, since it is possible to take a margin for the interval between gate electrodes

in the peripheral circuit area. In other words, it is possible to omit the mask forming process for etching only the insulating film for self-matching treatment in the peripheral circuit area. The process can thus be simplified.

Of those inventions described above, the effects obtained by representative inventions can be summarized as follows.

(1) Connecting holes can be formed in a self-matching manner even in the highly integrated DRAM memory cell area, as well as the element isolating area at the bottom of each connecting hole can be prevented from over-etching.

(2) When connecting holes are formed in a self-matching manner and the element isolating area at the bottom of each connecting hole is prevented from over-etching, the treatment margin of the connecting holes can be improved.

(3) When connecting holes are formed in a self-matching manner and the element isolating area at the bottom of each connecting hole is prevented from over-etching, the number of processes can be suppressed from increasing.

(4) The integration degree of the semiconductor integrated circuitry is more improved, as well as the refreshing characteristics of the DRAM are improved to improve the transistor characteristics of the memory cell area.

According to the investigation of well-known examples carried out by the present inventor after the present invention is made, it was found that the technologies for forming connecting holes of one side electrodes of a capacitor and forming bit line connecting holes in a self-matching manner with respect to word lines were disclosed in the public report of Unexamined Published Japanese Invention Application No.4-342164.

The technology for providing a silicon nitride film to prevent the semiconductor substrate or the element isolating insulating film from over-etching when in opening of both connecting holes of a capacitor and connecting holes of bit lines one side electrodes with respect to an interlaminar insulating film is disclosed in the public reports of Unexamined Published Japanese Patent Application No.8-264075 and No.8-344906. In addition, the technology for providing a silicon nitride film when connecting holes are opened to a source or a drain with respect to an insulating film on an MOSFET is disclosed in the official report of Unexamined Published Japanese Patent Application No.6-53162.

In addition, the method for manufacturing a semiconductor device having a double side wall film composed of a silicon nitride film and a silicon oxide film on side walls of each gate electrode is disclosed in the official

reports of Unexamined Published Japanese Patent Application No.3-276729 and No.6-168955, as well as USA Patent Filing Reports No.5, 364, and 804.

INDUSTRIAL APPLICABILITY

As described above, the semiconductor integrated circuitry and the method for manufacturing the circuitry of the present invention are suitable for fine treatment, high integration, and high reliability. Especially, they are suitable for a DRAM, an electrically reloadable nonvolatile memory or a highly integrated semiconductor circuitry provided with a logic circuit, a DRAM, or an electrically reloadable nonvolatile memory.

CLAIMS

1. A semiconductor integrated circuitry comprising first MISFET including gate electrodes formed on the main surface of a semiconductor substrate via a gate insulating film; semiconductor area in contact with a channel area formed under said gate electrodes on the main surface of said semiconductor substrate; and

second MISFET including gate electrodes formed on the main surface of the semiconductor substrate via said gate insulating film; a low density semiconductor area in contact with a channel area formed under said gate electrodes on the main surface of said semiconductor substrate; and a high density semiconductor area formed outside said low density semiconductor area, wherein

a cap insulating film is formed on top of said gate electrodes of said first and second MISFETs, first side walls formed with first insulating film are formed on side surfaces of said gate electrodes of said second MISFET, second side walls formed with second insulating film composed of a different member from that of said first insulating film are formed outside said first side walls,

a conductor portion connecting said first MISFET semiconductor area to a member formed in the upper layer of said first MISFET is formed in a self-matching manner with



respect to third side walls formed with said first insulating film, and

said high density semiconductor area is formed in a self-matching manner with respect to said second side walls formed with said second insulating film.

2. A semiconductor integrated circuitry as defined in claim 1, wherein

said first insulating film forms first and third side wall spacers composed of a silicon nitride film formed on side surfaces of said first and second MISFET gate electrodes and said second insulating film forms second side wall spacers composed of a silicon oxide film formed on side surfaces of said second MISFET gate electrodes with said side wall spacers therebetween.

3. A semiconductor integrated circuitry as defined in claim 1, wherein

said first insulating film is a silicon nitride film formed on said semiconductor substrate including side surfaces of said gate electrodes and said second insulating film is a silicon oxide film formed on side surfaces of said gate electrodes with said silicon nitride film therebetween.

4. A semiconductor integrated circuitry as defined in claim 1, 2, or 3 wherein



said second MISFET includes an N channel MISFET and a P channel MISFET and has a CMISFET structure.

5. A semiconductor integrated circuitry as defined in claim 1, 2, 3, or 4 wherein

said first MISFET is a selecting MISFET of a DRAM disposed in a memory array area of DRAM cells and said member formed in the upper layer of said first MISFET is a DRAM storage capacitor or a bit line.

6. A semiconductor integrated circuitry as defined in claim 5, wherein

an impurity doped in the semiconductor area of said selecting MISFET is phosphorus and the low density or high density semiconductor area of said N channel MISFET of said second MISFET is doped at least arsenic.

7. A semiconductor integrated circuitry as defined in claim 6, wherein

said N channel MISFET includes first N channel MISFET and second N channel MISFET and said first N channel MISFET includes an arsenic doped low density semiconductor area and an arsenic doped high density semiconductor area, and said second N channel MISFET includes a phosphorus doped low density semiconductor area and an arsenic doped high density semiconductor area.

8. A semiconductor integrated circuitry as defined in claim 7, wherein



said first N channel MISFET includes a boron doped semiconductor area in contact with said high density semiconductor area under said low density semiconductor area and said second N channel MISFET does not include said boron doped semiconductor area.

9. A semiconductor integrated circuitry as defined in claim 5, 6, 7, or 8, wherein

on the surface of said semiconductor area of said selecting MISFET is not formed a silicide layer and on the surface of said high density semiconductor area of said second MISFET is formed a silicide layer.

10. A semiconductor integrated circuitry as defined in claim 5, 6, 7, 8 or 9, wherein

said gate-insulating film of said selecting MISFET is thicker than that of said second MISFET.

11. A semiconductor integrated circuitry as defined in claim 1, 2, 3, or 4 wherein

said first MISFET, in which gate insulating film thereof is a tunnel insulating film, is a floating gate type MISFET disposed in a memory array area of nonvolatile memory cells including control gate electrodes formed on gate electrodes via floating gate electrodes and on said floating gate electrodes via an insulating film.

12. A semiconductor integrated circuitry as defined in claim 11, wherein



said gate insulating film of said second MISFET is thicker than that of said first MISFET.

13. A semiconductor integrated circuitry as defined in claim 5, 6, 7, 8, 9, 10, 11, or 12, wherein

said first MISFET includes said selecting MISFET and said floating gate type MISFET.

14. A semiconductor integrated circuitry as defined in claim 13, wherein

said DRAM bit line and a wiring formed in the upper layer of said floating gate type MISFET are formed in the same process.

15. A semiconductor integrated circuitry as defined in claim 13 or 14, wherein

insulating films of said selecting MISFET, said floating gate type MISFET, a peripheral circuit or logic circuit MISFET that drives said DRAM, and said peripheral circuit MISFET that drives said floating gate type MISFET are different in thickness from each other and said gate insulating film of said peripheral circuit MISFET that drives said floating gate type MISFET is thicker than that of said floating gate type MISFET and said gate insulating film of said floating gate type MISFET is thicker than that of said selecting MISFET, and said gate insulating film of said selecting MISFET is thicker than that of said



peripheral circuit or logic circuit MISFET that drives said DRAM.

16. A semiconductor integrated circuitry as defined in claim 1 or 15, wherein

in an area where said second MISFET is formed is formed a silicon nitride film covering said second MISFET and said semiconductor substrate.

17. A method for manufacturing a semiconductor integrated circuitry, comprising processes

(a) for forming a gate insulating film on the main surface of a semiconductor substrate;

(b) for forming plural gate electrodes and a cap insulating film on said gate insulating film;

(c) for forming a low density semiconductor area for both first and second MISFETs respectively in a self-matching manner with respect to said gate electrodes;

(d) for forming first side wall spacers on side surfaces of said gate electrodes;

(e) for forming second side wall spacers outside said first side wall spacers;

(f) for forming a high density semiconductor area in a self-matching manner with respect to said second side wall spacers of said second MISFET;



(g) for depositing an interlaminar insulating film composed of a silicon oxide film all over said semiconductor substrate;

(h) for etching said interlaminar insulating film and said second side wall spacers in a self-matching manner with respect to said first side wall spacers of said first MISFET to open connecting holes; and

(i) for forming a conductor in each of said connecting holes.

18. A method for manufacturing a semiconductor integrated circuitry, comprising processes

(a) for forming a gate insulating film on the main surface of a semiconductor substrate;

(b) for forming plural gate electrodes and a cap insulating film on said gate insulating film;

(c) for forming a low density semiconductor area for both first and second MISFETs respectively;

(d) for depositing a silicon nitride film all over said semiconductor substrate including side surfaces of said gate electrodes;

(e) for forming side wall spacers on side surfaces of said gate electrodes with said silicon nitride film therebetween;



(f) for forming a high density semiconductor area in a self-matching manner with respect to said side wall spacers of said second MISFET;

(g) for depositing an interlaminar insulating film composed of a silicon oxide film all over said semiconductor substrate;

(h) for etching said interlaminar insulating film and said side wall spacers in a self-matching manner with respect to said silicon nitride film to form openings, and further etching said silicon nitride film at the bottom of each of said openings to open connecting holes;

(i) for forming a conductor in each of said connecting holes.

19. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 17 or 18, wherein in said process (c) is implanted phosphorus in the semiconductor area of said first MISFET and at least in one or more low density semiconductor areas of said second MISFET is implanted arsenic.

20. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 17, 18, or 19, wherein

in said process (a) are formed the gate insulating films of both said first MISFET and said second MISFET in the same process.



21. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 17, 18, or 19, wherein

said process (a) for forming said gate insulating films includes a process for forming first gate insulating film in an area where said first and second MISFETs are formed; a process for removing said first gate insulating film selectively from the area where said second MISFET is formed; and a process for forming second gate insulating film in an area where said second MISFET is formed.

22. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 17 or 18, wherein

said gate insulating film is a tunnel insulating film of a floating gate type MISFET composing a nonvolatile memory and said process for forming said gate insulating film includes a process for forming floating gate electrodes of said floating gate type MISFET; and a process for forming control electrodes of said floating gate type MISFET on said floating gate electrodes via an insulating film.

23. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 17, 18, 19, 20, or 21, wherein

in prior to said process (a) is provided a process for forming a tunnel insulating film of said floating gate type MISFET composing a nonvolatile memory on the main surface



of said semiconductor substrate and forming floating gate electrodes of said floating gate type MISFET on said tunnel insulating film.

24. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 23, wherein gate electrodes formed in said process (b) can be formed in the same process as that of control gate electrodes of said floating gate type MISFET.

25. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 23 or 24, wherein said tunnel insulating film is formed thicker than said gate insulating film in said process (a).

26. A method for manufacturing a semiconductor integrated circuitry, as defined in any of claims 17 to 25, wherein

in prior to said process (g) is provided a process for depositing second silicon nitride film in an area where said second MISFET is formed, etching said interlaminar insulating film in an area where a conductor portion connecting said second MISFET to a member formed in the upper layer of said second MISFET is formed on conditions decided to take an etching selection ratio for said second silicon nitride film to form openings, further etching the second silicon nitride film at the bottom of each openings to open connecting holes, and forming said conductor portion.



27. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 26, wherein

said second silicon nitride film is formed in the same process as that of a silicon nitride film formed as said first insulating film.

28. A semiconductor integrated circuitry, comprising memory cells in each of which first MISFET and a capacity element are connected serially; and a peripheral circuit composed of plural second MISFETs, and said semiconductor integrated circuitry further includes

a semiconductor substrate having first area for forming said first MISFET; and second area for forming said plural second MISFETs;

first gate electrodes formed on the main surface of said semiconductor substrate via a gate insulating film in said first area; and second gate electrodes formed on the main surface of said semiconductor substrate via a gate insulating film in said second area;

first insulating film having the same flat surface as that of said first gate electrodes and being formed on said first electrodes in said first area, second insulating film having the same flat surface as that of said second gate electrodes and being formed on said gate electrodes in said second area;



first semiconductor area formed at both sides of said first gate electrodes in said first area and second and third semiconductor areas formed at both sides of said second gate electrodes in said second area;

first side wall spacers composed of third insulating film formed on side walls of said second gate electrodes in said second area; and second side wall spacers composed of fourth insulating film formed on side walls of said first side wall spacers;

third side wall spacers composed of third insulating film formed on side walls of said first gate electrodes in said first area; and

a conductor layer formed on said semiconductor substrate so as to come in contact with said first semiconductor area in a self-matching manner with respect to said third side wall spacers on the main surface of said semiconductor substrate, wherein

said first semiconductor area is formed in a self-matching manner with respect to said first gate electrodes, said second semiconductor area is formed in a self-matching manner with respect to said second gate electrodes, and said third semiconductor area is formed in a self-matching manner with respect to said second side wall spacers, and

said third and fourth insulating films are formed with different members from each other.



29. A semiconductor integrated circuitry, as defined in claim 28, wherein

said third insulating film is a silicon nitride film and said fourth insulating film is a silicon oxide film.

30. A semiconductor integrated circuitry, as defined in claim 29, wherein

the total width of said first side wall spacer and said second side wall spacer is greater than the width of said third side wall spacer.

31. A semiconductor integrated circuitry, as defined in claim 30, wherein

the width of said first side wall spacer is almost equal to the width of said third side wall spacer.

32. A semiconductor integrated circuitry, as defined in claim 28, wherein

said conductor layer is connected to one side electrode of said capacity element.

33. A semiconductor integrated circuitry, as defined in claim 28, further includes

a word line connected to said memory cells and extended in the row direction; and

a data line connected to said memory cells and extended in the column direction.

34. A semiconductor integrated circuitry, as defined in claim 33, wherein



said conductor layer is connected to said data line.

35. A semiconductor integrated circuitry, comprising
a word line extended in the row direction; a data line
extended in the column direction; memory cells, each of
which connected to said word line and said data line at an
intersection point of said word line and said data line; and
a peripheral circuit connected to said word line or said data
line, and said memory cell is composed of first MISFET and
a capacity element connected serially and said peripheral
circuit is composed of plural second MISFETs, wherein

said semiconductor integrated circuitry further
includes

a semiconductor substrate having first area for
forming said memory cells and second area for forming said
peripheral circuit;

two first conductor layers, each of which functions
as a word line formed on the main surface of said
semiconductor substrate in said first area; and gate
electrodes formed on the main surface of said semiconductor
substrate via a gate insulating film;

first insulating film formed on said first conductor
layer in said first area and having the same flat surface
as that of said first conductor layer; and second insulating
film formed on said gate electrodes in said second area and
having the same flat surface as that of said gate electrodes;



first semiconductor area formed on said two first conductor layers respectively in said first area; and second and third semiconductor areas formed on both sides of said gate electrodes in said second area;

first side wall spacers composed of third insulating film, formed on side surfaces of said gate electrodes; and second side wall spacers composed of fourth insulating film formed on side walls of said first side wall spacers in said second area respectively;

third side wall spacers composed of third insulating film, formed on side walls of said first conductor layer in said first area;

said main surface of said semiconductor substrate, coming in contact with said first semiconductor area in a self-matching manner with respect to said third side wall spacers between said two first conductor layers and having a conductor layer formed on said semiconductor substrate;

said first semiconductor area is formed in self-matching manner with respect to said first conductor layer, said second semiconductor area is formed in a self-matching manner with respect to said second gate electrodes, and said third semiconductor area is formed in a self-matching manner with respect to said second side wall spacers; and

said third and fourth insulating films are composed of different members from each other.



36. A method for manufacturing a semiconductor integrated circuitry having memory cells, in each of which first MISFET and a capacity element are connected serially; and a peripheral circuit composed of second MISFETs, comprising processes

(a) for preparing a semiconductor substrate having first area for forming said memory cells; and second area for forming said peripheral circuit;

(b) forming first conductor layer on said semiconductor substrate and first insulating film on said first conductor layer;

(c) for forming first MISFET gate electrodes in said first area and second MASET gate electrodes in said second area by patterning said first conductor layer and first insulating film;

(d) for implanting first conduction type impurity to form first semiconductor area in a self-matching manner with respect to said second gate electrodes in said second area;

(e) for depositing second insulating film covering said first and second gate electrodes;

(f) for forming first side wall spacers on side surfaces of said second gate electrodes in said second area by performing anisotropic etching for said second insulating film;



(g) for depositing third insulating film in said second area so as to cover said second gate electrodes and first side wall spacers;

(h) for forming second side wall spacers on side surfaces of first side wall spacers in said second area by performing anisotropic etching for said third insulating film;

(i) for implanting first conduction type impurity to form second semiconductor area in second area in a self-matching manner with respect to said second side wall spacers;

(j) for depositing fourth insulating film in said first area;

(k) for forming openings in said first area so as to overlap said first gate electrodes at some of said openings and expose the main surface of said semiconductor substrate; and

(l) for forming second conductor layer in each of said openings in said first area, wherein

said second conductor layer and said first gate electrodes are isolated electrically by said second insulating film from each other.

37. A method for manufacturing a semiconductor integrated circuitry, wherein



said second insulating film and third insulating film are formed with different members from each other.

38. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 37, wherein

between processes (e) and (f) is provided a process for forming a masking layer to cover said first area selectively, and no anisotropic etching is performed on said second insulating film in said first area in said process (f).

39. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 38, wherein

said processes (f) to (i) are performed leaving said masking layer as is.

40. A method for manufacturing a semiconductor integrated circuitry, as defined in claim 38, wherein

said process (k) includes processes

(m) for etching said fourth insulating film on conditions decided so that said fourth insulating film is etched more than said first insulating film; and

(n) for etching said first insulating film on conditions decided so that said first insulating film is etched more than said semiconductor substrate or said fourth insulating film.

41. A method for manufacturing a semiconductor integrated circuitry as defined in claim 40, wherein



between said processes (a) and (b) is further provided a process for forming an element isolating area on the surface of said semiconductor substrate.

42. A method for manufacturing a semiconductor integrated circuitry as defined in claim 41, wherein said process for forming said element isolating area includes processes

for forming a groove on the surface of said semiconductor substrate; and

for filling said groove selectively with fifth insulating film.

43. A method for manufacturing a semiconductor integrated circuitry as defined in claim 38, wherein another process is added so that after said fourth insulating film is formed, the surface of said fourth insulating film is polished.

44. A method for manufacturing a semiconductor integrated circuitry as defined in claim 36, wherein

in said process (f) is also formed first side wall spacers on side surfaces of said first gate electrodes in said first area.

45. A method for manufacturing a semiconductor integrated circuitry as defined in claim 44, wherein



said process (k) is performed on conditions decided so that said fourth insulating film is etched more than said second insulating film.

46. A method for manufacturing a semiconductor integrated circuitry as defined in claim 45, wherein said second insulating film is a silicon nitride film and said fourth insulating film is a silicon oxide film.

47. A method for manufacturing a semiconductor integrated circuitry as defined in claim 46, wherein another process for polishing fourth insulating film after said fourth insulating film is formed is added.

48. A method for manufacturing a semiconductor integrated circuitry having memory cells, in each of which first MISFET and a capacity element are connected serially; and a peripheral circuit composed of second MISFET, comprising processes

(a) for preparing a semiconductor substrate having first area for forming said memory cells and second area for forming said peripheral circuit;

(b) for forming first conductor layer on said semiconductor substrate and first insulating film on said first conductor layer;

(c) for patterning said first conductor layer and first insulating film to form first MISFET gate electrodes



in said first area and second MISFET second gate electrodes in said second area;

(d) implanting first conduction type impurity to form first semiconductor area in said second area in a self-matching manner with respect to said second gate electrodes;

(e) for depositing second insulating film so as to cover said first and second gate electrodes;

(f) for performing anisotropic etching for said second insulating film in said second area to form first side wall spacers on side surfaces of said second gate electrodes;

(g) for depositing third insulating film in said second area so as to cover said second gate electrodes and first side wall spacers;

(h) for performing anisotropic etching for said third insulating film to form second side wall spacers on side walls of said first side wall spacers in said second area;

(i) for implanting first conduction type impurity to form second semiconductor area in a self-matching manner with respect to said second side wall spacers in said second area;

(j) for depositing a high-melting point metal on the surface of said second semiconductor area in said second area;



(k) for performing a thermal treatment for the surface of said second semiconductor area to form a high-melting metallic silicide layer thereon;

(l) for removing non-reacted high-melting point metal;

(m) for depositing fourth insulating film in said first area;

(n) for forming openings in said first area so that some of said openings overlap on said first gate electrodes and part of the main surface of said semiconductor substrate is exposed; and

(o) for forming second conductor layer in each of said openings in said first area, wherein

said second conductor layer and said first gate electrodes are isolated by said second insulating film electrically.

49. A semiconductor integrated circuitry having memory cells, in each of which first MISFET and a capacity element are connected serially; and a peripheral circuit composed of plural second MISFETs, further including

a semiconductor substrate having first area for forming said first MISFET and second area for forming said second MISFETs;

first gate electrodes formed on the main surface of said semiconductor via a gate insulating film in said first



area; and second gate electrodes formed on the main surface of said semiconductor substrate via a gate insulating film in said second area;

first insulating film formed on said gate electrodes in said first area and having the same flat surface as that of said first gate electrodes; and second insulating film formed on said second gate electrodes in said second area and having the same flat surface as that of said second gate electrodes;

first semiconductor area formed at both ends of said first gate electrodes respectively in said first area; and second and third semiconductor areas formed at both ends of said second gate electrodes;

first side wall spacers formed on side walls of said first gate electrodes in said first area;

second side wall spacers formed on side walls of said second gate electrodes in said second area; and

a conductor layer formed on said semiconductor substrate, coming in contact with said first semiconductor area in a self-matching manner with respect to said first side wall spacers on the main surface of said semiconductor substrate; wherein

said first semiconductor area is formed in a self-matching manner with respect to said first gate electrodes, said second semiconductor area is formed in a self-matching



manner with respect to said second gate electrodes, and said third semiconductor area is formed in a self-matching manner with respect to said second side wall spacers, and

said first side wall spacer is narrower than said second side wall spacer.

