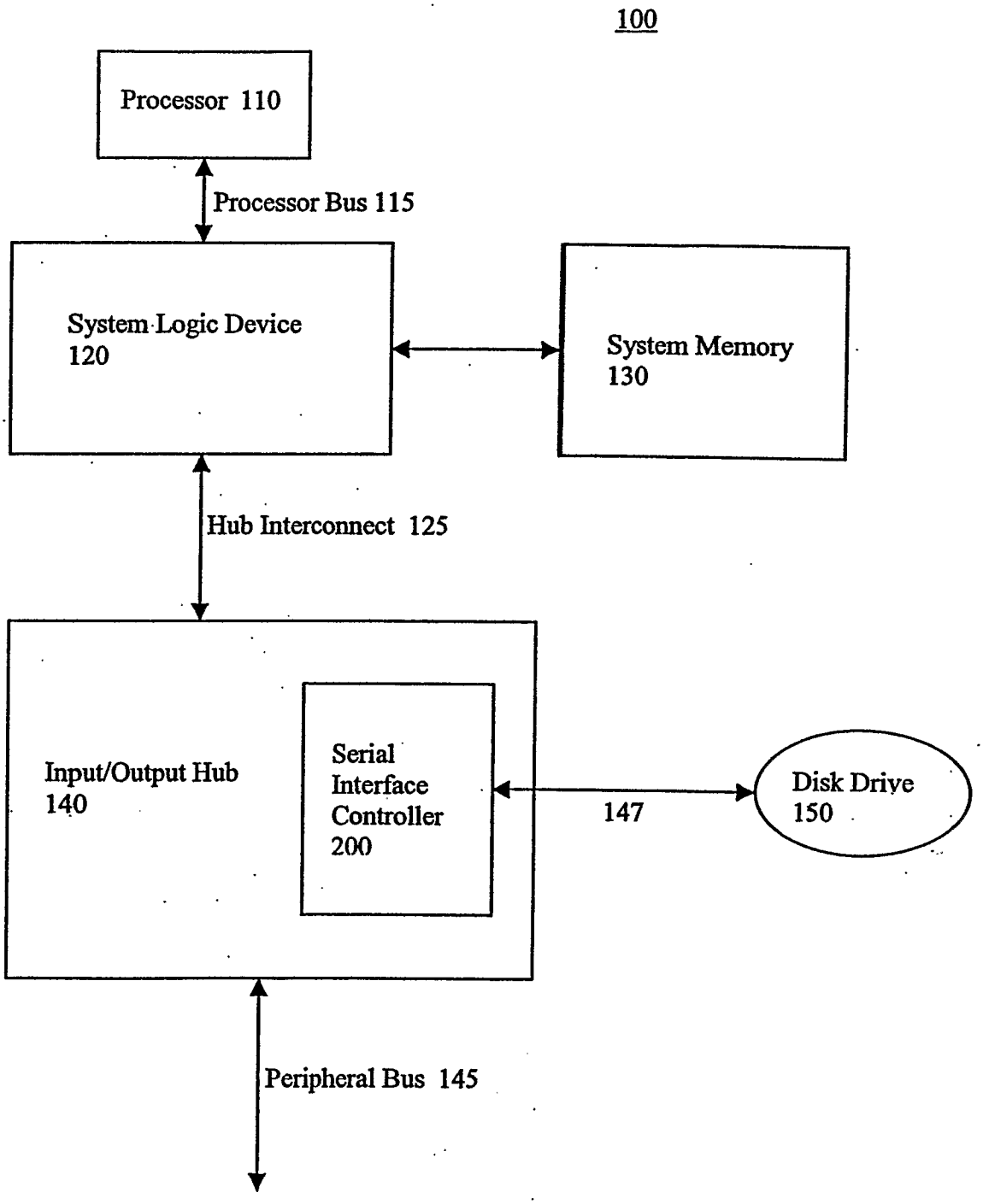

100
Processor 110
Processor Bus 115
System Logic Device 120
System Memory 130
Hub Interconnect 125
Input/Output Hub 140
Serial Interface Controller 200
147
Disk Drive 150
Peripheral Bus 145

Figure 1

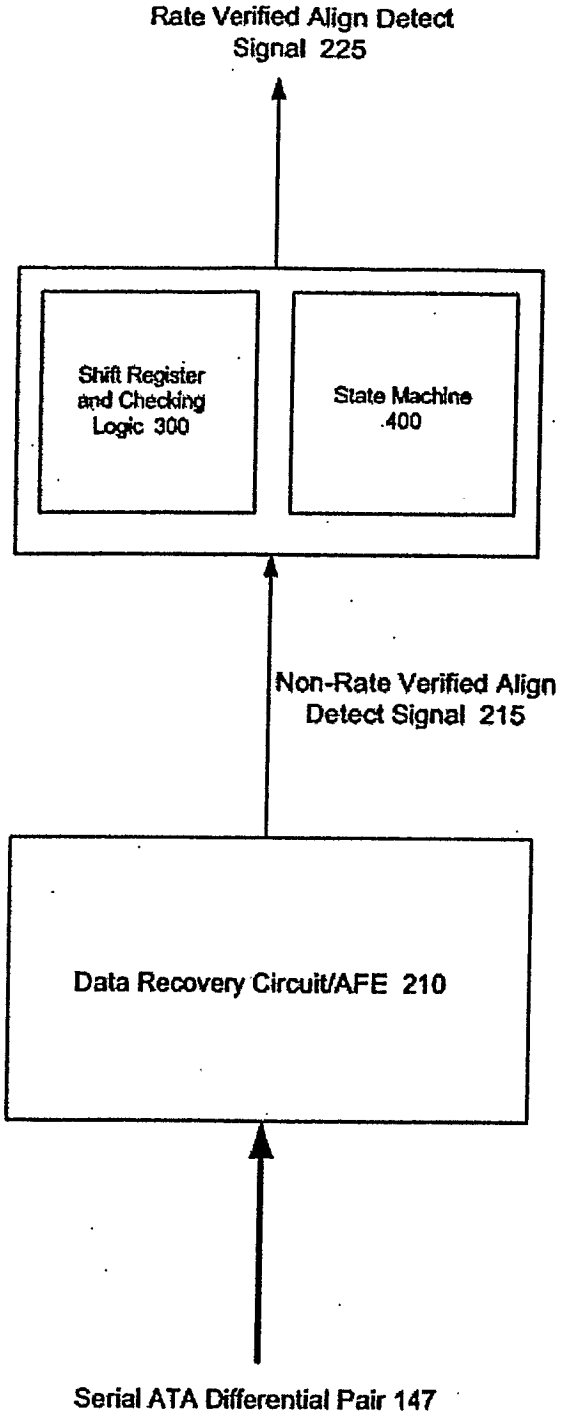

Rate Verified Align Detect Signal 225
Shift Register and Checking Logic 300
State Machine 400
Non-Rate Verified Align Detect Signal 215
Data Recovery Circuit/AFE 210
Serial ATA Differential Pair 147

Figure 2

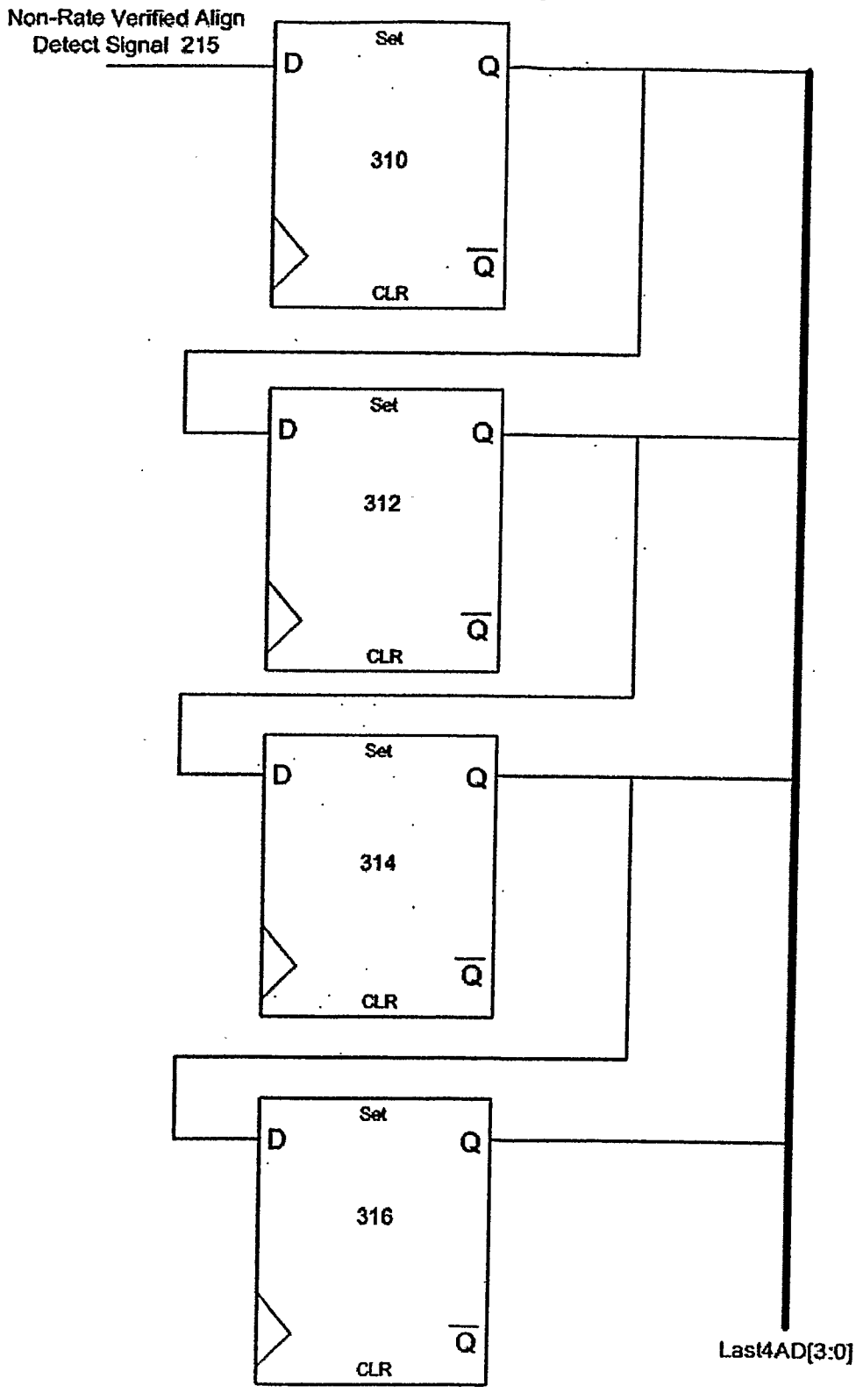

Non-Rate Verified Align
Detect Signal 215
Set
D
Q
310
Q
CLR
Set
D
Q
312
Q
CLR
Set
D
Q
314
Q
CLR
Set
D
Q
316
Q
CLR
Last4AD[3:0]

Figure 3a

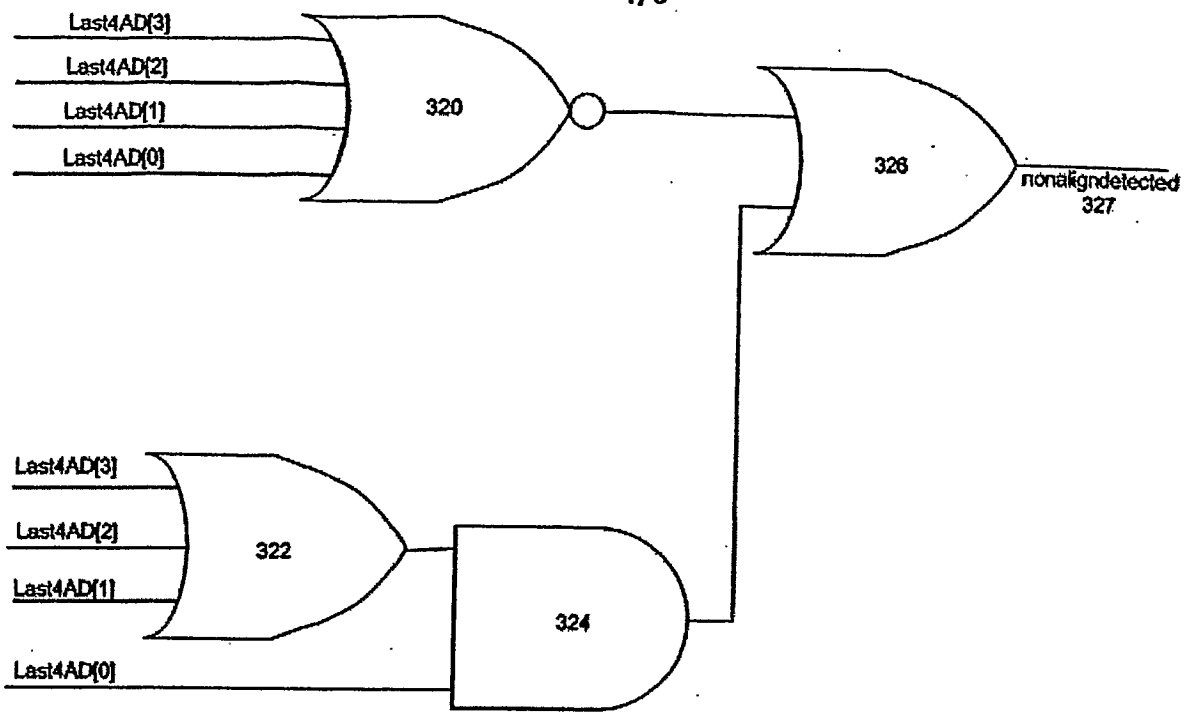

Last4AD[3]
Last4AD[2]
Last4AD[1]
Last4AD[0]
320
326
nonalignd etected
327
Last4AD[3]
Last4AD[2]
Last4AD[1]
Last4AD[0]
322
324

Figure 3b

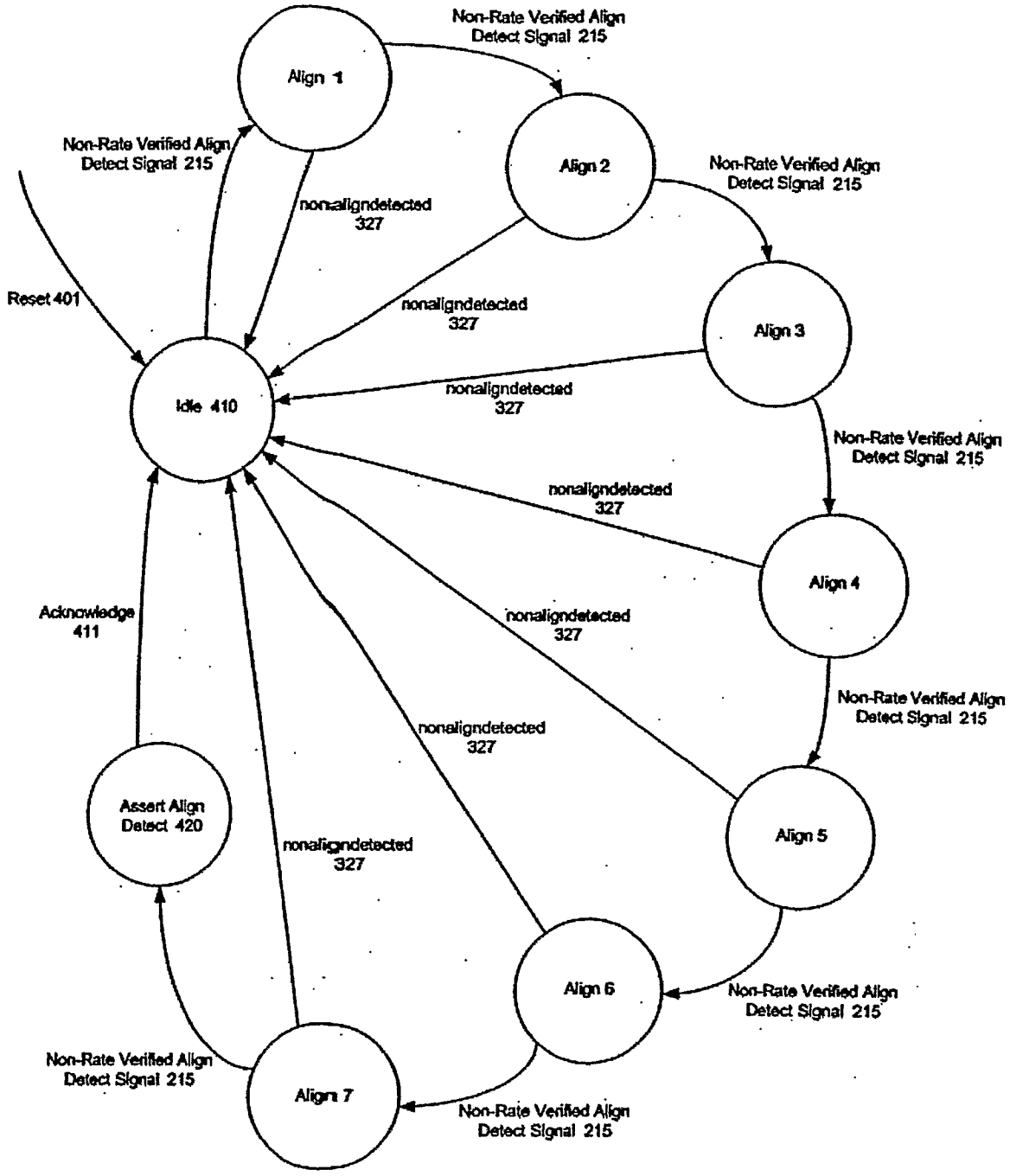

Align 1
Non-Rate Verified Align Detect Signal 215
Align 2
Non-Rate Verified Align Detect Signal 215
Align 3
Non-Rate Verified Align Detect Signal 215
Align 4
Non-Rate Verified Align Detect Signal 215
Align 5
Non-Rate Verified Align Detect Signal 215
Align 6
Non-Rate Verified Align Detect Signal 215
Align 7
Non-Rate Verified Align Detect Signal 215
Non-Rate Verified Align Detect Signal 215
nonalignderected 327
Reset 401
Idle 410
nonalignderected 327
nonalignderected 327
nonalignderected 327
nonalignderected 327
nonalignderected 327
Acknowledge 411
Assert Align Detect 420
nonalignderected 327

Figure 4

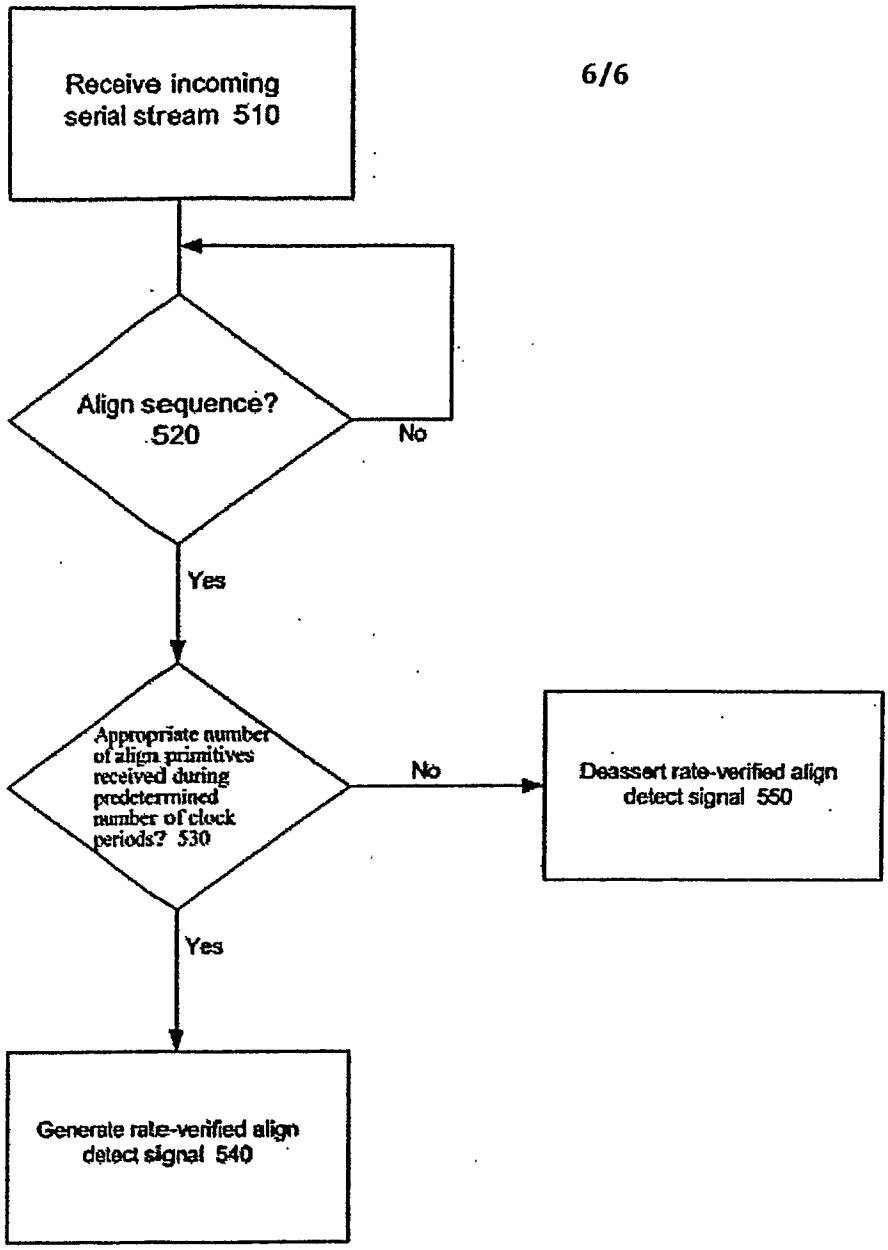

Receive incoming serial stream 510
Align sequence? 520
No
Yes
Appropriate number of align primitives received during predetermined number of clock periods? 530
No
Deassert rate-verified align detect signal 550
Yes
Generate rate-verified align detect signal 540

Figure 5