

ABSTRACT

A receiver includes a differential signal generator receiving a single-ended signal, and generating differential signals having a positive signal and a negative signal based on the single-ended signal, a reference signal, and a pair of compensation signals, a pair of charging circuits charging first and second nodes to a power level in a logic low period of a clock signal, a pair of discharging circuits discharging the first and second nodes according to a level of the positive signal and a level of the negative signal, respectively, in a logic high period of the clock signal, a comparator comparing signal levels of the first and second nodes and outputting an offset detection signal of the differential signals, and an offset compensator outputting the reference signal and the pair of compensation signals, each adjusted based on the offset detection signal, to the differential signal generator.

FIG. 4

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