SUMMARY OF THE INVENTION

It is an object of the present invention to ameliorate one or more disadvantages of the prior art.

According to one aspect of the present invention there is provided a method of operating a processing system, comprising:

executing fetched instructions in said processing system;

operating said processing system in a first power mode during which fetch circuitry in said processing system fetch up to N number of instructions from a memory per cycle of said fetch circuitry, wherein N is an integer number and $N>1$; and

operating said processing system in a second power mode during which said fetch circuitry fetch up to M number of instructions from said memory per cycle of said fetch circuitry, wherein M is an integer number and $0<M<N$.

According to a second aspect of the present invention there is provided circuitry in a data processing system, comprising:

means for executing fetched instructions in said processing system;

means for fetching up to N number of instructions from a memory per cycle of fetch circuitry in said processing system while said fetch circuitry operates in a first power mode, wherein N is an integer number and $N>1$; and

means for fetching up to M number of instructions from said memory per cycle of said fetch circuitry while said fetch circuitry operates in a second power mode, wherein M is an integer number and $0<M<N$.

CLAIMS

1. A method of operating a processing system, comprising:

executing fetched instructions in said processing system;

operating said processing system in a first power mode during which fetch circuitry in said processing system fetch up to N number of instructions from a memory per cycle of said fetch circuitry, wherein N is an integer number and $N>1$; and

operating said processing system in a second power mode during which said fetch circuitry fetch up to M number of instructions from said memory per cycle of said fetch circuitry, wherein M is an integer number and $0<M<N$.

2. The method of claim 1 wherein said first power mode is a full power mode, and said second power mode is a low power mode.

3. The method of claim 1 wherein said fetch circuitry operates in said second power mode in response to a software event.

4. The method of claim 1 wherein said fetch circuitry operates in said second power mode in response to a hardware event.

5. The method of claim 4 wherein said hardware event occurs when a temperature of said processing system exceeds a threshold temperature.

6. The method of claim 5 wherein said threshold temperature is a maximum safe temperature of said processing system operating in said first power mode.

7. The method of claim 1 wherein said memory is cache memory.

8. The method of claim 7 wherein said cache memory is an instruction cache memory.

9. The method of claim 7 and comprising disabling a group of sense amplifiers coupled to cells of said cache memory storing instructions other than said M instructions while said fetch circuitry operates in said second power mode.

10. Circuitry in a data processing system, comprising:

means for executing fetched instructions in said processing system;

means for fetching up to N number of instructions from a memory per cycle of fetch circuitry in said processing system while said fetch circuitry operates in a first power mode, wherein N is an integer number and $N > 1$; and

means for fetching up to M number of instructions from said memory per cycle of said fetch circuitry while said fetch circuitry operates in a second power mode, wherein M is an integer number and $0 < M < N$.

11. The circuitry of claim 10 wherein said first power mode is a full power mode, and said second power mode is a low power mode.

12. The circuitry of claim 10 wherein said fetch circuitry operates in said second power mode in response to a software event.

13. The circuitry of claim 10 wherein said fetch circuitry operates in said second power mode in response to a hardware event.

14. The circuitry of claim 13 wherein said hardware event occurs when a temperature of said processing system exceeds a threshold temperature.

15. The circuitry of claim 14 wherein said threshold temperature is a maximum safe temperature of said processing system operating in said first power mode.

16. The circuitry of claim 10 wherein said memory is cache memory.

17. The circuitry of claim 16 wherein said cache memory is an instruction cache memory.

18. The circuitry of claim 16 and comprising circuitry for disabling a group of sense amplifiers coupled to cells of said cache memory storing instructions other than said M instructions while said fetch circuitry operates in said second power mode.

SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION IN AN ELECTRONIC CIRCUIT

ABSTRACT OF THE DISCLOSURE

While fetch circuitry operates in a first power mode, per cycle of the fetch circuitry, up to N number of instructions are fetched from a memory, where N is an integer number and $N > 1$. While the fetch circuitry operates in a second power mode, per cycle of the fetch circuitry, up to M number of instructions are fetched from the memory, where M is an integer number and $0 < M < N$.

Fig. 2