

ABSTRACT OF THE DISCLOSURE

A memory system and a buffer device include a structure for performing training operations for a plurality of memory devices to ensure data reliability. A memory controller is configured to control a memory operation for a plurality of memory devices. A memory module includes the plurality of memory devices and a buffer device connected between the memory devices and the memory controller. Training operations for the memory devices to be performed by the buffer device including a training block with a signal delay circuit, and the memory controller performs the training operations by controlling the training block.

FIG. 1